PRETEC Datasheet

Super-Thin Lynx IDE SSD

Version 1.0

Dec 2013

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Document Version

Version	Description	Date	Editor	Approved by
1.0	New issue	Dec, 2013	Justin Hsu	Richard Wei

Pretec/C-ONE Technology Corp.

Contents

1. Introduction

1.1 General Description

Pretec Super-Thin Lynx IDE SSD uses SLC NAND flash, which leads to its remarkable high performance and comes with capacities 512MB to 8GB. The IDE SSD performs sequential read/write for each sector (512 bytes) count. It also conforms to IDE Specification and is designed with precision mechanics to enable host devices to read/write from the IDE interface into Flash Media. It can operate with a 5V single power from the host side. Pretec 2.5" Super-Thin Lynx IDE SSD has been approved through various compatibility tests.

1.2 Features

- IDE interface
  ATA command set compatible
  Support for 8-bit or 16-bit host data transfer
  Compatibility with host ATA disk I/O BIOS, DOS/Windows file system, utilities and application software
- Extremely rugged and reliable
  Advanced defect block management
  Support background erased operation
  Dynamic Wear-Leveling
- 5 Volt power supply, very low power consumption
  Zero-power data retention, no batteries required
- Automatic on-the-fly, in-buffer Error Correcting
- Hardware Error Correcting of 4 bits random error per sector
- Mode access
  - PIO Mode 6
  - UDMA Mode 4
  - Supported Multi word DMA Mode 4

1.3 Part Number Definition

Code	Definition	symbol	Description
X_1X_2	Interface	PA	2.IDE
X_3 X_4 X_5 X_6	Solution	L100	Lynx Series
X_7 X_8 X_9 X_{10}	Capacity	512M	512MB
		001G	1GB
		002G	2GB
		004G	4GB
		008G	8GB
X_{11}	Housing	M	Metal housing
X_{12}	-	-	-
X_{13}	Temperature Range	C	Commercial Grade 0°C ~ +70°C
		H	Industrial Grade -40°C ~ +85°C
X_{14}	Solution	A	Async SLC

1.4 Ordering Information

Part Number	Capacity	Description
PAL100512MM-CA	512MB	Super-Thin Lynx SSD 512MB, Commercial
PAL100001GM-CA	1GB	Super-Thin Lynx SSD 1GB, Commercial
PAL100002GM-CA	2GB	Super-Thin Lynx SSD 2GB, Commercial
PAL100004GM-CA	4GB	Super-Thin Lynx SSD 4GB, Commercial
PAL100008GM-CA	8GB	Super-Thin Lynx SSD 8GB, Commercial

Part Number	Capacity	Description
PAL100512MM-HA	512MB	Super-Thin Lynx SSD 512MB, Industrial
PAL100001GM-HA	1GB	Super-Thin Lynx SSD 1GB, Industrial
PAL100002GM-HA	2GB	Super-Thin Lynx SSD 2GB, Industrial
PAL100004GM-HA	4GB	Super-Thin Lynx SSD 4GB, Industrial
PAL100008GM-HA	8GB	Super-Thin Lynx SSD 8GB, Industrial

3. Product Specification

3.1 Operation and Environment Description

Operating Voltage	DC Input Power	5V ± 10%	
Typical Power Consumptions	5V	Read Mode: 119mA (Max.)	
		Write Mode: 107mA (Max.)	
		Standby Mode: 1.9mA (Approach values)	
Environment Conditions	Operating Temperature	Normal Temp.	0°C to +70°C
		Industrial Temp.	-40°C to +85°C
	Storage Temperature	-55°C to +95°C	
	Humidity Operation	5% to 95% (Non-condensing)	
	Humidity Non-operation	5% to 95% (Non-condensing)	
	Shock Operation	3000-G (Max.) (duration 0.5ms, half sine wave)	
	Shock Non-operation	3000-G (Max.) (duration 0.5ms, half sine wave)	
	Vibration Operation	30-G (Peak to peak to maximum)	
	Vibration Non-operation	30-G (Peak to peak to maximum)	
Operation System Supported	DOS, Windows 98/ME/NT/2000/XP/7/8		

3.2 Physical Description

Measures	L x W x H 69.85 x 100.2 x 5.8 (mm)	
Storage Capacities	Capacity	512MB, 1GB, 2GB, 4GB, 8GB
Performance	Data Transfer Rates	Read speed up to 35 MB/s (Max.)
		Write speed up to 16 MB/s (Max.)
Reliability	MTBF	3,000,000 hours
	Error Correction	Error Correcting of 4 bits random error per sector
	R/W Test	Testdisk: 3,000,000 Read/Write cycles

4. Support Flash Media

4.1Logical Format Parameters (CHS)

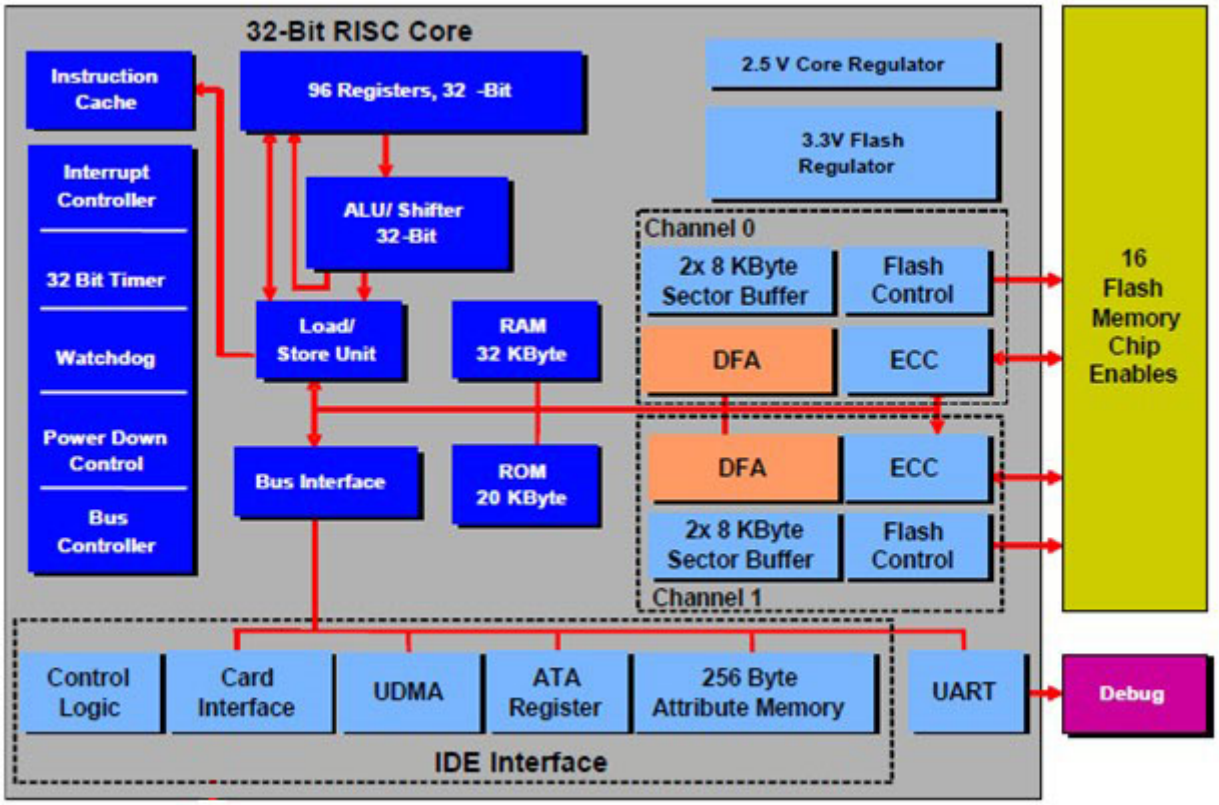
Card Density*1	512MB	1GB	2GB	4GB	8GB
Cylinder	1009	2,025	4,058	8,123	16,254
Heads	16	16	16	16	16
Sectors/Track*2	63	63	63	63	63
Total Sectors/Card*3	1,017,072	2,041,200	4,090,464	8,187,984	16,384,032
Capacity	Depended on file management				

Unit: Bytes

Notes:
*1. It's the logical address capacity including the area which is used for file system.
*2. Total tracks = number of head x number of cylinder.
*3. Total sector/Card = sector/track x number of head x number of cylinder.

5. Block Diagram

5.1 Controller Archive



6.Specification and Features

6.1 Electrical Specification

6.1.1 Recommended Operating Conditions

Operating Conditions	Min.	Typ.	Max.
I/O DC Supply Voltage (5V)	4.5 V	5 V	5.5 V
Temperature	-40°C	25°C	85°C

6.1.2 DC Characteristics for Host Interface

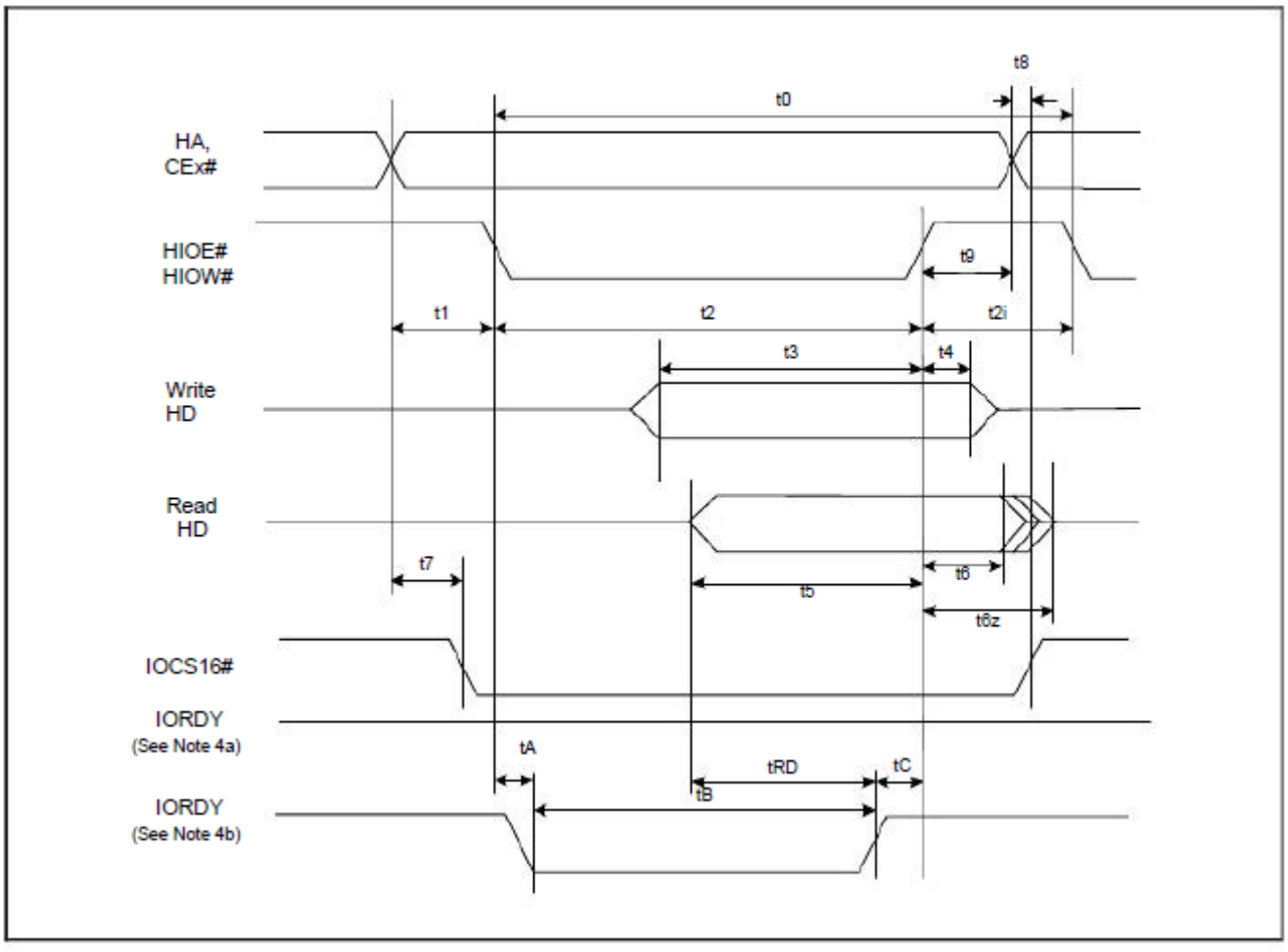
Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage 5V(From Host)	VCC	4.5	5.5	V	
High Level Output Voltage	VOH	2.5		V	
Low Level Output Voltage	VOL		0.4	V	
High Level Input Voltage	VIH	2.4		V	Non-Schmitt trigger
		2.05		V	Schmitt trigger
Low Level Input Voltage	VIL		0.6	V	Non-Schmitt trigger
			1.25	V	
Pull-Up Resistance	RPU	52.7	141	kΩ	
Pull-Down Resistance	RPD	47.5	172	kΩ	

6.1.3 True IDE Mode PIO (Read/Write) Timing Specification

	Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
t0	Cycle time (Min.)	600	383	240	180	120	100	80
t1	Address valid to HIOE# / HIOW# setup (Min.)	70	50	30	30	25	15	10
t2	HIOE# / HIOW# (Min.)	165	125	100	80	70	65	55
t2	HIOE# / HIOW# (Min.) Register (8-bit)	290	290	290	80	70	65	55
t2i	HIOE# / HIOW# recovery time (Min.)	-	-	-	70	25	25	20
t3	HIOW# data setup (Min.)	60	45	30	30	20	20	15
t4	HIOW# data hold (Min.)	30	20	15	10	10	5	5
t5	HIOE# data setup (Min.)	50	35	20	20	20	15	10
t6	HIOE# data hold (Min.)	5	5	5	5	5	5	5

t6Z	HIOE# data tristate (Max.)	30	30	30	30	30	20	20
t7	Address valid to IOCS16# assertion (Max.)	90	50	40	n/a	n/a	n/a	n/a
t8	Address valid to IOCS16# released (Max.)	60	45	30	n/a	n/a	n/a	n/a
t9	HIOE# / HIOW# to address valid hold	20	15	10	10	10	10	10
tRD	Read Data valid to IORDY active (Min.), ifIORDY initially low after tA	0	0	0	0	0	0	0
tA	IORDY Setup time	35	35	35	35	35	na	na
tB	IORDY Pulse Width (Max.)	1250	1250	1250	1250	1250	na	na
tC	IORDY assertion to release (Max.)	5	5	5	5	5	na	na

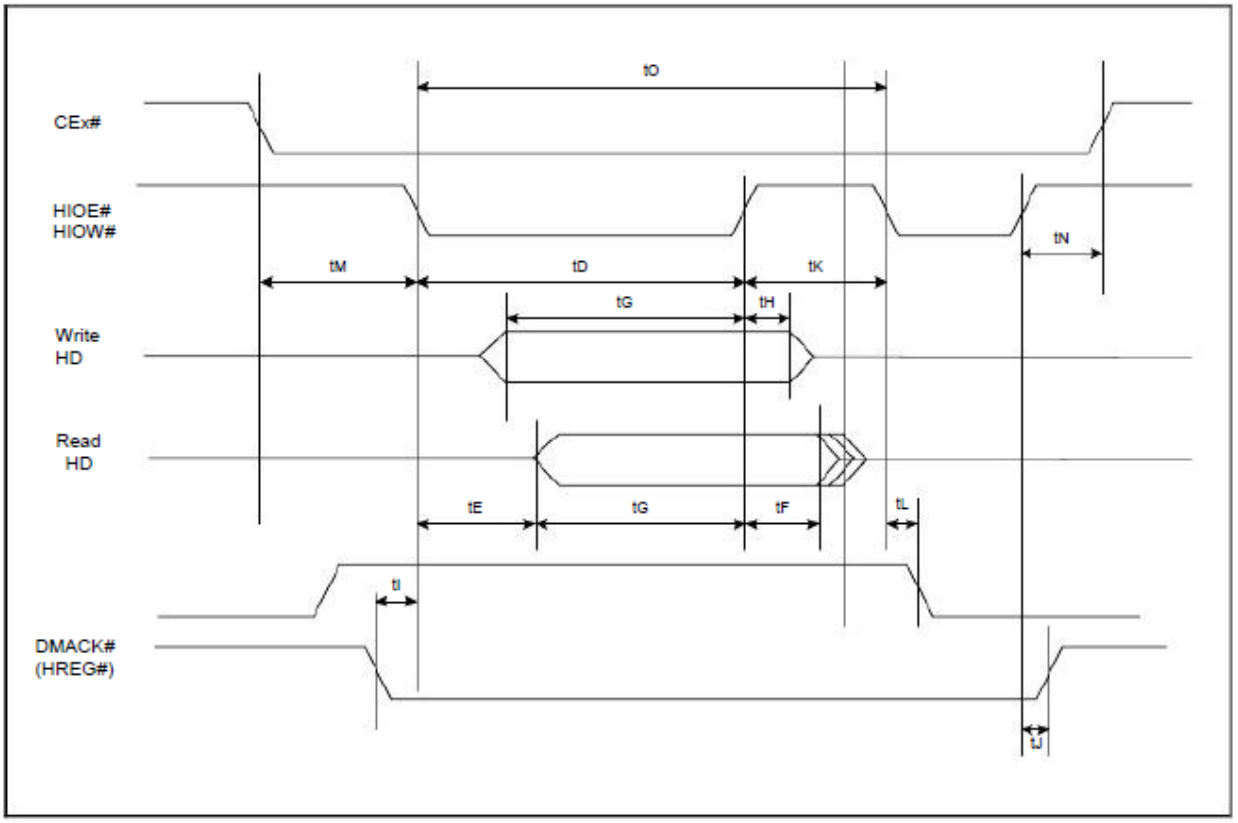
6.1.4 True IDE PIO Mode Read/Write Timing Diagram



6.1.5 True IDE Multiword DMA Mode I/O (Read/Write) Timing Specification

	Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Unit
tO	Cycle time (Min.)	480	150	120	100	80	ns
tD	HIOE# / HIOW# asserted width (Min.)	215	80	70	65	55	ns
tE	HIOE# data access (Max.)	150	60	50	50	45	ns
tF	HIOE# data hold (Min.)	5	5	5	5	5	ns
tG	HIOE# / HIOW# data setup (Min.)	100	30	20	15	10	ns
tH	HIOW# data hold (Min.)	20	15	10	5	5	ns
tI	HREG# to HIOE# / HIOW# setup (Min.)	0	0	0	0	0	ns
tJ	HIOE# / HIOW# to HREG# hold (Min.)	20	5	5	5	5	ns
tKR	HIOE# negated width (Min.)	50	50	25	25	20	ns
tKW	HIOW# negated width (Min.)	215	50	25	25	20	ns
tLR	HIOE# to DMARQ delay (Max.)	120	40	35	35	35	ns
tLW	HIOW# to DMARQ delay (Max.)	40	40	35	35	35	ns
tM	CEx# valid to HIOE# / HIOW#	50	30	25	10	5	ns
tN	CEx# hold	15	10	10	10	10	ns

6.1.6 True IDE Multiword DMA Mode Read/Write Timing Diagram



6.1.7 Ultra DMA Data Burst Timing Requirements

Name	UDMA Mode 0		UDMA Mode 1		UDMA Mode 2		UDMA Mode 3		UDMA Mode 4		UDMA Mode 5		UDMA Mode 6		UDMA Mode 7	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t2CYCTYP	240		160		120		90		60		40		30		24	
tCYC	112		73		54		39		25		16.8		13.0		10	
t2CYC	230		153		115		86		57		38		29		23	
tDS	15.0		10.0		7.0		7.0		5.0		4.0		2.6		2.5	
tDH	5.0		5.0		5.0		5.0		5.0		4.6		3.5		2.9	
tDVS	70.0		48.0		31.0		20.0		6.7		4.8		4.0		2.9	
tDVH	6.2		6.2		6.2		6.2		6.2		4.8		4.0		3.2	
tCS	15.0		10.0		7.0		7.0		5.0		5.0		5.0		5.0	

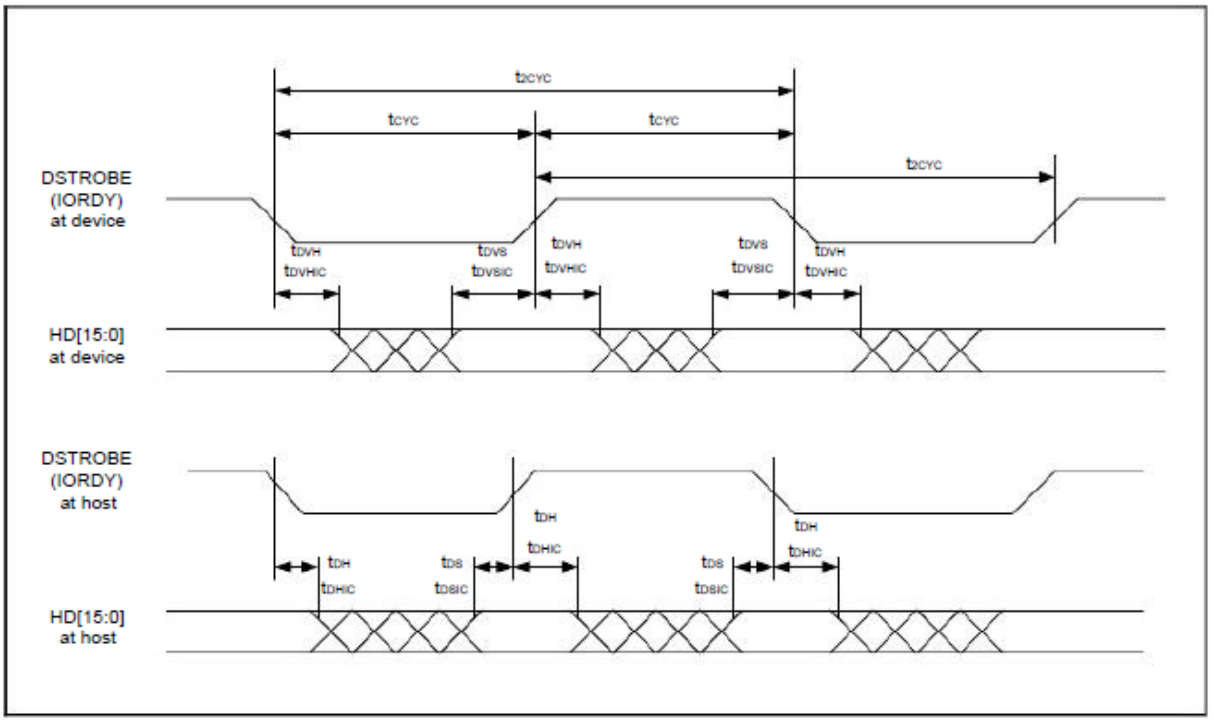
tCH	5.0		5.0		5.0		5.0		5.0		5.0		5.0		5.0	
tCVS	70.0		48.0		31.0		20.0		6.7		10.0		10.0		10.0	
tCVH	6.2		6.2		6.2		6.2		6.2		10.0		10.0		10.0	
tZFS	0		0		0		0		0		35		25		15.0	
tDZFS	70.0		48.0		31.0		20.0		6.7		25		17.5		10.5	
tFS		230		200		170		130		120		90		80		70
tLI	0	150	0	150	0	150	0	100	0	100	0	75	0	60		50
tMLI	20		20		20		20		20		20		20		20	
tUI	0		0		0		0		0		0		0		0	
tAZ		10		10		10		10		10		10		10		10
tZAH	20		20		20		20		20		20		20		20	
tZAD	0		0		0		0		0		0		0		0	
tENV	20	70	20	70	20	70	20	55	20	55	20	50	20	50	20	50
tRFS		75		70		60		60		60		50		50		50
tRP	160		125		100		100		100		85		85		85	
tIORDYZ		20		20		20		20		20		20		20		20
tZIORDY	0		0		0		0		0		0		0		0	
tACK	20		20		20		20		20		20		20		20	
tSS	50		50		50		50		50		50		50		50	

6.1.8 Ultra DMA Data Burst Timing Descriptions

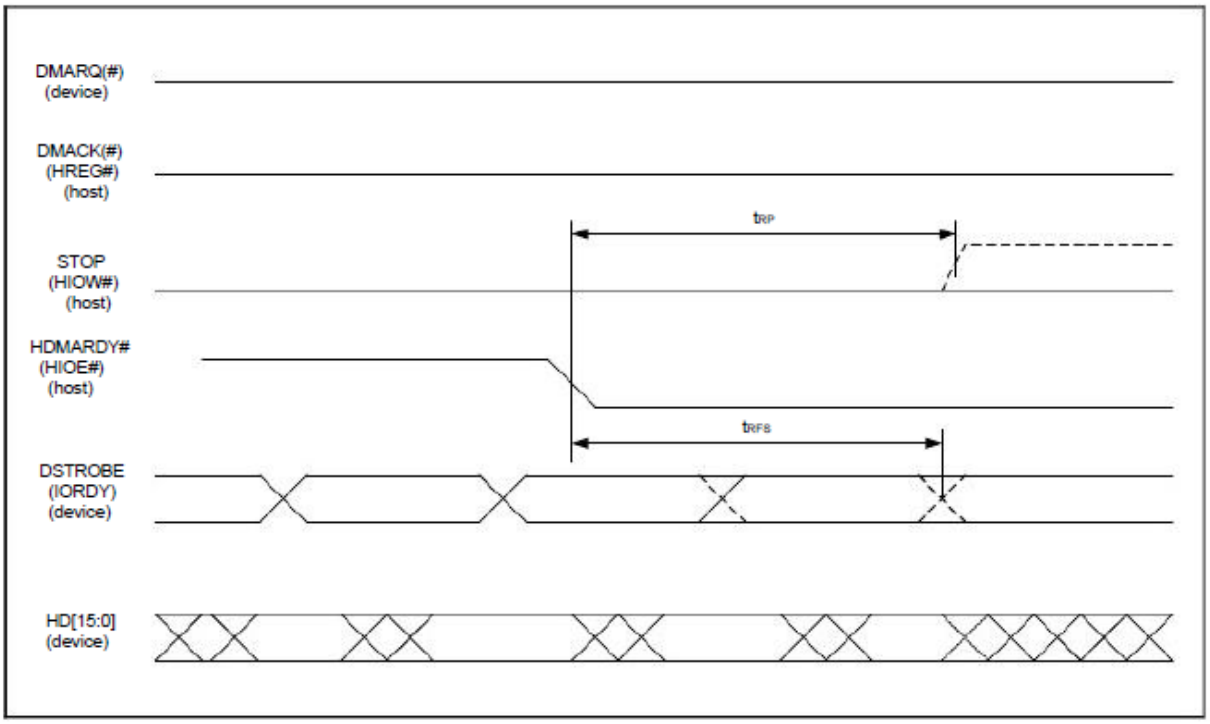
Name	Comment
t2CYCTYP	Typical sustained average two cycle time
tCYC	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)
t2CYC	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)
tDS	Data setup time at recipient (from data valid until STROBE edge)
tDH	Data hold time at recipient (from STROBE edge until data may become invalid)
tDVS	Data valid setup time at sender (from data valid until STROBE edge)
tDVH	Data valid hold time at sender (from STROBE edge until data may become invalid)
tCS	CRC word setup time at device
tCH	CRC word hold time at device
tCVS	CRC word valid setup time at host (from CRC valid until DMACK(#) negation)

tCVH	CRC word valid hold time at sender (from DMACK(#) negation until CRC may become invalid)
tZFS	Time from STROBE output released-to-driving until the first transition of critical timing.
tDZFS	Time from data output released-to-driving until the first transition of critical timing.
tFS	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)
tLI	Limited interlock time
tMLI	Interlock time with minimum
tUI	Unlimited interlock time
tAZ	Maximum time allowed for output drivers to release (from asserted or negated)
tZAH	Minimum delay time required for output
tZAD	drivers to assert or negate (from released)
tENV	Envelope time (from DMACK(#) to STOP and HDMARDY# during data in burst initiation and from DMACK(#) to STOP during data out burst initiation)
tRFS	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY#)
tRP	Ready-to-pause time (that recipient shall wait to pause after negating DMARDY#)
tIORDYZ	Maximum time before releasing IORDY
tZIORDY	Minimum time before driving IORDY
tACK	Setup and hold times for DMACK(#) (before assertion or negation)
tSS	Time from STROBE edge to negation of DMARQ(#) or assertion of STOP (when sender terminates a burst)

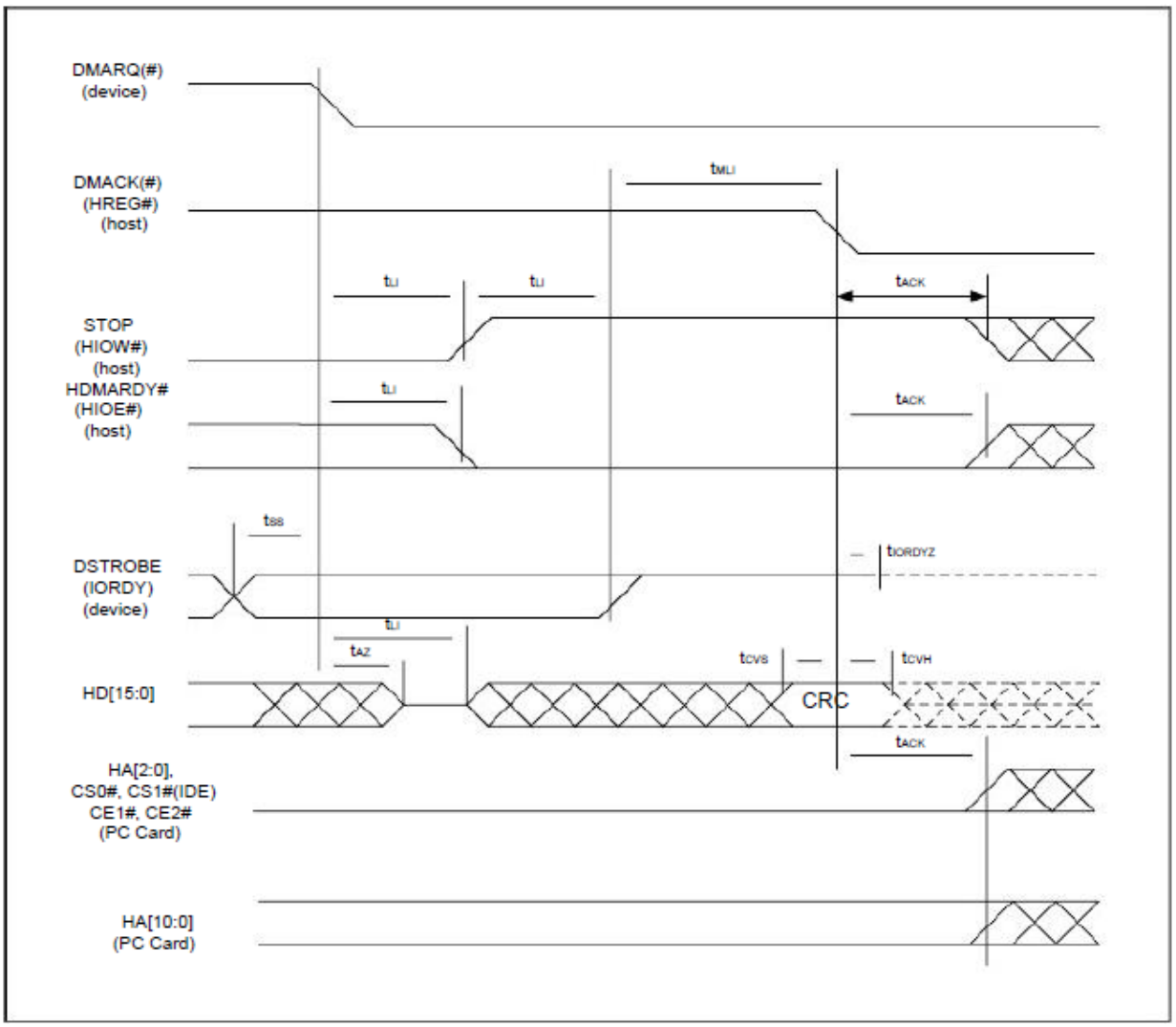
6.1.9 Sustained Ultra DMA Data-In Burst Timing



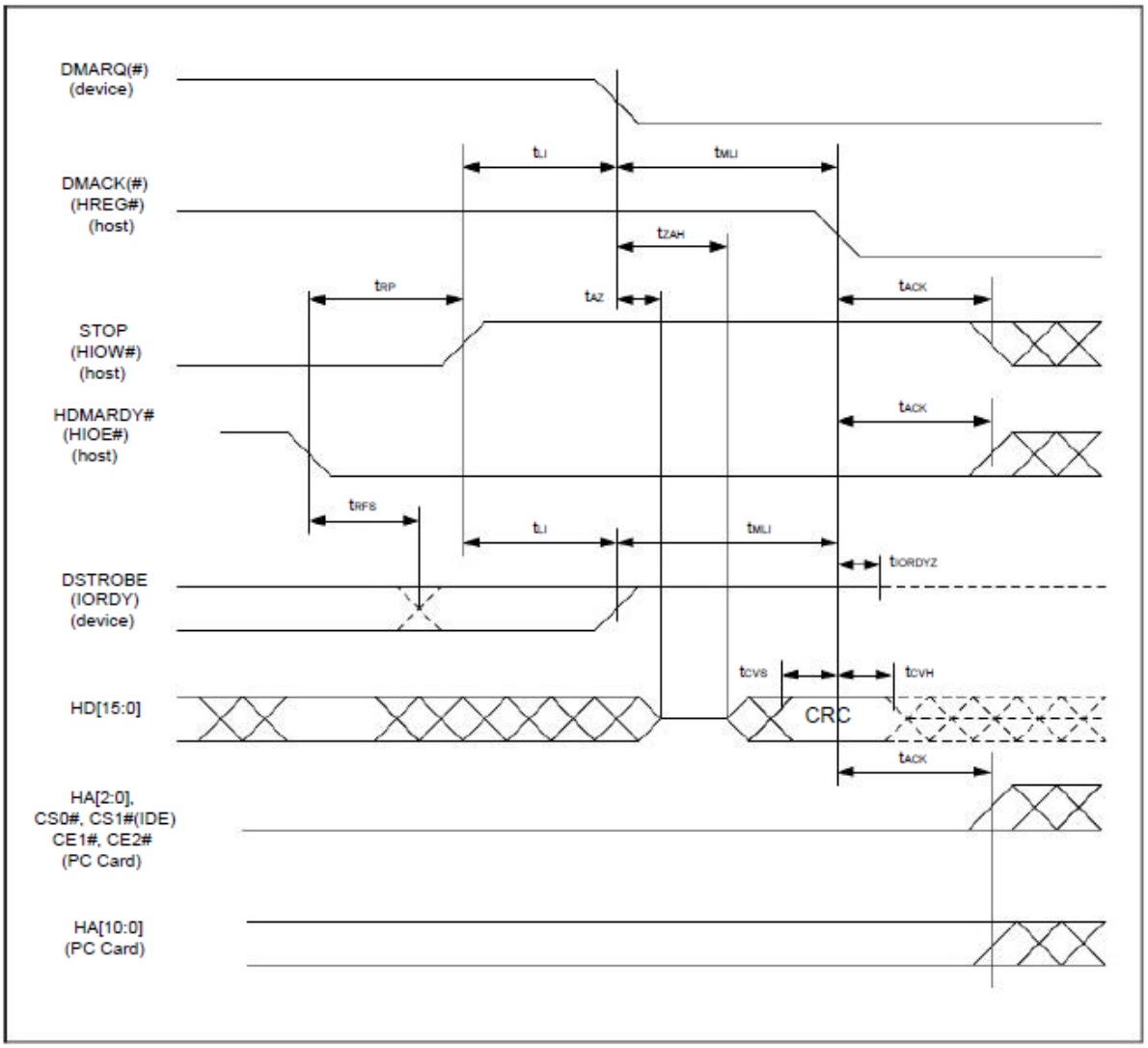
6.1.10 Ultra DMA Data-In Burst Host Pause Timing



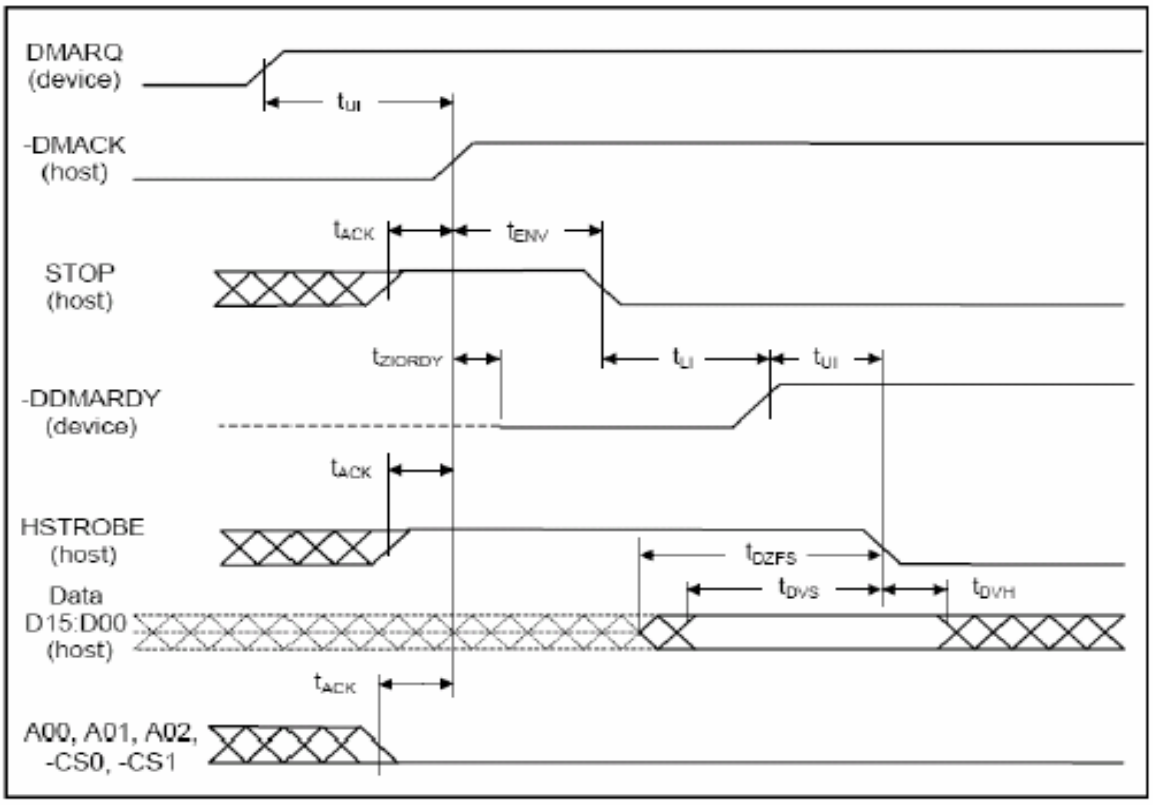
6.1.11 Ultra DMA Data-In Burst Device Termination Timing



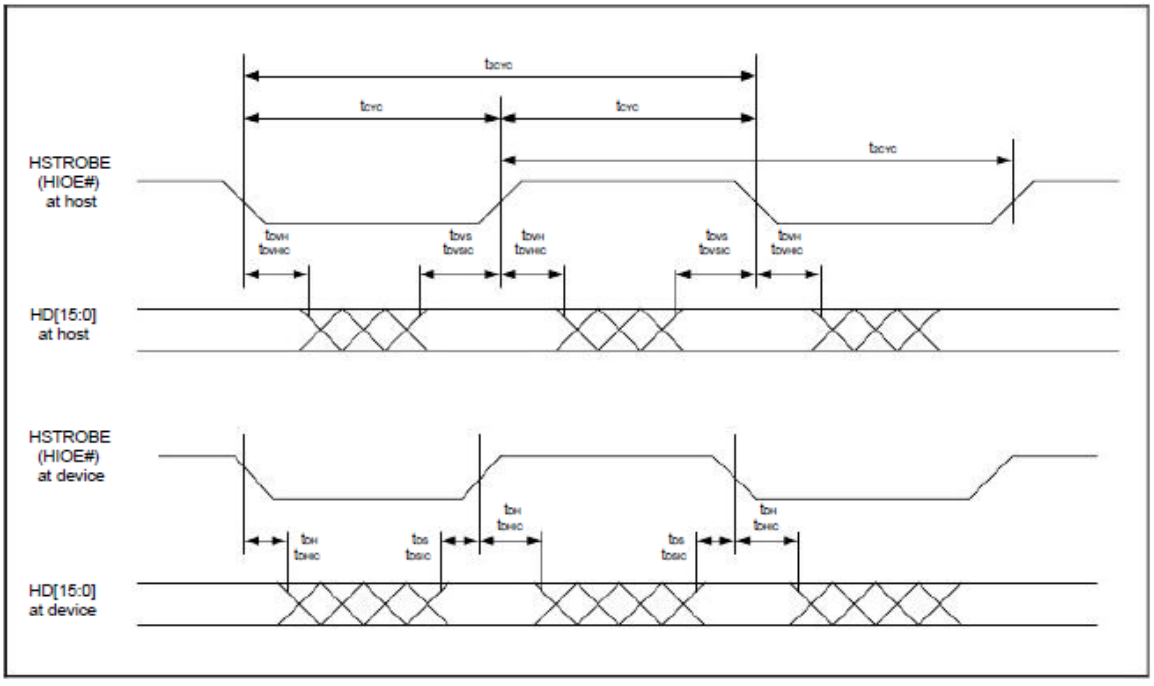
6.1.12 Ultra DMA Data-In Burst Host Termination Timing



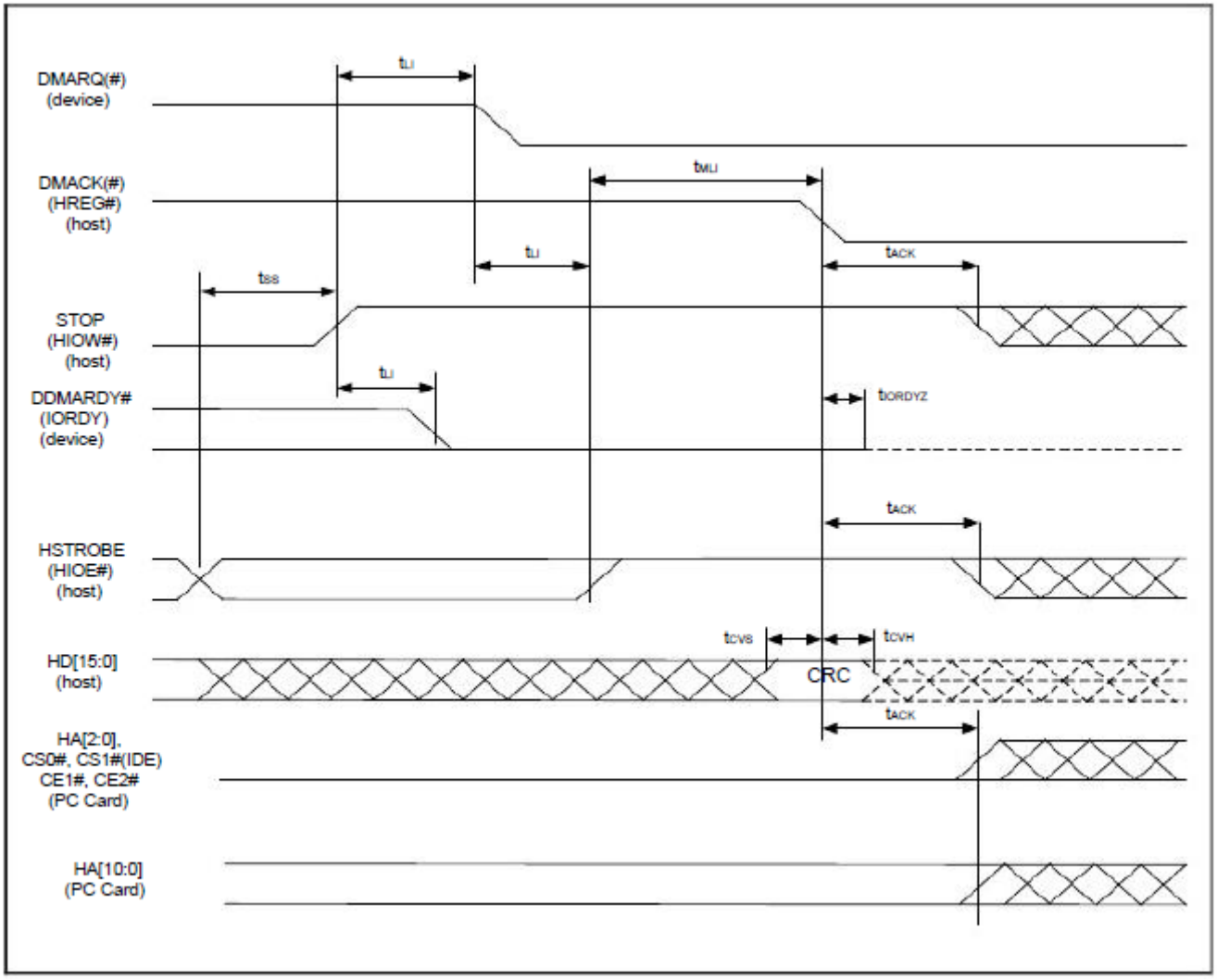
6.1.13 Ultra DMA Data-Out Burst Host Initiation Timing



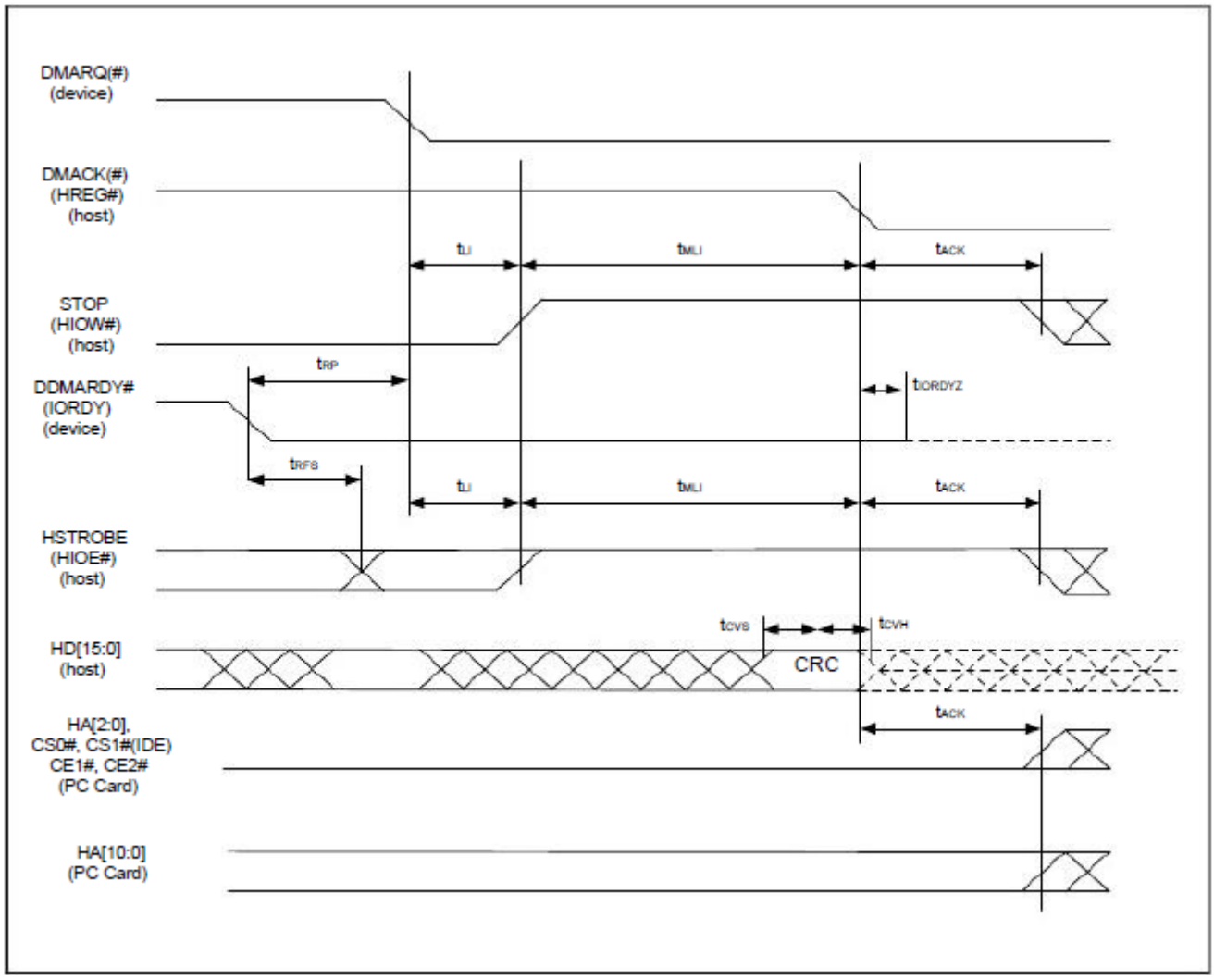
6.1.14 Sustained Ultra DMA Data-Out Burst Timing



6.1.15 Ultra DMA Data-Out Burst Host Termination Timing



6.1.16 Ultra DMA Data-Out Burst Device Termination Timing



7. Specification and Features

7.1 Physical Specification

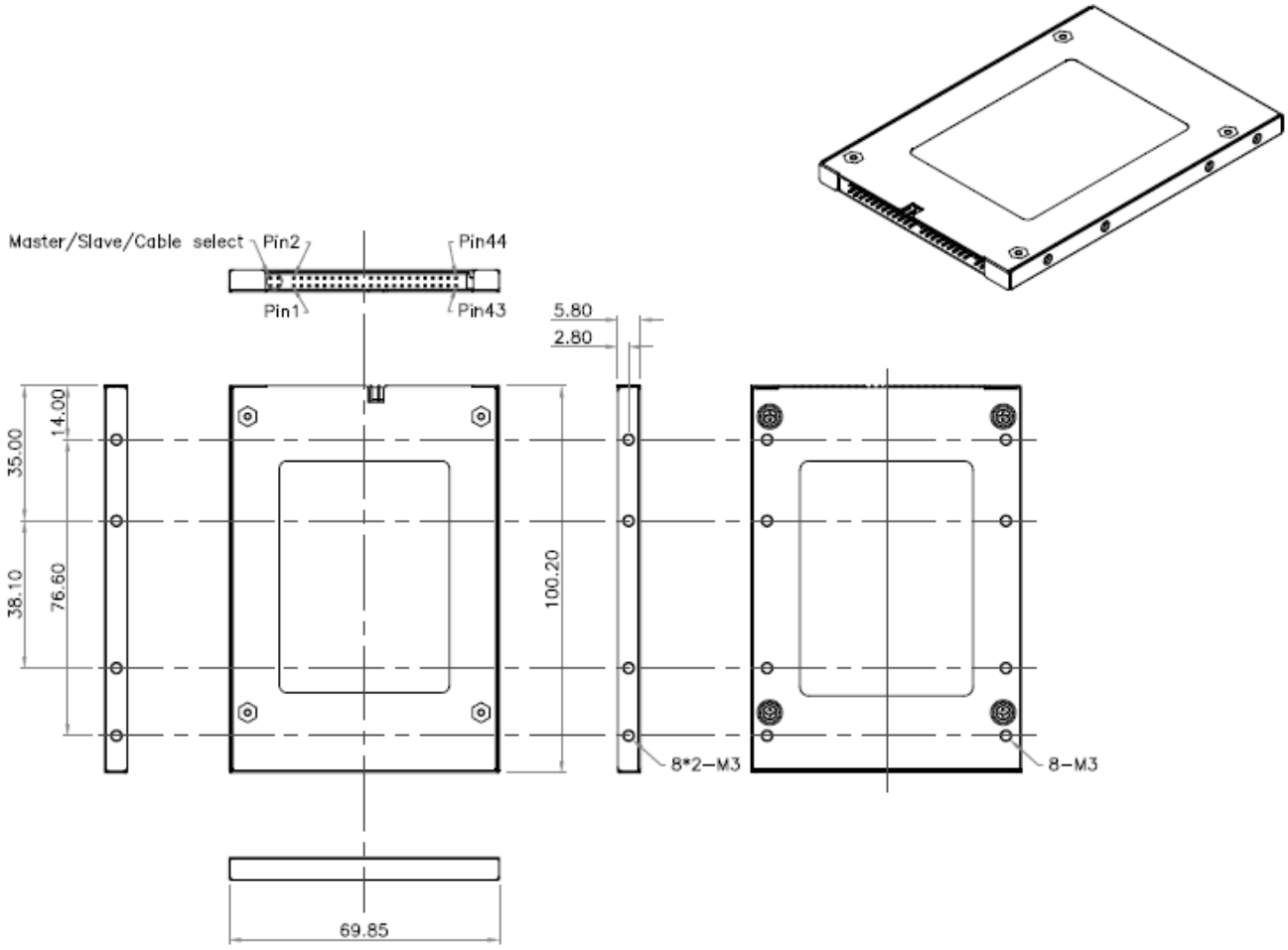


Figure 1: Mechanical Dimensions of 2.5" Lynx IDE SSD (H = 5.8mm)

8. Pin Assignment

8.1 Pin Type

Pin Num.	Signal Name	Pin Type	Pin Num.	Signal Name	Pin Type
A	GND	Ground	B	NSCEL	I
C	#Slave	I	D	NSCEL	I
E	Key	Cut Pin	F	Key	Cut Pin
1	#Reset	I	2	GND	Ground
3	Data 7	I/O	4	Data 8	I/O
5	Data 6	I/O	6	Data 9	I/O
7	Data 5	I/O	8	Data 10	I/O
9	Data 4	I/O	10	Data 11	I/O
11	Data 3	I/O	12	Data 12	I/O
13	Data 2	I/O	14	Data 13	I/O
15	Data 1	I/O	16	Data 14	I/O
17	Data 0	I/O	18	Data 15	I/O
19	GND	Ground	20	Key	Cut Pin
21	DMARQ	O	22	GND	Ground
23	#IOW	I	24	GND	Ground
25	#IOR	I	26	GND	Ground
27	IORDY	I	28	CSEL	I
29	DMACK	I	30	GND	Ground
31	IRQ	O	32	#IOCS16	O
33	A1	I	34	#PDIAG	I/O
35	A0	I	36	A2	I
37	#CS0	I	38	#CS1	I
39	#DASP	I/O	40	GND	
41	Vcc	Supply Voltage	42	Vcc	Supply Voltage
43	GND	Ground	44	TYPE	

8.2 Interface Signals Description

Signal Name	Pin	I/O	Description
#SLAVE	A,C	I	SLAVE Pins A and C are pulled-up input pins that are shorted together internally. (Pins B and D are ground.) These pins are used to configure the SSDdrive as Slave device. When all pins A, B, C and D are grounded, the SSDdrive is also configured as a Slave device. If both pins A and B remain open, the SSDdrive is configured as a Master or as the only drive in a single drive system.

#RESET	1	I	HOST RESET Reset signal from the host that is active on power up and inactive thereafter.
Data (15-0)	3 - 18	I/O	HOST DATA15-0 These 16 lines carry the Data between the controller and the host. The low 8 lines transfer commands, status, and ECC information between the host and the controller.
DMARQ	21	O	DMA REQUEST When ready to transfer data to or from the host, this signal used for DMA data transfers between host and device, shall be asserted by the device.
#IOW	23	I	I/O WRITE This strobe pulse is used to clock data or commands on the host data bus into the controller. The clocking will occur on the negative to positive edge of the signal (trailing edge).
#IOR	25	I	I/O READ This is a read strobe generated by the host. This signal gates data or status on the host bus and strobes the data from the controller into the host on the low to high transition (trailing edge).
IORDY	27	I	I/O READY This signal is negated to extend the host transfer cycle of any host register access (Read or Write) when the device is not ready to respond to a data transfer request.
Vcc	41,42	--	+5 V POWER
Signal Name	**Pin**	**I/O**	**Description**
CSEL	28	I	CABLE SELECT When grounded, the device is configured as a Master. When opened, this device is configured as a Slave.
DMACK	29	I	DMA ACKNOWLEDGE This signal shall respond to DMARQ by the host to initiate DMA transfers.
IRQ	31	O	INTERRUPT REQUEST This is an interrupt request from the controller to the host, asking for service. The output of this signal is tri-stated when the interrupt are disabled by the host.
#IOCS16	32	O	I/O SELECT 16 This open drain output is asserted low to indicate to the host the current cycle is a 16-bit word data transfer.
#PDIAG	34	I/O	PASS DIAGNOSTIC After an Execute Diagnostic command to indicate to the master it has passed its diagnostics, this bi-directional open drain signal is asserted by the slave.

A (2-0)	33,35,36	I	HOST ADDRESS 2-0 These address lines are used to select the registers within the controller task file.
#CS0	37	I	HOST CHIP SELECT 0 A chip select signal used to select the controller task file.
#CS1	38	I	HOST CHIP SELECT 1 A chip select signal that is used to select the control and diagnostic register.
#DASP	39	I/O	DISK ACTIVE/SLAVE PRESENT This open drain output signal is asserted low any time the drive is active. In a master/slave configuration, the slave uses it to inform the master of its present.
NC	E,F,20	-	These pins are reserved for the connector keys.
GND	A,D,2,19,22, 24,26,30,40,43	--	GROUND

8.3 The Jumper Setting of Lynx IDE SSD

The Lynx IDE SSD can be configured as Primary (Master), Secondary (Slave) and Cable Select mode.

- **Cable Select mode**: If pin A and B are jumped, the drive is installed as the Cable Select drive.
- **Primary (Master) mode**: If pin C and D are jumped, the drive is installed as the Primary (Master) drive.
- **Secondary (Slave) mode**: Either pin AC or none of the pins should be grounded, the drive is Installed as the Secondary (Slave) drive.

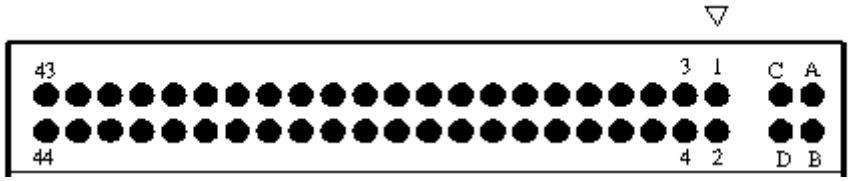
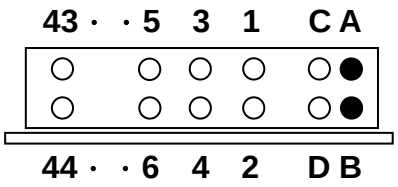


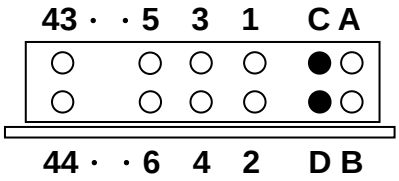
Figure 3: The Connector of Lynx IDE SSD

Cable Select



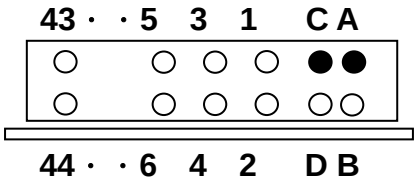
If pin A and B are jumped, the drive is configured as Cable Select drive

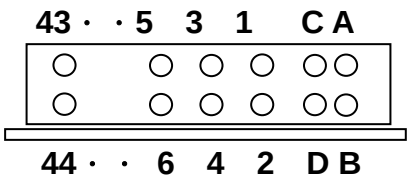
Primary (Master)



If pin C and D are jumped, the drive is configured as Primary (Master) drive

Secondary (Slave)





If all pins A, B, C, and D are open, or pin A and C are jumped, the drive is configured as Secondary (Slave) drive

9.ATA Specific Register Definitions

As we described the adapter provides several kinds of addressing modes, Memory mode, I/O mode, and True IDE mode. Below are described the procedures access for accessing each mode the Task File registers.

9.1 True IDE Mode

#CS0	#CS1	DA2	DA1	DA0	#IORD = "0"	#IOWR = "0"
1	1	X	X	X	Hi-Z	Not Used
1	0	0	X	X	Hi-Z	Not Used
1	0	1	0	X	Hi-Z	Not Used
0	0	X	X	X	Invalid	Invalid
1	0	1	1	0	Alternate Status	Device Control
1	0	1	1	1	Device Address	Not Used
0	1	0	0	0	Data	Data
0	1	0	0	1	Error	Feature
0	1	0	1	0	Sector Count	Sector Count
0	1	0	1	1	Sector Number	Sector Number
0	1	1	0	0	Cylinder Low	Cylinder Low
0	1	1	0	1	Cylinder High	Cylinder High
0	1	1	1	0	Drive/Head	Drive/Head
0	1	1	1	1	Status	Command

9.2 ATA Registers

9.2.1 Data Register

The Data register is a 16-bit register used to transfer data blocks between the ATA data buffer and the host. In addition, the Format Track command uses this register to transfer the sector-information. Setting this mode requires calling the Set Features command.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
D7	D6	D5	D4	D3	D2	D1	D0

bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8
D15	D14	D13	D12	D11	D10	D9	D8

9.2.2 Error Register

The Error Register contains additional information about the source of an error. The information in the register is only valid when an error is indicated in ERR-bit (bit-0 = 1) of the Status Register. This register is valid when the BSY bit in Status register and Alternate status register are set to “0”(Ready).

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
BBK	UNC	MC[0]	IDNF	MCR[0]	ABRT	T0NF[0]	AMNF

BBK	Bad Block mark detected in the requested sector ID field - Not supported
UNC	Non-Correctable data error encountered
MC[0]	Removable media access ability has changed - not supported (is 0)
IDNF	Requested sector ID-field Not Found
MCR[0]	Media Change Request indicates that the removable-media drive's latch has changed, indicating that the user wishes to remove the media - not supported (is 0)
ABRT	Drive status error or Aborted invalid command
T0NF[0]	Track 0 Not Found during a Recalibrate command - Not supported
AMNF	Address Mark Not Found after finding the correct ID field - Not supported

9.2.3 Feature Register

This register enables drive-specific features. See the Set Features or Get/Set Features command descriptions.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
Feature byte							

9.2.4 Sector Count Register

The Sector Count Register contains the number of data sectors requested to be transferred during a read or write operation between the host and the adapter. A zero register value specifies 256 sectors. The command was successful if this register is zero at command completion. If the request is not completed, the register contains the number of sectors left to be transferred.

This register’s initial value is “01H”

Some commands (e.g. Initialize Drive Parameters or Format Track) may redefine the register's contents.)

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
Sector count byte							

9.2.5 Sector Number Register

In the CHS (Cylinder, Head, Sector) mode, the Sector Number Register contains the subsequent command's starting sector number, which can be from 1 to the maximum number of sectors per track. In LBA (logical block address) mode, this register contains LBA bits 0-7, which are updated at command completion. See the command descriptions for register contents at command completion (whether successful or unsuccessful).

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
SN7	SN6	SN5	SN4	SN3	SN2	SN1	SN0
LBA7	LBA6	LBA5	LBA4	LBA3	LBA2	LBA1	LBA0
SN0 – SN7		Sector number byte (8-bits)					
LBA0 – LBA7		LBA bits 0 to 7					

9.2.6 Cylinder Low Register

In the CHS mode, the Cylinder Low Register contains the cylinder number low-8 bits and reflects their status at command completion. In LBA mode, this register contains LBA bits 8-15 and reflects their status at command completion.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
CL7	CL6	CL5	CL4	CL3	CL2	CL1	CL0
LBA15	LBA14	LBA13	LBA12	LBA11	LBA10	LBA9	LBA8
CL0 – CL7		Cylinder Low byte (8-bits)					
LBA8 – LBA15		LBA bits 8 to 15					

9.2.7 Cylinder High Register

In the CHS mode, the Cylinder High Register contains the cylinder numbers high-8 bits and reflects their status at command completion. In LBA mode, this register contains LBA bits 16-23 and reflects their status at command completion.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
LBA23	LBA22	LBA21	LBA20	LBA19	LBA18	LBA17	LBA16
CH0 – CH7		Cylinder High byte (8-bits)					
LBA16 – LBA23		LBA bits 16 to 23					

9.2.8 Drive Head Register

The Drive Head Register is used to select the drive and head (heads minus 1, when executing Initialize Drive Parameters command). It is also used to select the LBA addressing instead of the CHS addressing.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
1	LBA	1	DRV	HS3	HS2	HS1	HS0
HS0-HS3/		Head number.					
DRV		Drive select number. When DRV=0, the master drive is selected.					
		When DRV=1, the Slave drive is selected.					
LBA24-LBA27		MSB of the LBA addressing.					
LBA		Address mode select. 0 = CHS (Cylinder, Head, Sector) mode. 1 = LBA (Logical Block Address) mode. Logical Block address interrupted as follows: LBA07-LBA00 :Sector Number Register D7-D0 LBA15-LBA08:Cylinder Low Register D7-D0 LBA23-LBA16:Cylinder High Register D7-D0 LBA27-LBA24:Drive/Head Register HS3-HS0					

9.2.9 Status Register

This register contains the adapter status. The contents of this register are updated to reflect the current state of the adapter and the progress of any command being executed by the adapter. When the BSY bit is equal to zero, the other bits in this register are valid. When the BSY bit is equal to one, the other bits in this register are not valid. When the register is read, the interrupt (#IREQ pin) is cleared.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
BSY	DRDY	DWF	DSC	DRQ	CORR	0	ERR
ERR		When set, indicates that an error has occurred during the previous					

	command execution. The bits in the Error Register indicate the cause.
IDX	Index is not used – always set to Zero.
CORR	Indicates that a data error was corrected; transfer is not terminated.
DRQ	Data Request. When set, indicates that the adapter is ready to transfer a word or byte of data between the host and the adapter.
DSC	Drive Seek Complete. When set, indicates that the requested sector was found.
DWF	Drive Write Fault status. When set, indicates that an error has occurred during write.
DRDY	Indicates whether the adapter is capable of performing drive operations (commands). This bit is cleared at power up and remains cleared until the drive is ready to accept a command. On error, DRDY changes only after the host reads the Status register.
BSY	This signal is set during the time the adapter accesses the command buffer or the registers. During this time the host is locked out from accessing the command register and buffer. As long as this bit is set no bits in the register are valid.

9.2.10 Alternate Status Register

The Alternate Status Register contains command block status information (see Status register). Unlike the Status register, reading this register does not acknowledge or clear an interrupt.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
BSY	DRDY	DWF	DSC	DRQ	CORR	0	ERR

9.2.11 Device Control Register

The Device Control Register is used to control the drive interrupt request and issue an ATA soft reset to the drive.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
---	---	---	---	1	SRST	#IEN	0
#IEN		INTERRUPT ENABLE: When set (0), it enables interrupts to the host (using the #IREQ tri-state pin). When inactive (1) or drive is not selected, it disables all pending interrupts (#IREQ in high-Z).					

	This bit is ignored in Memory mode.
SRST	SOFT RESET: When set, forces the ATA to perform an AT disk control soft reset operation.

9.2.12 Drive Address Register

This register reflects the drive and its heads. This register is provides for compatibility with the AT disk interface. It's recommended that this register is not mapped into this host's I/O space because of potential conflicts on bit7.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
High-Z	#WTG	#HS3	#HS2	#HS1	#HS0	#DS1	#DS0
#DS0		When set (0), it indicates that drive 0 is active and selected.					
#DS1		When set (0), it indicates that drive 1 is active and selected.					
#HS0 - #HS3		Negation of the head number in the Drive/Head Register.					
#WTG		When set (0), it indicates that a write operation is in progress, otherwise it is inactive (1) - not supported.					

Note:

Addressing Mode Descriptions - The adapter, on a command by command basis, can operate in either CHS or LBA addressing modes. Identify Drive Information tells the host whether the drive supports LBA mode. The host selects LBA mode via the Drive/Head Register. Sector number, Cylinder Low, Cylinder High, and Drive/Head Register bits HS3=0 contain the zero-based LBA. The drive's sectors are linearly mapped with: LBA = 0 => Cylinder 0, head 0, sector 1. Regardless of the translation mode, a sector LBA address does not change. LBA = (Cylinder * no of heads + heads) * (sectors/track) + (Sector - 1).