LINEAR FLASH MEMORY CARD

SERIES-I (Fx1xxx)
Product Specification

Preliminary

Documentation History

Version	Description	Date	Written By
1.0	New Issue	Aug. 2006	Greg Liu

Contents

Preliminary

Features

★ PCMCIA / JEIDA standard
★ Series 1 Flash memory card
★ Memory Capacity :256K~2 Mega bytes
★ Byte (x8) / word (x16) data bus selectable
★ Fast access time : 250ns (maximum)
★ Optional attribute memory : 8K byte E^2PROM
★ Read voltage : 5V , write/erase voltage : 12V
★ 128K (or 256K) byte per memory segment structure
★ 10000 write/erase cycles
★ 1 second typical per 128K-byte segment
★ 10 us typical random writes to erased byte
★ Command register architecture
★ Built-in write protect switch
★ Credit card size : 54.0 x 85.6 x 3.3 (mm)

General Description

C-ONE's high performance FLASH memory cards conform to the PCMCIA / JEIDA international standard and consist of multiple Catalyst's 28F010 or 28F020(or compatible) FLASH memory devices and decoder IC mounted on a very thin printed circuit board using surface mounting technology.

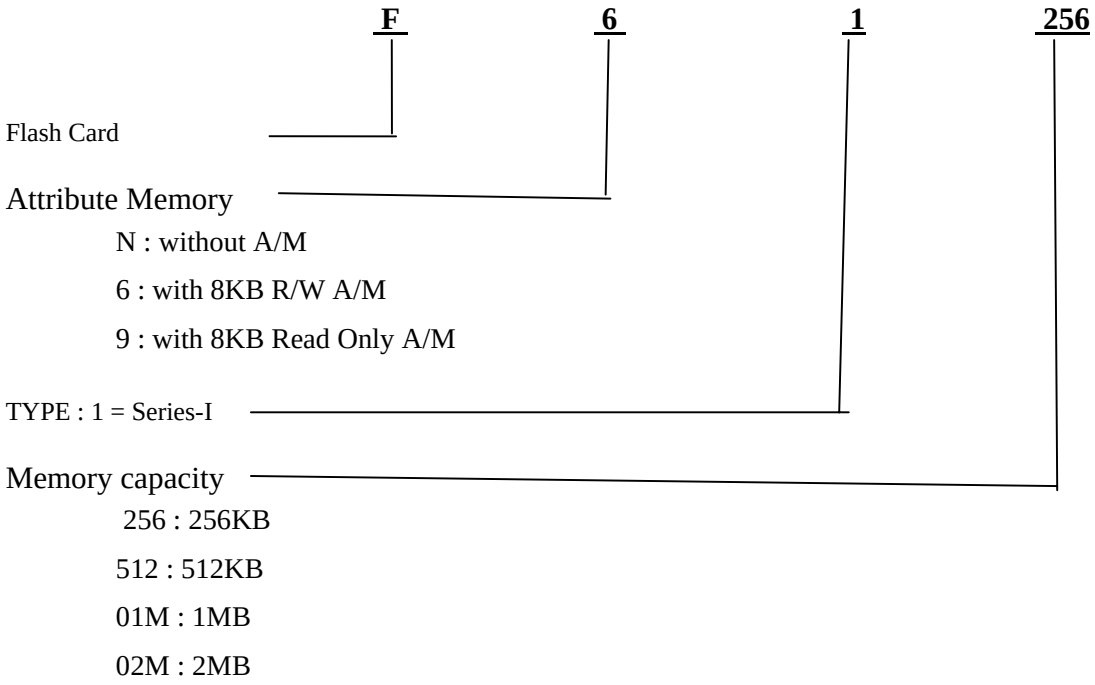
Each card is organized as an array of individual memory segments. Each segment is 128K (or 256K) bytes in size. With this segment structure , the electrical segment-erasure capability gives the designer the flexibility to selectively rewrite segments of data while saving other segments for infrequently updated look-up tables.

This series Flash memory cards offer portable , reprogrammable and nonvolatile solid-state storage media and can be used for flexible integration into various system platforms with PCMCIA/JEIDA interface. With the extra and optional 8K bytes "attribute memory" space , the Card Information Structure (CIS) can be written into it by OEM with standard format or customized requirements.

Catalyst 28F010 : (31B4) the manufacturer code of 31H and the device code of B4H.
Catalyst 28F020 : (31BD) the manufacturer code of 31H and the device code of BDH.

INTEL 28F010 : (89B4) the manufacturer code of 89H and the device code of B4H.
INTEL 28F020 : (89BD) the manufacturer code of 89H and the device code of BDH.

Product Number Definition



Note : A/M means attribute memory.

Product List

Item No.	Part Number				Memory Capacity		Attribute Memory
					Bytes	Words	
1	CAT28F010*2	E28F010*2			256KB	128KB	8KB E^2PROM
2	CAT28F010*4	E28F010*4	CAT28F020*2	E28F020*2	512KB	256KB	
3	CAT28F010*8	E28F010*8	CAT28F020*4	E28F020*4	1MB	512KB	
4			CAT28F020*8	E28F020*8	2MB	1MB	
5	CAT28F010*2	E28F010*2			256KB	128KB	None
6	CAT28F010*4	E28F010*4	CAT28F020*2	E28F020*2	512KB	256KB	
7	CAT28F010*8	E28F010*8	CAT28F020*4	E28F020*4	1MB	512KB	
8			CAT28F020*8	E28F020*8	2MB	1MB	

Table 1

Block Diagram

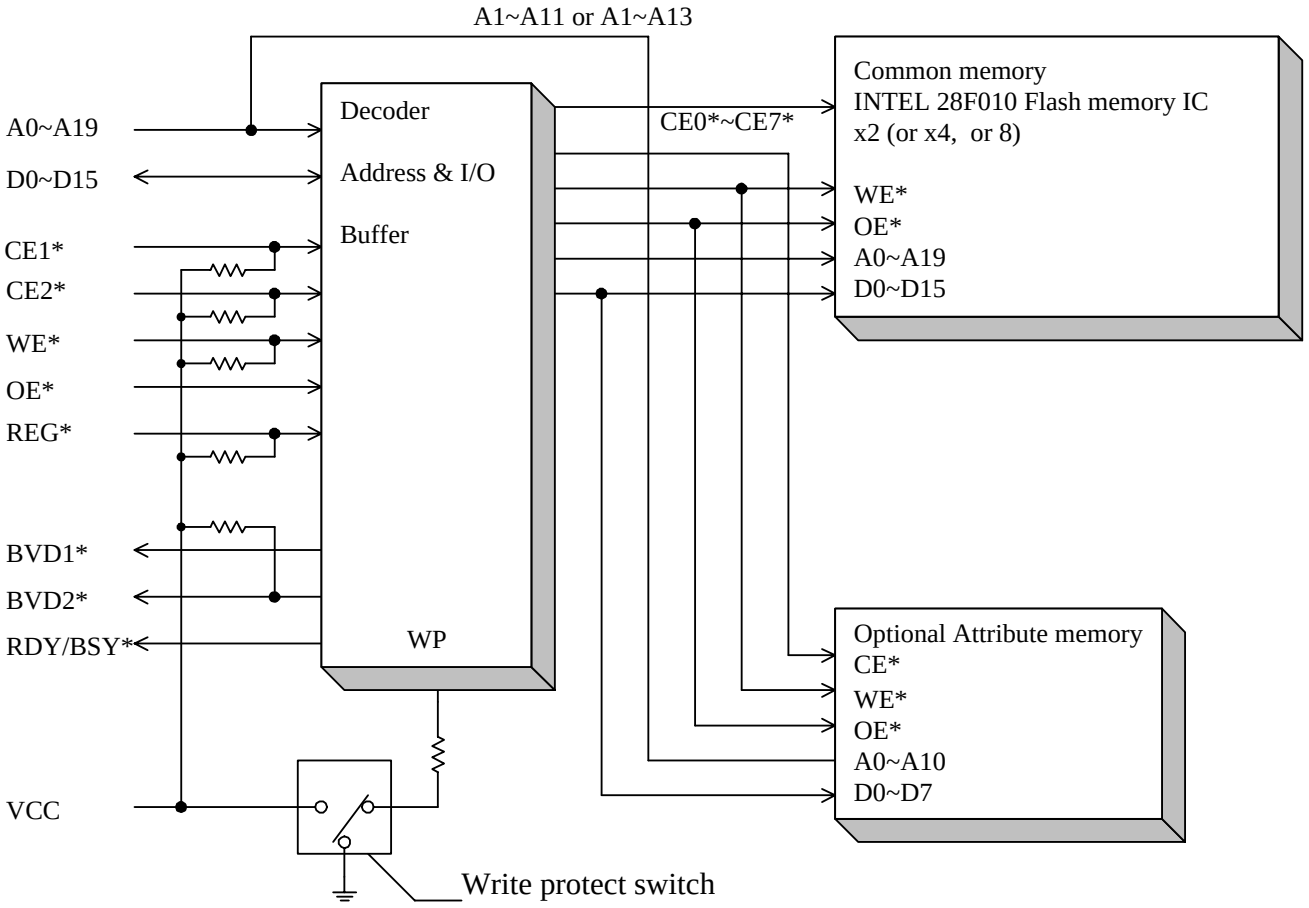


Figure 1

Pin Configuration (C1FLA01M54)

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Pin No.
VCC	BUSY*	WE*	A14	A13	A8	A9	A11	OE*	A10	CE1*	D7	D6	D5	D4	D3	GND	Pin Name
34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	Pin No.
GND	WP	D2	D1	D0	A0	A1	A2	A3	A4	A5	A6	A7	A12	A15	A16	VPP1	Pin Name
51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	Pin No.
VCC	NC	NC	A19	A18	A17	NC	NC	NC	CE2*	D15	D14	D13	D12	D11	CD1*	GND	Pin Name
68	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	Pin No.
GND	CD2*	D10	D9	D8	BVD1*	BVD2*	REG*	NC	NC	NC	NC	NC	NC	NC	NC	VPP2	Pin Name

Table 2

Note : * mean low active

C1FLA2565 series : A19,A18 = NC
C1FLA5125 series : A19 = NC
C1FLA25654~C1FLA01M54 series : A16 = BUSY* ; A61 = REG*
C1FLA25650~C1FLA01M50 series : A16 = NC ; A61 = NC

Pin Description

Symbol	Function	I/O
A0-A19	Addresses	I
D0-D15	Data Inputs/Outputs	I/O
CE1*/CE2*	Card Enable	I
OE*	Output Enable	I
WE*	Write Enable	I
REG*	Attribute Memory Enable	I
WP	Write-protect status Detect	O
BVD1*/BVD2*	Battery Voltage Detect	O
BUSY*	Ready/Busy status	O
CD1*/CD2*	Card Detect (tied to GND internally)	O
VCC	+5 Volt Power Supply	-
VPP1/VPP2	Write (programming) Power Supply	-
GND	Ground	-
NC	No Connection	-

Table 3

Pin Location

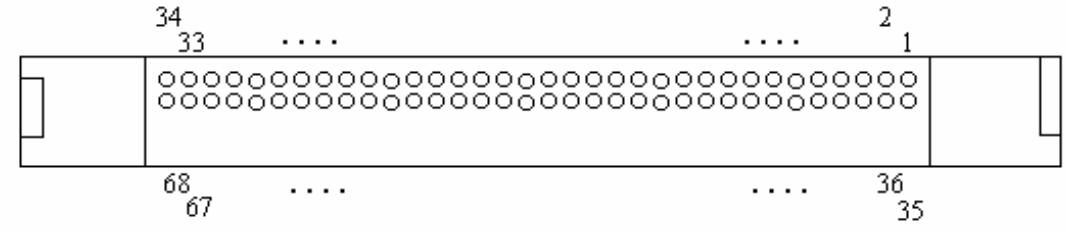


Figure 2 Bottom View (Connector Side)

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
V_{CC} Supply Voltage	V_{CC}	4.5	5.5	V
V_{PP} Supply Voltage (read)	V_{PPL}	0	6.5	V
V_{PP} Supply Voltage (erase/write)	V_{PPH}	11.4	12.6	V
Input High Voltage	V_{IH}	2.4	VCC + 0.3	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Operating Temperature	T_{OPR}	0	70	° C

Table 4

Absolute Maximum Ratings *

Parameter	Symbol	Value	Unit
V_{CC} Supply Voltage	V_{CC}	- 0.5 to + 6.0	V
V_{PP} Supply Voltage (read)	V_{PPL}	- 2.0 to + 7.0	V
V_{PP} Supply Voltage (erase/write)	V_{PPH}	- 2.0 to + 14.0	V
Input Voltage	V_{IN}	- 0.5 to V_{CC}+0.3(6V max.)	V
Output Voltage	V_{OUT}	- 0.5 to + 6.0	V
Operating Temperature	T_{OPR}	0 to + 70	° C
Storage Temperature	T_{STR}	- 30 to + 70	° C
Relative Humidity (non-condensing)	H_{UM}	95(maximum)	%

Table 5

***Comments**

Stress above those listed under " Absolute Maximum Ratings " may cause permanent damage to the products. These are stress rating only. Functional operation of these products at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Common Memory Function Table

Function		REG*	CE2*	CE1*	A0	OE*	WE*	V_{PP2}	V_{PP1}	D15 - D8	D7 - D0
Read-Only	Byte Read	H	H	L	L	L	H	V_{PPL}	V_{PPL}	High-Z	Even Byte Data Out
		H	H	L	H	L	H	V_{PPL}	V_{PPL}	High-Z	Odd Byte Data Out
	Odd Byte Only Read	H	L	H	X	L	H	V_{PPL}	V_{PPL}	Odd Byte Data Out	High-Z
	Word Read	H	L	L	X	L	H	V_{PPL}	V_{PPL}	Odd Byte Data Out	Even Byte Data Out
	Output Disable	X	X	X	X	H	H	V_{PPL}	V_{PPL}	High-Z	High-Z
	Standby	X	H	H	X	X	X	V_{PPL}	V_{PPL}	High-Z	High-Z
Read/Write	Byte Read	H	H	L	L	L	H	V_{PPX}	V_{PPH}	High-Z	Even Byte Data Out
		H	H	L	H	L	H	V_{PPH}	V_{PPX}	High-Z	Odd Byte Data Out
	Odd Byte Only Read	H	L	H	X	L	H	V_{PPH}	V_{PPX}	Odd Byte Data Out	High-Z
	Word Read	H	L	L	X	L	H	V_{PPH}	V_{PPH}	Odd Byte Data Out	Even Byte Data Out
	Byte Write	H	H	L	L	H	L	V_{PPX}	V_{PPH}	X	Even Byte Data In
		H	H	L	H	H	L	V_{PPH}	V_{PPX}	X	Odd Byte Data In
	Odd Byte Only Write	H	L	H	X	H	L	V_{PPH}	V_{PPX}	Odd Byte Data In	X
	Word Write	H	L	L	X	H	L	V_{PPH}	V_{PPH}	Odd Byte Data In	Even Byte Data In
	Standby	X	H	H	X	X	X	V_{PPH}	V_{PPH}	High-Z	High-Z
	Output Disable	X	X	X	X	H	L	V_{PPH}	V_{PPH}	High-Z	High-Z

Table 6

Attribute Memory Function Table

Function	REG*	CE2*	CE1*	A0	OE*	WE*	V_{PP2}	V_{PP1}	D15 - D8	D7 - D0
Standby	X	H	H	X	X	X	V_{PPL}	V_{PPL}	High-Z	High-Z
Byte Read	L	H	L	L	L	H	V_{PPL}	V_{PPL}	High-Z	Even Byte Data Out
	L	H	L	H	L	H	V_{PPL}	V_{PPL}	High-Z	Invalid Data Out
Word Read	L	L	L	X	L	H	V_{PPL}	V_{PPL}	Invalid Data Out	Even Byte Data Out
Odd Byte Only Read	L	L	H	X	L	H	V_{PPL}	V_{PPL}	Invalid Data Out	High-Z
Byte Write	L	H	L	L	H	L	V_{PPL}	V_{PPL}	X	Even Byte Data In
	L	H	L	H	H	L	V_{PPL}	V_{PPL}	X	X
Word Write	L	L	L	X	H	L	V_{PPL}	V_{PPL}	X	Even Byte Data In
Odd Byte Only Write	L	L	H	X	H	L	V_{PPL}	V_{PPL}	X	X

Table 7

Notes :

1. Refer to DC Characteristics. When $V_{PP1/2} = V_{PPL}$ memory contents can be read but not written or erased.
2. L = V_{IL} ; H = V_{IH} ; X = don't care , can be either V_{IH} or V_{IL}.
3. $V_{PPX} = V_{PPH}$ or V_{PPL}.
4. With $V_{PPL1/2}$ at high voltage , the standby current equals $I_{CC} + I_{PP}$ (Standby).

Command Set Table

Command	Bus Cycles Req	First Bus Cycle				Second Bus Cycle				Notes
		Operation	Address	Data		Operation	Address	DAta		
				Byte Mode	Word Mode			Byte Mode	Word Mode	
Read Memory	1	Write	X	00H	0000H					
Read Intelligent ID Codes	3	Write	IA	90H	9090H	Read				4
Set-up Erase/Erase	2	Write	ZA	20H	2020H	Write	ZA	20H	2020H	5
Erase Verify	2	Write	EA	A0H	A0A0H	Read	EA	EVD	EVD	5
Set-up Write/Write	2	Write	WA	40H	4040H	Write	WA	WD	WD	6
Write Verify	2	Write	WA	C0H	C0C0H	Read	WA	WVD	WVD	6
Reset	2	Write	X	FFH	FFFFH	Write	X	FFH	FFFFH	7

Table 8

Notes :

1. Bus operations are defined in Table 6.

2. IA = Identifier address : 00H for manufacture code , 01H for device code.

   EA = Address of memory location to be read during erase verify.

   WA = Address of memory location to be written.

   ZA = Address of 128K-Byte segments involved in erase operation.

   Address are latched on the falling edge of the Write Enable pulse.

3. ID = Data read from location IA during device identification.

Flash Memory	Manufacturer Code	Device Code
INTEL 28F010	89H	B4H
AMD 28F010	01H	A7H
MITSUBISHI 28F101	1CH	D0H
T1 TMS28F010B	89H	B4H
T1 TMS28F020	89H	BDH

   EVD = Data read from location EA during erase verify.

   WD = Data to be written at location WA. Data is latched on the rising edge of Write Enable.

   WVD = Data read from location WA during write verify. WA is latched on the Write command.

4. Following the Read Inteligent ID command , two read operations access manufacturer and device codes.

5. Figure 5,8,9 illustrate the Erase Algorithm.

6. Figure 4,6,7 illustrate the Write Algorithm.

7. The second bus cycle must be followed by the desired command register write.

Command Definitions

When V_{PPL} is applied to the V_{PP} pin(s) , the contents of the segment Command Register(s) default to 00H , enabling read-only operations.

Placing V_{PPH} on the V_{PP} pin(s) enable(s) read / write operations. Segment operations are selected by writing specific data into the Command Register.

Read Command

While $V_{PP1/2}$ is high , for erasure and writing , segment memory contents can be accessed via the read command. The read operation is initiated by writing 00H (0000H for the word-wide configuration) into the segment Command Register(s). Microprocessor read cycles retrieve segment data. The accessed segment remains enabled for reads until the Command Register(s) contents are altered.

The default contents of each segment's register(s) upon $V_{PP1/2}$ power-up is 00H (0000H for word-wide). This default value ensures that no spurious alteration of memory card contents occurs during the $V_{PP1/2}$ power transition. Where the $V_{PP1/2}$ supply is left at V_{PPH} , the memory card powers-up and remains enabled for reads until the command Register contents of targeted segments are changed. Refer to the AC Read Characteristics and Waveforms for specific timing parameters.

Intelligent Identifier Command

Each segment of this series cards contains an intelligent Identifier to identify memory card device characteristics. The operation is initiated by writing 90H (9090H for word-wide) into the Command Register(s). Following the command write , a read cycle from address 0000H retrieves the manufacturer code 89H (8989H for word-wide). A read cycle from address 0002H returns the device code B4H (B4B4H for word-wide). To terminate the operation , it is necessary to write another valid command into the register(s).The above data are for INTEL 28F010 chips, for other chips, please refer to the table page 9.

Set-up Erase/Erase Commands

Set-up Erase is a command-only operation that stages the targeted segment(s) for electrical erasure of all bytes in the segment. The set-up erase operation is performed by writing 20H to the Command Register (2020H for word-wide).

To commence segment-erasure , the erase command (20H or 2020H) must again be written to the register(s). The erase operation begins with the rising edge of the Write-Enable pulse and terminates with the rising edge of the next Write-Enable pulse (i.e., Erase-Verify Command).

This two-step sequence of set-up followed by execution ensures that segment memory contents are not accidentally erased. Also , segment-erasure can only occur when high voltage is applied to the $V_{PP1/2}$ pins. In the absence of this high voltage , segment memory contents are protected against erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameterts.

Erase-Verify Command

The erase command erases all of the bytes of the segment in parallel. After each erase operation , all bytes in the segment must be individually verified. In byte-mode operations , segments are segregated by A0 in odd and even banks ; erase and erase verify operations must be done in complete passes of even-bytes-only then odd-bytes-only. See the Erase Algorithm for byte-wide mode. The erase verify operation is initiated by writing A0H (A0A0H for word-wide) into the Command Register(s). The address for the byte(s) to be verified must be supplied as it is latched on the falling edge of the Write Enable pulse. The register write terminates the erase operation with the rising edge of its Write Enable pulse.

The enabled segment applies an internally-generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are erased. Similarly , reading FFFFH from the addressed word indicates that all bits in the word are erased.

The erase-verify command must be written to the Command Register prior to each byte (word) verification to latch its address. The process continues for each byte (word) in the segment(s) until a byte (word) does not return FFH (FFFFH) data , or the last address is accessed.

In the case where the data read is not FFH (FFFFH) , another erase operation is performed. (Refer to Set-up Erase/Erase.) Verification then resumes from the address of the last-verified byte (word). Once all bytes (words) in the segment(s) have been verified , the erase step is complete. The accessed segment can now be written. At this point , the verify operation is terminated by writing a valid command (e.g., Write Set-up) to the Command Register. The Erase algorithms for byte-wide and word-wide configurations illustrate how commands and bus operations are combined to perform electrical erasure of this series cards. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Set-up Write/Write Commands

Set-up write is a command-only operation that stages the targeted segment for byte writing. Writing 40H (4040H) into the Command Register(s) performs the set-up operation.

Once the write set-up operation is performed , the next Write Enable pulse causes a transition to an active write operation. Addresses are internally latched on the falling edge of the Write Enable pulse. Data is internally latched on the rising edge of the Write Enable pulse. The rising edge of Write Enable also begins the write operation. The write operation terminates with the next rising edge of Write Enable , which is used to write the verify command. Refer to AC Write Characteristics and Waveforms for specific timing parameters.

Write Verify Command

This series cards are written on a byte-by-byte or word-by-word basis. Byte or word writing may occur sequentially or at random. Following each write operation , the byte or word just written must be verified.

The write-verify operation is initiated by writing C0H (C0C0H for word-wide) into the Command Register(s). The register write(s) terminate(s) the write operation with the rising edge of its Write Enable pulse. The write-verify operation stages the accessed segment(s) for verification of the byte or word last written. No new address information is latched. The segment(s) apply(ies) an internally-generated margin voltage to the byte or word. A microprocessor read cycle outputs the data. A successful comparison between the written byte or word and true data means that the byte or word is successfully written. The write operation then proceeds to the next desired byte or word location. The Write algorithms for byte-wide and word-wide configurations illustrate how commands are combined with bus operations to perform byte and word writes. Refer to AC Write Characteristics and Waveforms for specific timing parameters.

Reset Command

A reset command is provided as a means to safely abort the erase- or write-command sequences. Following either set-up command (erase or write) with two consecutive writes of FFH (FFFFH for word-wide) will safely abort the operation. Segment memory contents will not be altered. A valid command must then be written to place the accessed segment in the desired state.

Full Card Erase Flow

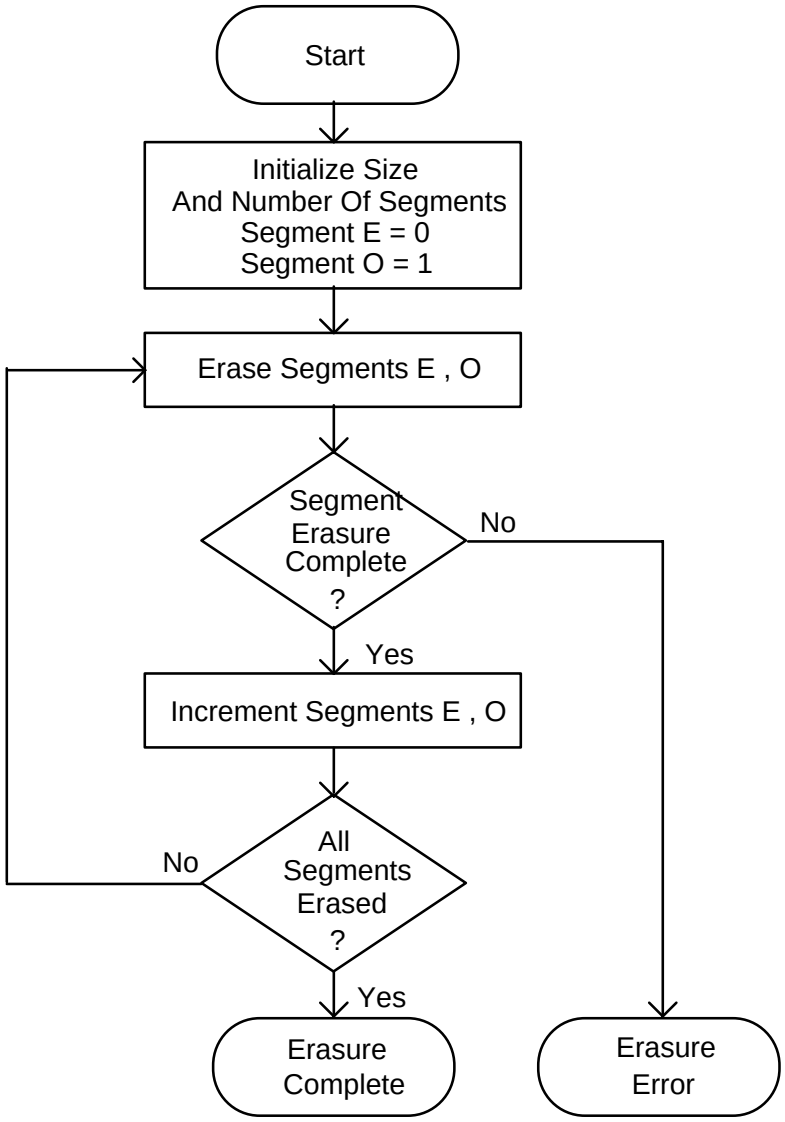
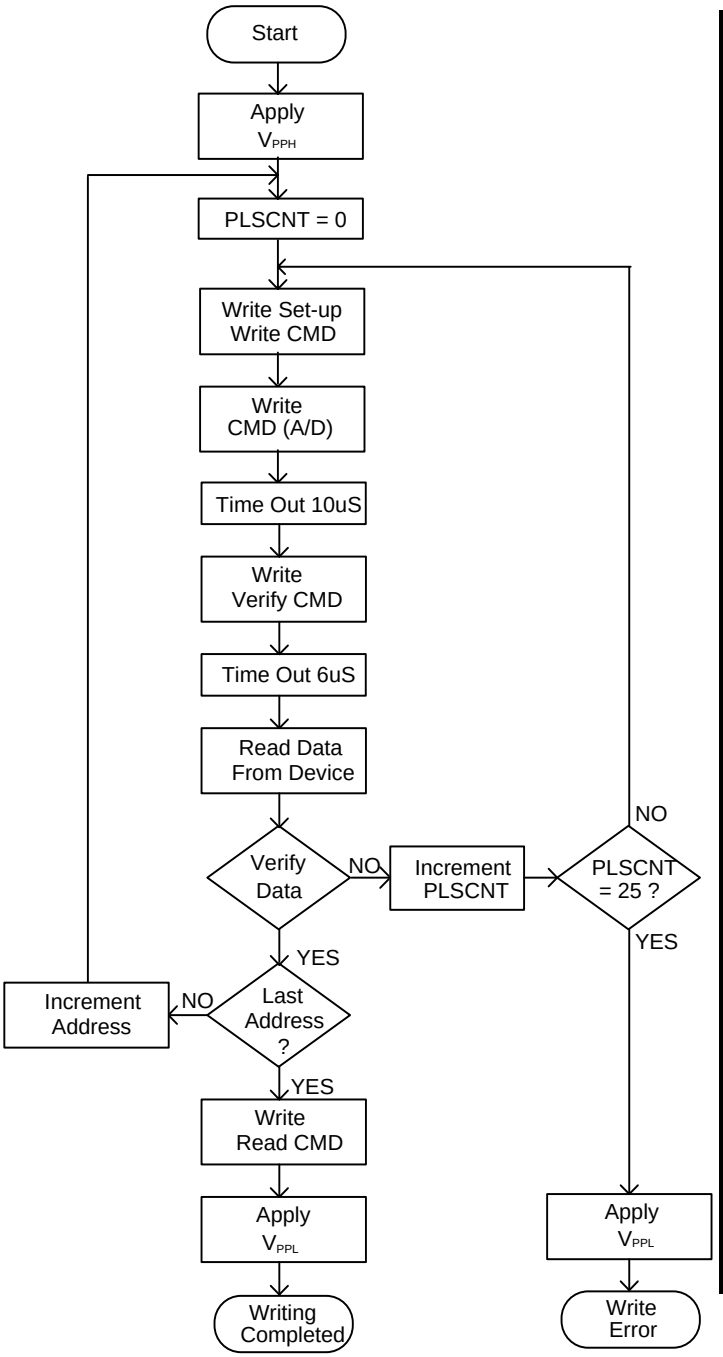


Figure 3

Notes : E = Even , O = Odd

Write Algorithm for Byte-wide Mode



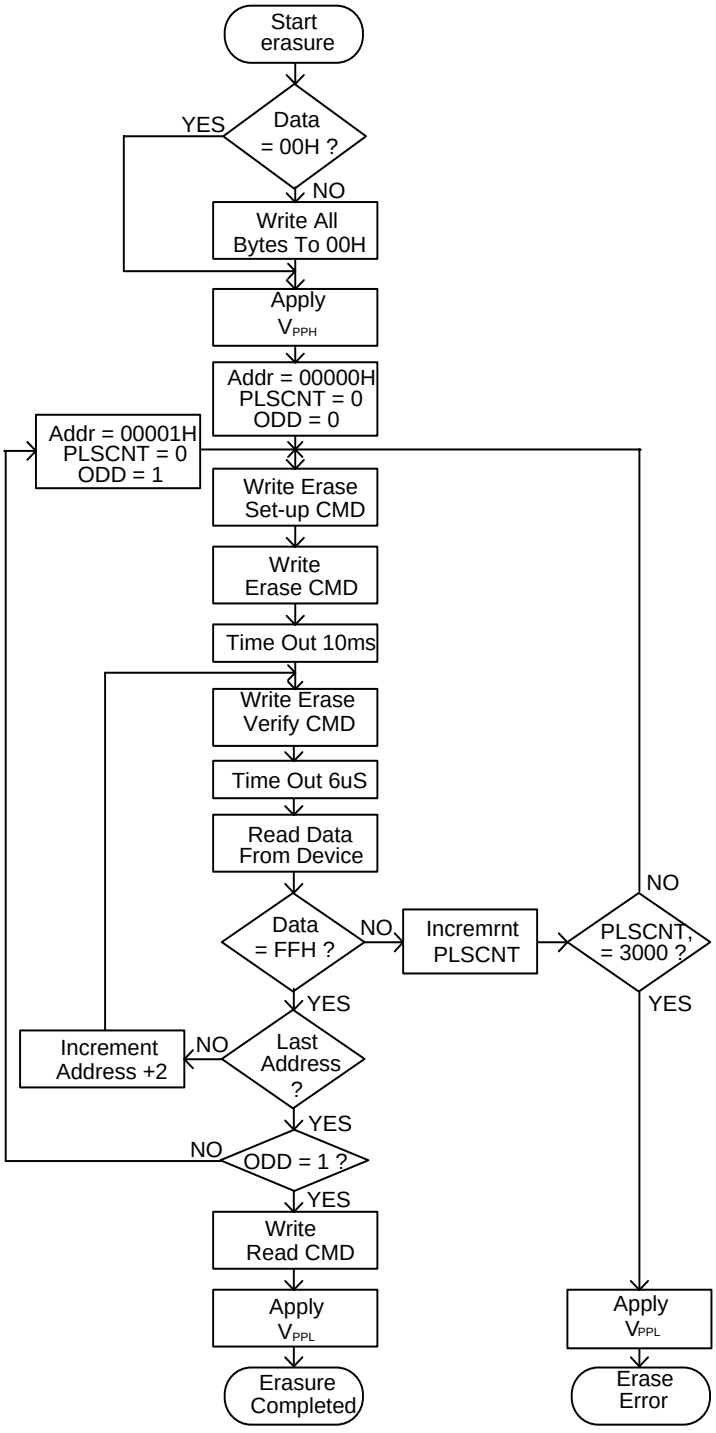
Bus Operation	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (=12.0V)
		Initialize pulse-count
Write	Set-up Write	Data=40H
Write	Write	Valid address/data
Standby		Duration of Write operation (t_{WHWH1})
Write	Write Verify	Data=C0H; Stops Write Operation
Standby		t_{WHGL}
Read		Read byte to verify Write Operation
Standby		Compare data output to data expected
Write	Read	Data=00H, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL}

Figure 4

Notes :

1. See DC Characteristics for the value of V_{PPH} and V_{PPL}.
2. Write Verify is only performed after a byte write operation. A final read/compare may be performed (optional) after the register is written with the Read command.

Erase Algorithm for Byte-Wide Mode



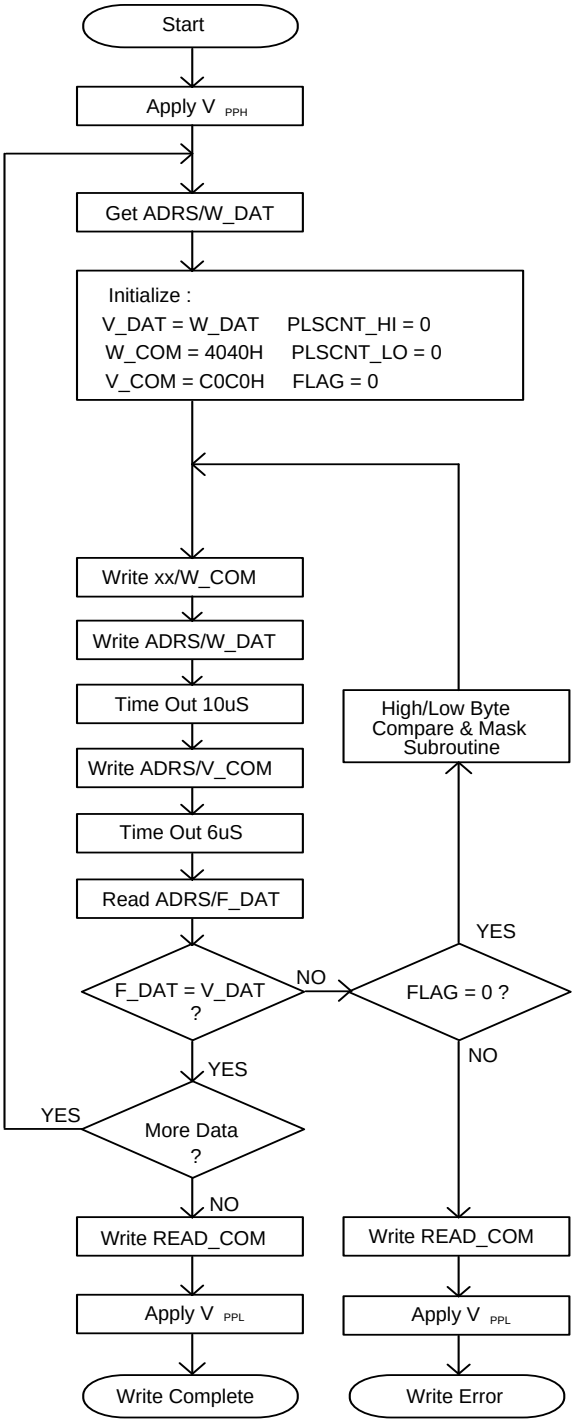
Bus Operation	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (=12.0V)
		Use Write Operation Algorithm
		Initialize even/odd Addresses, Erase Pulse Width, and Pulse Count
Write	Set-up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase operation (t_{WHWH2})
Write	Erase Verify	Addr = Byte to verify; Data = A0H; Stops Erase Operation
Standby		t_{WHGL}
Read		Read byte to verify erasure
Standby		Compare output to FFH increment pulse count
Write	Read	Data = 00H, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL}

Figure 5

Notes :1. See DC Characteristics for the value of V_{PPH} and V_{PPL}.

2. Erase Verify is only performed after chip erasure. A final read/compare may be performed (optional) after the register is written with the Read command.

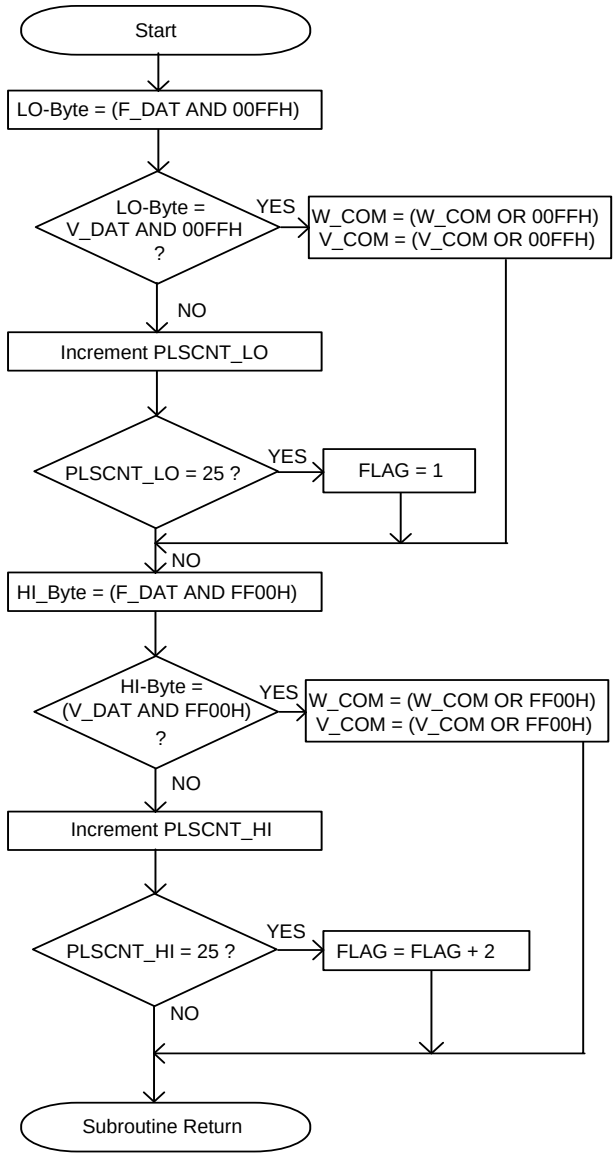
Write Algorithm for Word-wide Mode



Comments
Wait for V_{PP} ramp to V_{PPH}
ADRS = address to write W_DAT = data word to write
Initialize Data Word Variables: V_DAT = valid data W_COM = Write Command V_COM = Write Verify Command PLSCNT HI = HI Byte Pulse Counter PLSCNT LO = LO Byte Pulse Counter FLAG = Write Error Flag
Write Set-up Command xx = Address don't care Write
See Write Verify and Mask Subroutine. Write Verify Command
F_DAT = flash memory data Compare flash memory data to valid data (word compare). If not equal, check for Write Error flag. If Flag not set, compare High and Low Bytes in the Subroutine. Check buffer of I/O port for more data to write.
Reset device for read operation.
Turn off V_{PP}.

Figure 6

Write Verify and Mask Subroutine for Word-wide Mode

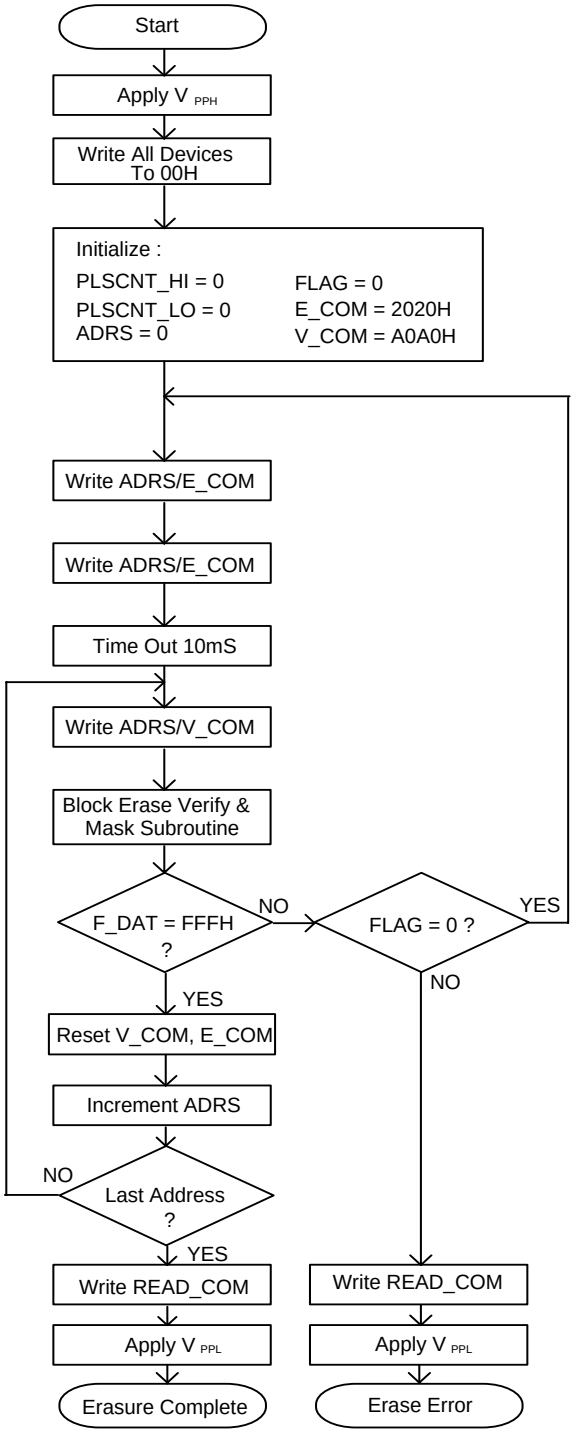


Comments
To look at the LO Byte, Mask* the HI Byte with 00.
If the LO Byte verifies, mask the LO Byte commands with the reset command (FFH)
If the LO Byte does not verify, then increment its pulse counter and check for max count. FLAG = 1 denotes a LO Byte error.
Repeat the sequence for the HI Byte.
FLAG = 2 denotes a HI Byte error. FLAG = 3 denotes both a HI and LO Byte errors. Flag = 0 denotes no max count errors; continue with algorithm.

Figure 7

*Masking can easily and efficiently be done in assembly languages. Simply load word registers with the incoming data (F_DAT), the program commands and the verify commands. Then manipulate the HI or LO register contents.

Erase Algorithm for Word-wide Mode



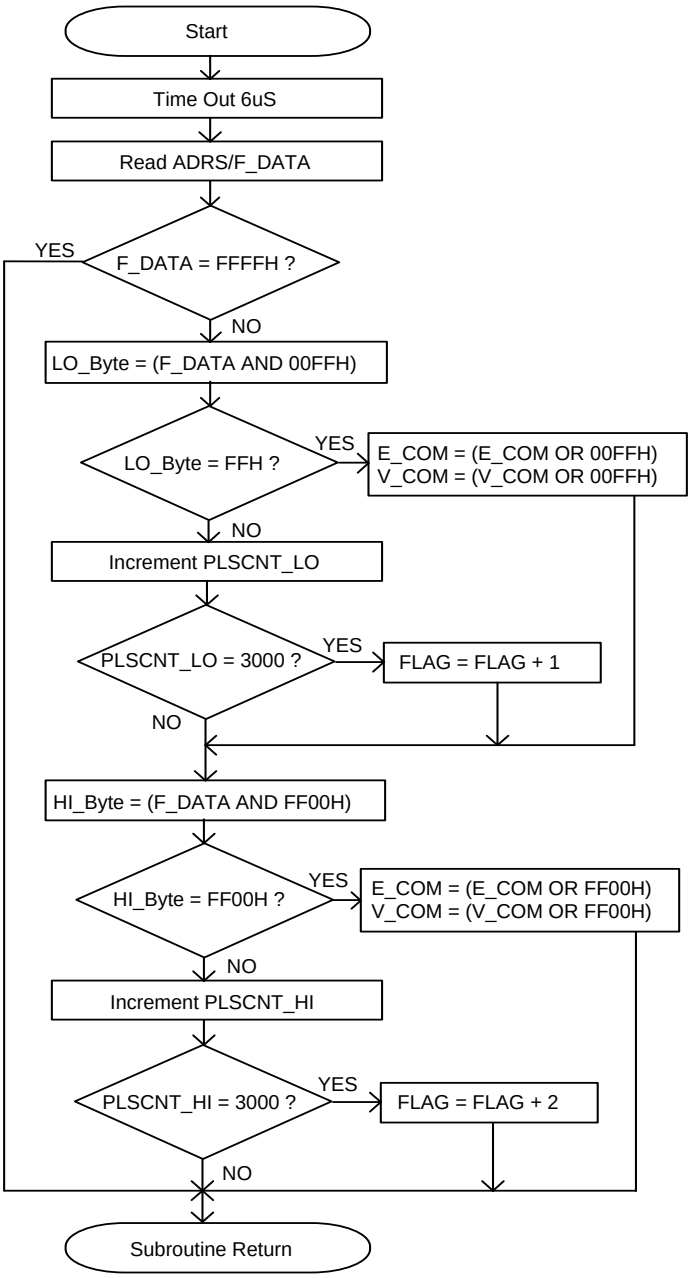
Comments
Wait for V_{PP} to stabilize
Use Write operation algorithm in x8 or x16 configuration Initialize Variables: PLSCNT_HI = HI Byte Pulse Counter PLSCNT LO = LO Byte Pulse Counter FLAG = Erasure error flag ADRS = Address E_COM = Erase Command V_COM = Verify Command Erase Set-up Command
Start Erasing
Duration of Erase Operation.
Erase Verify Command stops erasure.
See Block Erase Verify & Mask Subroutine
When both devices at ADRS are erased, F_DATA = FFFFH. If not equal, increment the pulse counter and check for last pulse. Reset commands default to (E_COM = 2020H) (V_COM = A0A0H) before verifying next ADRS.
Reset device for read operation.
Turn off V_{PP}.

Figure 8

Notes :

x16 Addressing uses A_1-A_{19} only. A_0 = 0 throughout word-wide operation.

Erase Verify and Mask Subroutine for Word-wide Mode



Comments
This subroutine reads the data word (F_DATA). It then masks the HI or LO Byte of the Erase and Verify commands from executing during the next operation. If both HI and LO Bytes verify, then return. Mask* the HI Byte with 00H. If the LO Byte verifies erasure, then mask* the next erase and verify commands with FFH (RESET). If the LO Byte does not verify, then increment its pulse counter and check for max count. FLAG = 1 denotes a LO Byte error. Repeat the sequence for the HI Byte. FLAG = 2 denotes a HI Byte error. FLAG = 3 denotes both a HI and LO Byte errors. Flag = 0 denotes no max count errors; continue with algorithm.

Figure 9

*Masking can easily and efficiently be done in assembly languages. Simply load word registers with the incoming data (F_DAT), the program commands and the verify commands. Then manipulate the HI or LO register contents.

DC Electrical Characteristics

(recommended operating conditions unless otherwise noted)

Symbol	Parameter	Byte Mode		Word Mode		Unit	Test Condition
		min	max	min	max		
I_{LI}	Input Leakage Current	-10	10	-10	10	uA	V_{IN} = 0V to V_{CC} (Note 1)
		-70	10	-70	10	uA	V_{IN} = 0V to V_{CC} (Note 2)
I_{LO}	Output Leakage Current	-10	10	-10	10	uA	CE1* = CE2* = V_{IH} or OE* = V_{IH} , V_{OUT} = 0V to V_{CC} (Note 3)
V_{IH}	Input High Voltage	2.4	V_{CC} + 0.3	2.4	V_{CC} + 0.3	V	
V_{IL}	Input Low Voltage	-0.3	0.8	-0.3	0.8	V	
V_{OH}	Output High Voltage	3.8		3.8		V	I_{OH} = -2.0mA (Note 4)
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 3.2mA (Note 4)
I_{CCS}	V_{CC} Standby Current		0.8		0.8	mA	CE1* = CE2* = V_{IH} or ≥ V_{CC}-0.2V
I_{CC1}	V_{CC} Active Read Current		50		80	mA	CE1* or/and CE2* = V_{IL}, Min. cycle, I_{OUT} = 0mA
I_{CC2}	V_{CC} Write Current		30		60	mA	Writing in progress
I_{CC3}	V_{CC} Erase Current		30		60	mA	Erasure in progress
I_{CC4}	V_{CC} Write Verify Current		30		60	mA	V_{PP} = V_{PPH} , WriteVerify in progress
I_{CC5}	V_{CC} Erase Verify Current		30		60	mA	V_{PP} = V_{PPH} , WriteVerify in progress
I_{PP1}	V_{PP} Read Current		0.8		1.6	mA	$V_{PP} > V_{CC}$
	or Standby Current		±0.04		±0.08	mA	$V_{PP} \leq V_{CC}$
I_{PP2}	V_{PP} Write Current		30		60	mA	V_{PP} = V_{PPH} Write in progress
I_{PP3}	V_{PP} Erase Current		30		60	mA	V_{PP} = V_{PPH} Erasure in progress
I_{PP4}	V_{PP} Write Verify Current		5.0		12	mA	V_{PP} = V_{PPH} Write Verify in progress
I_{PP5}	V_{PP} Erase Verify Current		5.0		12	mA	V_{PP} = V_{PPH} Erase Verify in progress
V_{PPL}	V_{PP} During Read-Only Operation	0	6.5	0	6.5	V	
V_{PPH}	V_{PP} During Erase / Write Operation	11.4	12.6	11.4	12.6	V	
V_{LKO}	V_{CC} Erase / Write lock Voltage	3.2		3.2		V	

Table 9

Notes : 1.) Except CE1* , CE2* , WE* , REG* pins.
2.) For CE1* , CE2* , WE* , REG* pins.
3.) Except BVD1* , BVD2* , CD1* , CD2* pins.
4.) Except CD1* , CD2* pins.

Input / Output Capacitance

(T = 25°C, f = 1MHZ) (These parameters are sampled , not 100% tested)

Symbol	Parameter	Min	Max	Unit	Conditions
C_{IN1}	Address Capacitance		8	pF	V_{IN} = 0V
C_{IN2}	Control Capacitance		16	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance		21	pF	V_{OUT} = 0V
$C_{I/O}$	I/O Capacitance		16	pF	$V_{I/O}$ = 0V

Table 10

AC Test Conditions

Input Rise and Fall Times (10% to 90%) 10ns

Input Pulse Levels ..... V_{OL} and V_{OH}

Input Timing Reference Level .....V_{IL} and V_{IH}

Output Timing Reference Level .....V_{IL} and V_{IH}

AC Electrical Characteristics — Common Memory Read Only Operations

Symbol		Parameter	Min	Max	Unit	Notes
t_{AVAV}	t_{RC}	Read Cycle Time	250		ns	2
t_{AVQV}	t_{ACC}	Address Access Time		250	ns	2
t_{ELQV}	t_{CE}	Card Enable Access Time		250	ns	2
t_{GLQV}	t_{OE}	Output Enable Access Time		125	ns	2
t_{ELQX}	t_{LZ}	Card Enable to Output in Low Z	5		ns	2
t_{EHQZ}		Card Disable to Output in High Z		60	ns	2
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5		ns	2
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z		60	ns	2
	t_{OH}	Output Hold from Address, CE*, or OE* Change	5		ns	1,2
t_{WHGL}		Write Recovery Time Before Read	6		us	2

Table 11

Notes :

1. Whichever occurs first.
2. Rise / Fall time ≤ 10ns

AC Electrical Characteristics — Common Memory Write/Erase Operations

(recommended operating conditions unless otherwise noted)

Symbol		Parameter	Min	Max	Unit	Notes
t_{AVAV}	t_{WC}	Write Cycle Time	250		ns	1,2
t_{AVWL}	t_{AS}	Address Set-up Time	0		ns	1,2
t_{WLAX}	t_{AH}	Address Hold Time	100		ns	1,2
t_{DVWH}	t_{DS}	Data Set-up Time	80		ns	1,2
t_{WHDX}	t_{DH}	Data Hold Time	30		ns	1,2
t_{WHGL}		Write Recovery Time Before Read	6		us	1,2
t_{GHWL}		Read Recovery Time Before Write	0		us	1,2
t_{WLOZ}		Output High-Z from Write Enable	5		ns	1,2
t_{WHOX}		Output Low-Z from Write Enable		60	ns	1,2
t_{ELWL}	t_{CS}	Card Enable Set-up Time Before write	40		ns	1,2
t_{WHEH}	t_{CH}	Card Enable Hold Time	0		ns	1,2
t_{WLWH}	t_{WP}	Write Pulse Width	100		ns	1,2
t_{WHWL}	t_{WPH}	Write Pulse Width High	50		ns	1,2
t_{WHWH1}		Duration of Write Operation	10		us	1,2,3
t_{WHWH2}		Duration of Erase Operation	9.5		ms	1,2,3
t_{VPEL}		V_{PP} Set-up Time to Card Enable Low	100		ns	1,2

Table 12

Notes :

1. Read timing parameters during read/write operations are the same as during read-only operations.

   Refer to AC Characteristics for Read-Only Operations.

2. Rise/Fall time ≤ 10ns.

3. The integrated stop timer terminates the write/erase operations , thereby eliminating the need for a maximum specification.

Read Operation Timing Diagram (Common Memory)

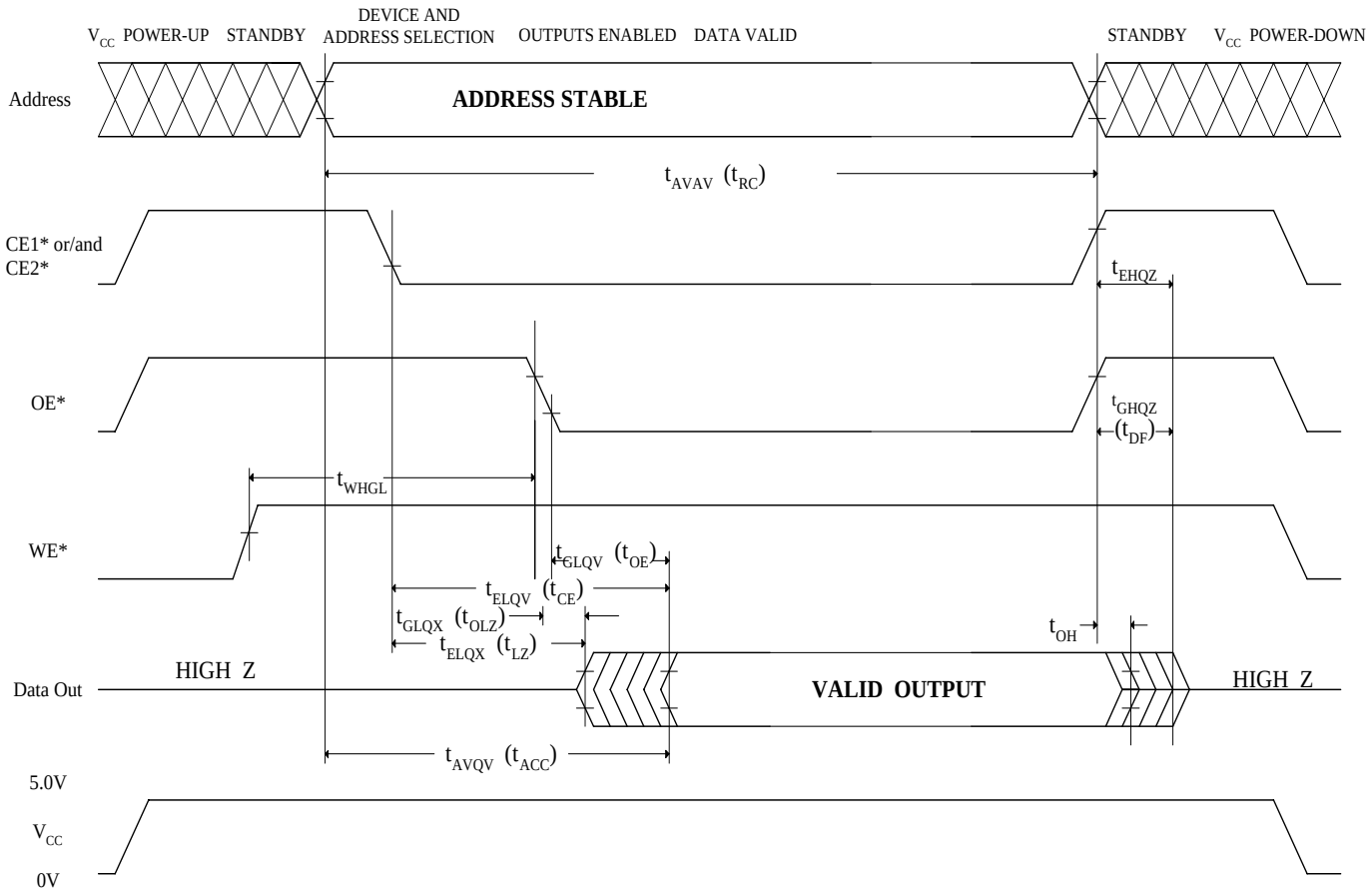


Figure 10

Write Operation Timing Diagram (Common Memory)

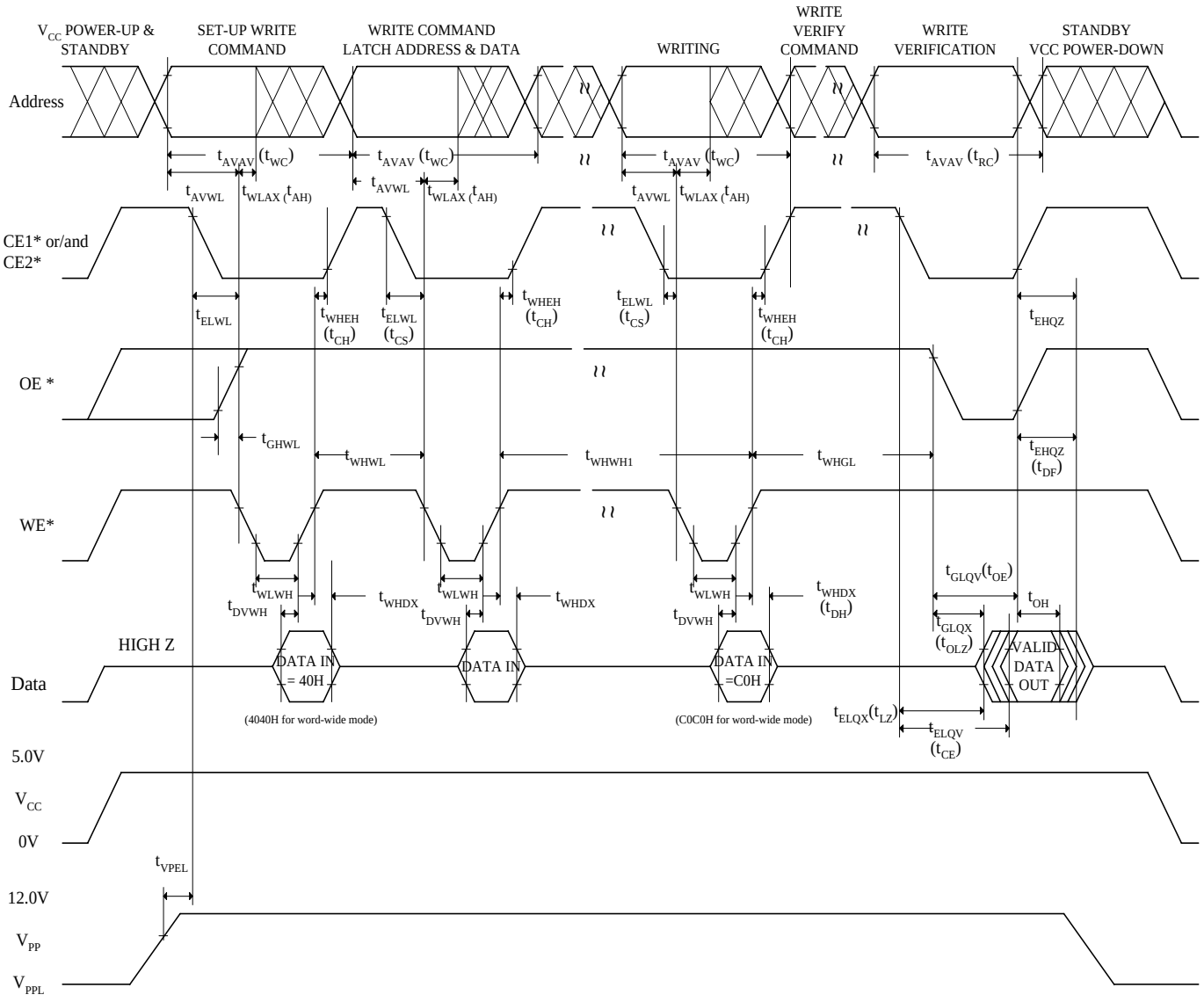


Figure 11

Erase Operation Timing Diagram (Common Memory)

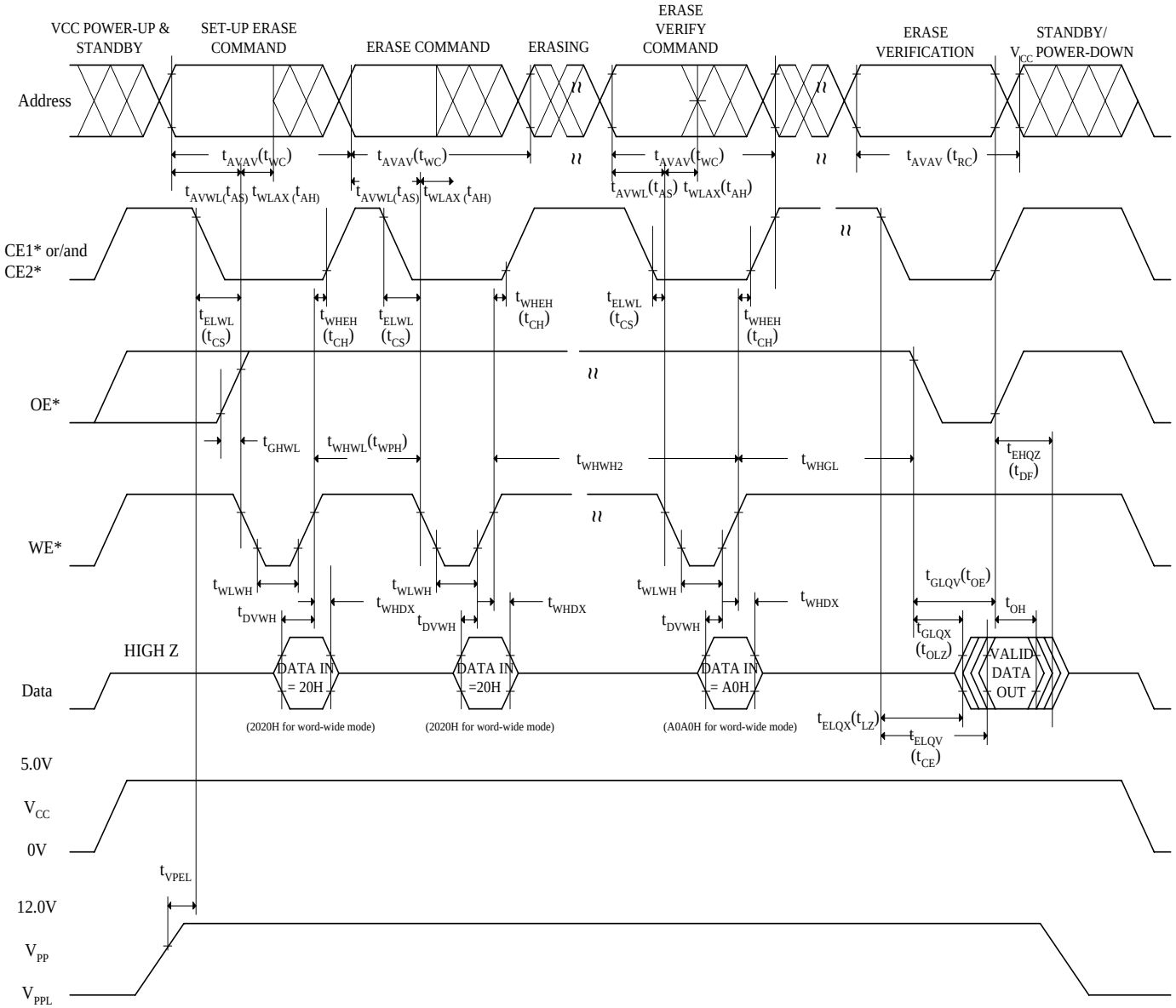


Figure 12

Alternative CE* Controlled Write Operations (Common Memory)

Symbol	Parameter	Min	Max	Unit	Notes
t_{AVAV}	Write Cycle Time	250		ns	
t_{AVEL}	Address Set-up Time	0		ns	
t_{ELAX}	Address Hold Time	100		ns	
t_{DVEH}	Data Set-up Time	80		ns	
t_{EHDX}	Data Hold Time	30		ns	
t_{EHGL}	Write Recovery Time Before Read	6		us	
t_{GHEL}	Read Recovery Time Before Write	0		us	
t_{WLEL}	Write Enable Set-up Time before Card-Enable	0		ns	
t_{EHWH}	Write Enable Hold Time	0		ns	
t_{ELEH}	Write Pulse Width	100		ns	1
t_{EHEL}	Write Pulse Width High	20		ns	
t_{PEL}	V_{PP} Set-up Time to Card-Enable Low	100		ns	

Table 13

Notes :

Card Enable Controlled Writes : Write operations are driven by the valid combination of Card Enable and Write Enable. In systems where Card Enable defines the write pulse width (with a longer Write Enable timing waveform) all set-up , hold and inactive Write Enable times should be measured relative to the Card Enable waveform.

Alternative CE* Controlled Write Timing Diagram (Common Memory)

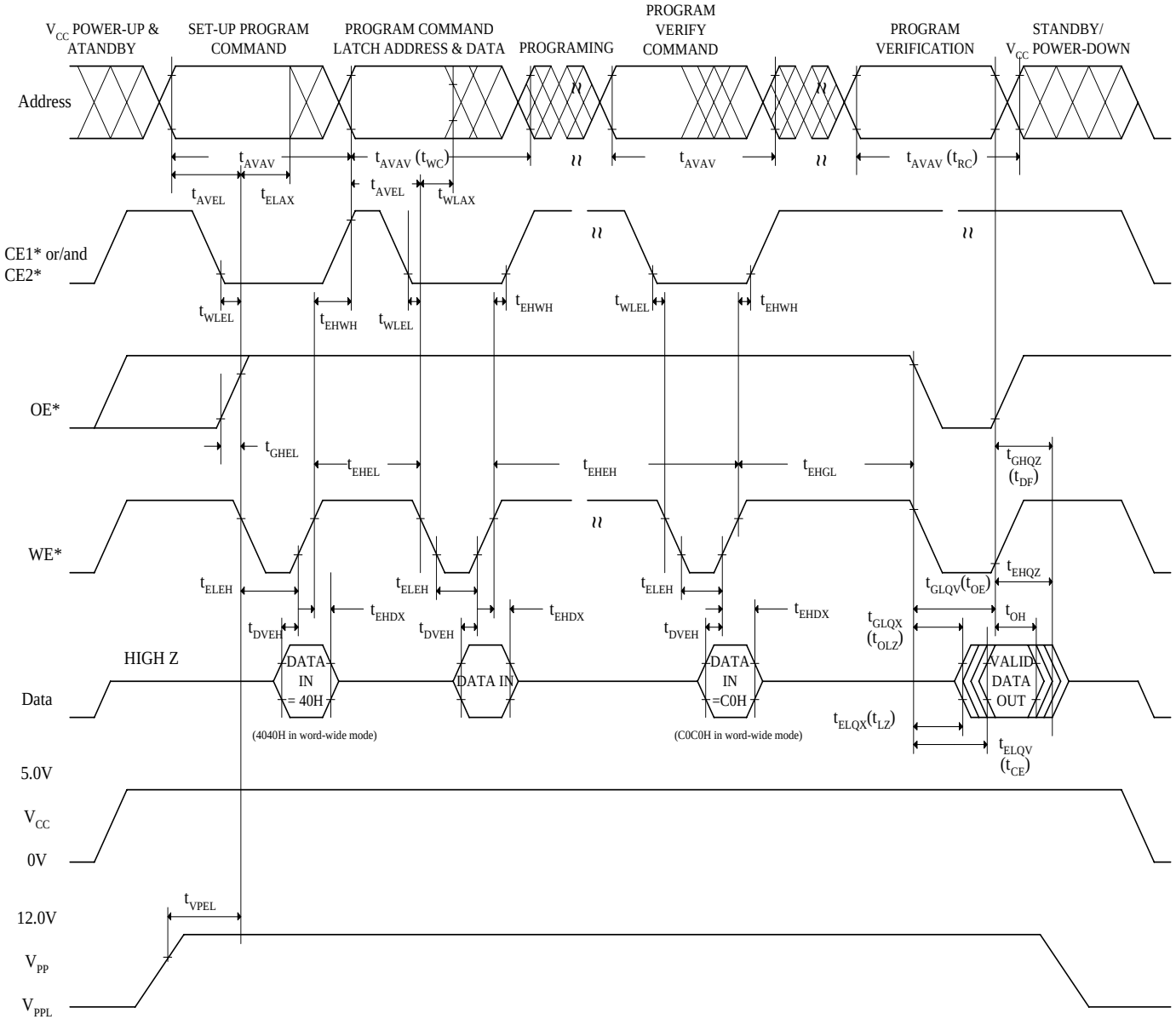


Figure 13

AC Electrical Characteristics (Attribute Memory)

(recommended operating conditions unless otherwise noted)

Read Cycle (Attribute Memory)

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{cr}	Read Cycle Time	300		ns	
$t_{a(A)}$	Address Access Time		300	ns	
$t_{a(CE)}$	Card Select Access Time		300	ns	
$t_{a(OE)}$	Output Enable Access Time		150	ns	
$t_{dis(CE)}$	Output Disable Time (from CE*)		100	ns	
$t_{dis(OE)}$	Output Disable Time (from OE*)		100	ns	
$t_{en(CE)}$	Output Enable Time (from CE*)	5		ns	
$t_{en(OE)}$	Output Enable Time (from OE*)	5		ns	
$t_{v(A)}$	Data Hold Time (from address changed)	0		ns	

Table 14

Write Cycle (Attribute Memory)

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{cw}	Write Cycle Time		1	ms	
t_{AS}	Address Setup Time	30		ns	
t_{AH}	Address Hold Time	50		ns	
t_{WP}	Write Pulse Width	120		ns	
t_{CS}	Card Enable Time to WE*	15		ns	
t_{CH}	Card Enable Hold Time from WE* High	0		ns	
t_{DS}	Data Setup Time	70		ns	
t_{DH}	Data Hold Time	30		ns	
t_{OES}	OE* Setup Time	30		ns	
t_{OEH}	OE* Hold Time	30		ns	

Table 15

Read Cycle Timing Diagram (Attribute Memory) (REG*=VIL , WE*=VIH)

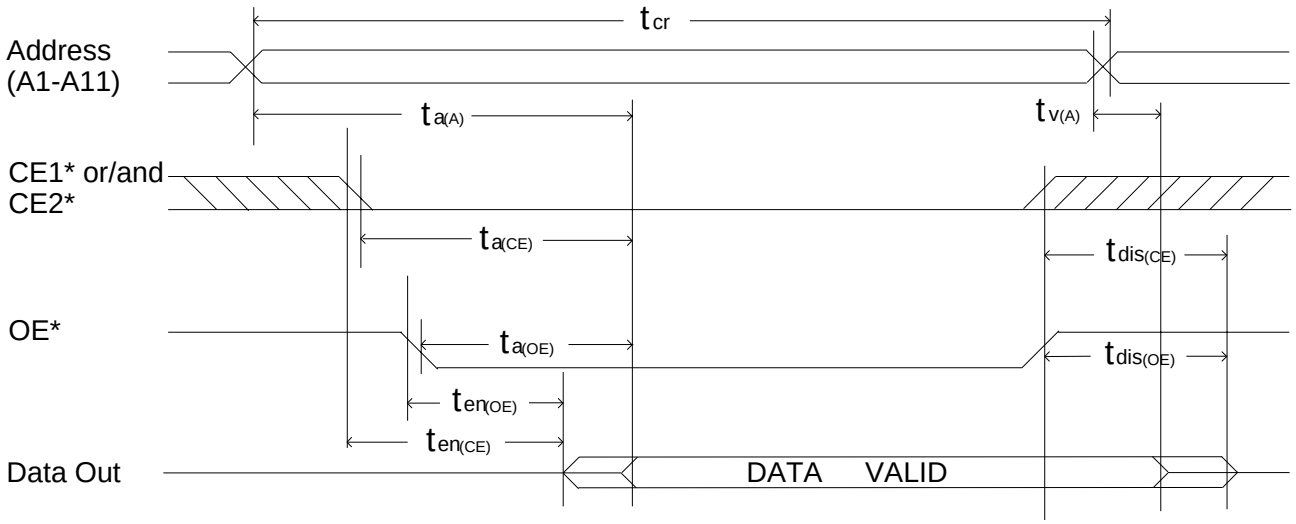


Figure 14

Write Cycle Timing Diagram (Attribute Memory) (REG*=VIL)

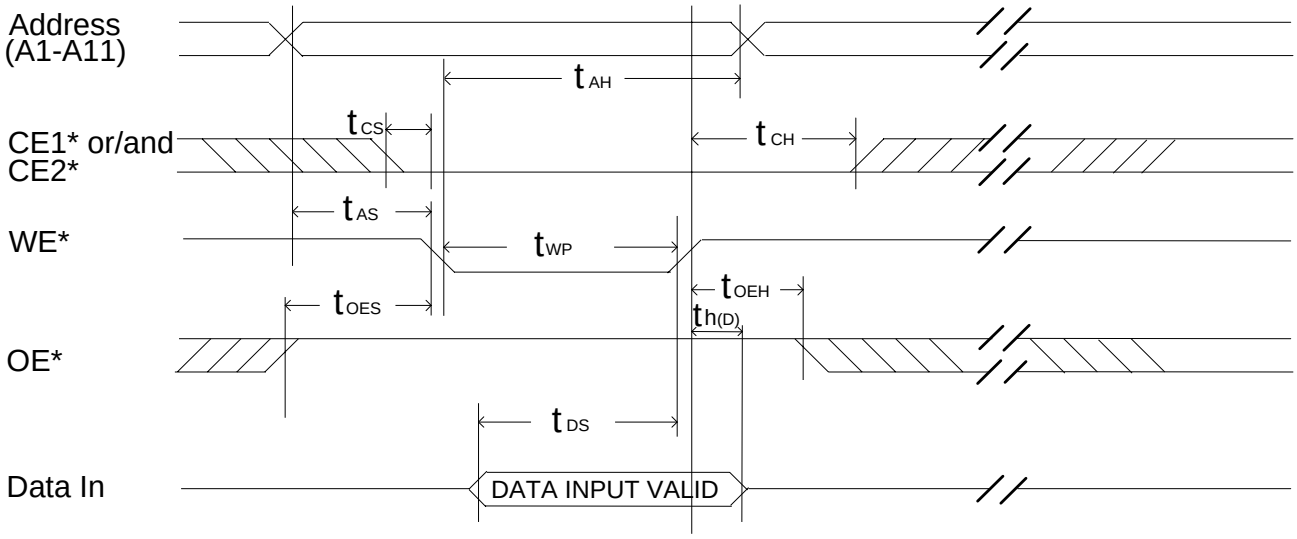


Figure 15

Outline Dimensions (Unit: mm)