LINEAR FLASH MEMORY CARD

SERIES-II (Fx2xxx)
Product Specification

Preliminary

Documentation History

Version	Description	Date	Written By
1.0	New Issue	Aug. 2006	Greg Liu

Contents

Features

★ PCMCIA / JEIDA standard

★ Memory Capacity : 2~8 Mega bytes

★ Byte(x8) / word(x16) data bus selectable

★ Fast read access time : 200ns (maximum)

★ Fast byte or word random write : 6us (typical)

★ Optional attribute memory : 8K byte E^2PROM

★ Read voltage : 5V , write/erase voltage : 12V

★ 128K byte per block structure

★ 100000 write/erase cycles per block

★ Automatic erase/write

- command user interface

- status register

★ Erase suspend capability

- keeps erase as back ground task

★ Built-in write protect switch

★ Credit card size : 54.0 x 85.6 x 3.3 (mm)

★ Commercial / Industrial grade

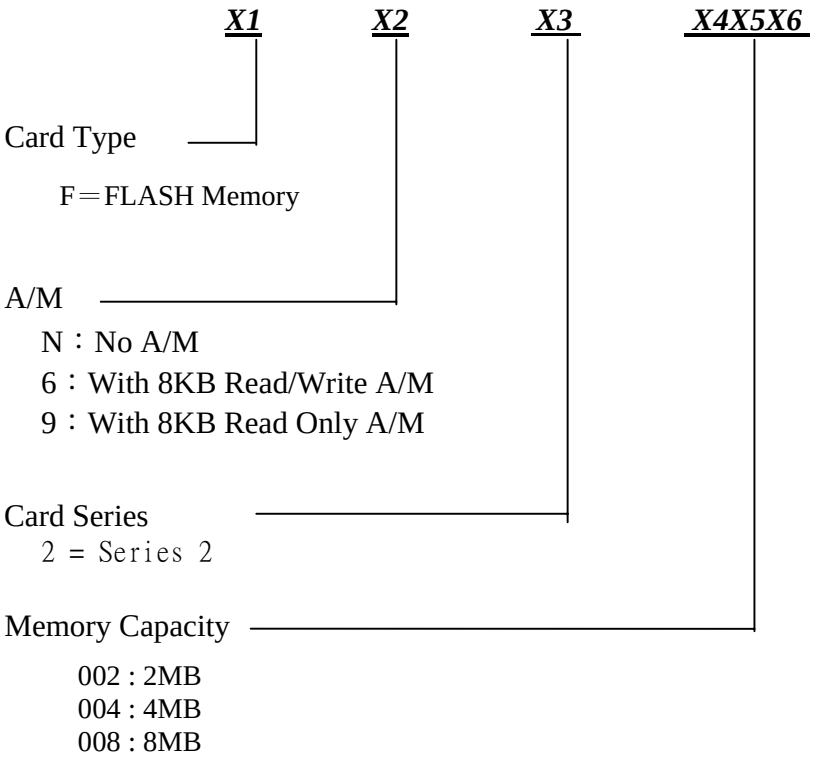
General Description

C-ONE's high performance FLASH memory cards conform to the PCMCIA / JEIDA international standard and consist of multiple Intel's 28F008SA or compatible FLASH memory devices and decoder IC mounted on a very thin printed circuit board using surface mounting technology.

This series Flash memory cards contain 32 to 256 independent device blocks. Each block can be individually erasable. To support PCMCIA-compatible byte-wide operation , the flash array is divided into 128K x 8 bits device blocks. To support PCMCIA-compatible word-wide operation , the devices are paired so that each accessible memory block is 64K words.

This series Flash memory cards offer portable , reprogrammable and nonvolatile solid-state storage media and can be used for flexible integration into various system platforms with PCMCIA/JEIDA interface. With the extra and optional 8K bytes "attribute memory" space , the Card Information Structure (CIS) can be written into it by C-ONE or by customer with standard format or customized requirements.

Product Number Definition



Note : A/M means attribute memory.

Product List

Item No.	Part Number	Memory Capacity		Attribute	Memory
		Bytes	Words	Size	Status
1.	FN2002	2M	1M	None	None
2.	FN2004	4M	2M		
3.	FN2006	6M	3M		
4.	FN2008	8M	4M		
5.					
6.					
7.					
8.					
9.	F62002	2M	1M	8KB E^2PROM	Readable / Writable
10.	F62004	4M	2M		
11.	F62006	6M	3M		
12.	F62008	8M	4M		
13.					
14.					
15.					
16.					
17.	F92002	2M	1M	8KB E^2PROM	Read only
18.	F92004	4M	2M		
19.	F92006	6M	3M		
20.	F92008	8M	4M		
21.					
22.					
23.					
24.					

Table 1 ----- with optional 8KB attribute memory

Block Diagram

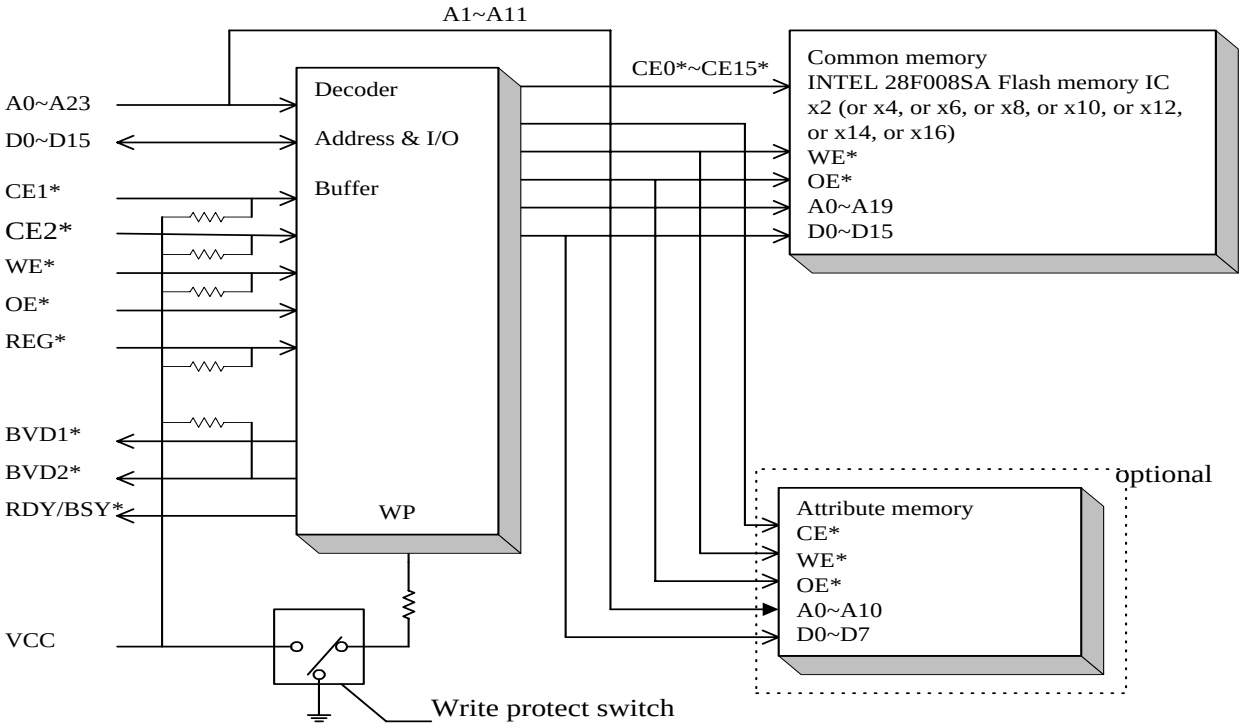


Figure 1 Cards with optional 8KB attribute memory

Pin Configuration (16MB card with attribute memory)

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Pin no.
VCC	RY/BY*	WE*	A14	A13	A8	A9	A11	OE*	A10	CE1*	D7	D6	D5	D4	D3	GND	Pin Name
34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	Pin No.
GND	WP	D2	D1	D0	A0	A1	A2	A3	A4	A5	A6	A7	A12	A15	A16	VPP1	Pin Name
51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	Pin No.
VCC	A21	A20	A19	A18	A17	NC	NC	NC	CE2*	D15	D14	D13	D12	D11	CD1*	GND	Pin Name
68	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	Pin No.
GND	CD2*	D10	D9	D8	BVD1*	BVD2*	REG*	NC	NC	NC	NC	NC	NC	A23	A22	VPP2	Pin Name

Table 3

Note :*mean low active
2MB card series : A21,A22,A23 = NC
4MB card series : A22,A23 = NC
6MB card series : A23 = NC
8MB card series : A23 = NC

Pin Description

Symbol	Function	I/O
A0-A23	Addresses	I
D0-D15	Data Inputs/Outputs	I/O
CE1*/CE2*	Card Enable	I
OE*	Output Enable	I
WE*	Write Enable	I
REG*	Attribute Memory Enable	I
WP	Write-protect status Detect	O
BVD1*/BVD2*	Battery Voltage Detect (pull high to Vcc internally)	O
RY/BY*	Ready/Busy status	O
CD1*/CD2*	Card Detect (tied to GND internally)	O
VCC	+5 Volt Power Supply	-
VPP1/VPP2	Write (programming) Power Supply	-
GND	Ground	-
NC	No Connection	-

Table 4

Pin Location

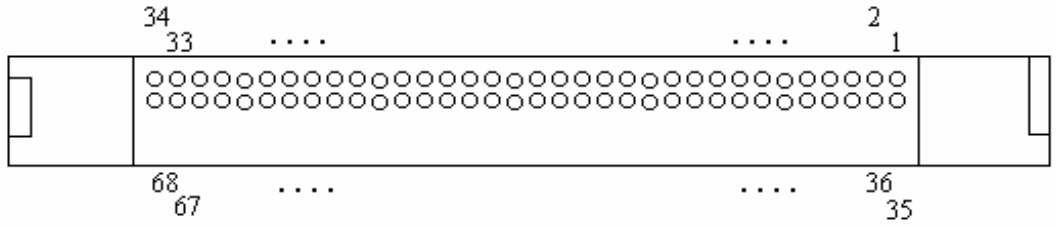


Figure 3 Bottom View (Connector Side)

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
V_{CC} Supply Voltage	V_{CC}	4.5	5.5	V
V_{PP} Supply Voltage (read)	V_{PPL}	0	6.5	V
V_{PP} Supply Voltage (erase/write)	V_{PPH}	11.4	12.6	V
Input High Voltage	V_{IH}	2.4	VCC + 0.3	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Operating Temperature(Commercial)	T_{OPR}	0	70	º C
Operating Temperature(Industrial)	T_{OPR}	-40	85	º C

Table 5

Absolute Maximum Rating *

Parameter	Symbol	Value	Unit
V_{CC} Supply Voltage	V_{CC}	-0.5 to +6.0	V
V_{PP} Supply Voltage (read)	V_{PPL}	-2.0 to +7.0	V
V_{PP} Supply Voltage (erase/write)	V_{PPH}	-2.0 to +14.0	V
Input Voltage	V_{IN}	-0.5 to V_{CC} + 0.3(6V max.)	V
Output Voltage	V_{OUT}	-0.5 to +6.0	V
Operating Temperature (Commercial)	T_{OPR}	0 to +70	º C
Operating Temperature (Industrial)	T_{OPR}	-40 to +85	º C
Storage Temperature	T_{STR}	-40 to +125	º C
Relative Humidity (non-condensing)	H_{UM}	95(maximum)	%

Table 6

***Comments**

Stress above those listed under " Absolute Maximum Ratings " may cause permanent damage to the products. These are stress rating only. Functional operation of these products at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Common Memory Function Table

Function	REG*	CE2*	CE1*	A0	OE*	WE*	V_{PP2}	V_{PP1}	D15-D8	D7-D0
Standby	X	H	H	X	X	X	V_{PPL}	V_{PPL}	High-Z	High-Z
Byte Read	H	H	L	L	L	H	V_{PPL}	V_{PPL}	High-Z	Even Byte Data Out
	H	H	L	H	L	H	V_{PPL}	V_{PPL}	High-Z	Odd Byte Data Out
Word Read	H	L	L	X	L	H	V_{PPL}	V_{PPL}	Odd Byte Data Out	Even Byte Data Out
Odd Byte Only Read	H	L	H	X	L	H	V_{PPL}	V_{PPL}	Odd Byte Data Out	High-Z
Byte Write	H	H	L	L	H	L	V_{PPH}	V_{PPH}	X	Even Byte Data In
	H	H	L	H	H	L	V_{PPH}	V_{PPH}	X	Odd Byte Data In
Word Write	H	L	L	X	H	L	V_{PPH}	V_{PPH}	Odd Byte Data In	Even Byte Data In
Odd Byte Only Write	H	L	H	X	H	L	V_{PPH}	V_{PPH}	Odd Byte Data In	X

Table 7

Attribute Memory Function Table

Function	REG*	CE2*	CE1*	A0	OE*	WE*	V_{PP2}	V_{PP1}	D15-D8	D7-D0
Standby	X	H	H	X	X	X	V_{PPL}	V_{PPL}	High-Z	High-Z
Byte Read	L	H	L	L	L	H	V_{PPL}	V_{PPL}	High-Z	Even Byte Data Out
	L	H	L	H	L	H	V_{PPL}	V_{PPL}	High-Z	Invalid Data Out
Word Read	L	L	L	X	L	H	V_{PPL}	V_{PPL}	Invalid Data Out	Even Byte Data Out
Odd Byte Only Read	L	L	H	X	L	H	V_{PPL}	V_{PPL}	Invalid Data Out	High-Z
Byte Write	L	H	L	L	H	L	V_{PPL}	V_{PPL}	X	Even Byte Data In
	L	H	L	H	H	L	V_{PPL}	V_{PPL}	X	X
Word Write	L	L	L	X	H	L	V_{PPL}	V_{PPL}	X	Even Byte Data In
Odd Byte Only Write	L	L	H	X	H	L	V_{PPL}	V_{PPL}	X	X

Table 8

Notes :

1. L=V_{IL} ; H=V_{IH} ; X=don't care , can be either V_{IH} or V_{IL}.

Card Information Structure

The Card Information Structure (CIS) starts from address zero of the card's Attribute Memory. It contains a variable-length chain of data blocks (tuples). The table shown below is the generic CIS of C-ONE's Series 2 Flash Memory Card. (For detailed tuple description, please refer to the Metaformat Specification of PC Card Standard.)

Tuple Address (Hex)	Data (Hex)	Description
00	01	CISTPL_DEVICE
02	03	TPL_LINK
04	52	DEVICE_INFO = FLASH 200ns
06	06	CARD SIZE 2MB
	0E	4MB
	16	6MB
	1E	8MB
	26	10MB
	2E	12MB
	36	14MB
	3E	16MB
08	FF	CISTPL_END
0A	15	CISTPL_VERS_1
0C	1F	TPL_LINK
0E	04	TPLLV1_MAJOR
10	01	TPLLV1_MINOR
12	00	NULL
14	53	S
16	45	E

Tuple Address (Hex)	Data (Hex)	Description
18	52	R
1A	49	I
1C	45	E
1E	53	S
20	2D	- (dash)
22	32	2
24	20	SPACE
26	20	SPACE (for 2/4/6/8MB)
	31	1 (for 10/12/14/16MB)
28	30	0
	32	2
	34	4
	36	6
	38	8
2A	4D	M
2C	42	B
2E	20	SPACE
30	46	F
32	4C	L

Tuple Address (Hex)	Data (Hex)	Description
34	41	A
36	53	S
38	48	H
3A	20	SPACE
3C	43	C
3E	41	A
40	52	R
42	44	D
44	00	Product Information terminated by NULL
46	00	No Additional Product Information
48	00	No Additional Product Information
4A	FF	CISTPL_END
4C	18	CISTPL_JEDEC_C
4E	02	TPL_LINK
50	89	INTEL JEDEC ID
52	A2	28F008SA JEDEC ID
54	1E	CISTPL_DEVICEGEO
56	06	TPL_LINK
58	02	DGTPL_BUS

Tuple Address (Hex)	Data (Hex)	Description
5A	11	DGTPL_EBS
5C	01	DGTPL_RBS
5E	01	DGTPL_WBS
60	01	DGTPL_PART
62	01	DGTPL_HWIL
64	21	CISTPL_FUNCID
66	02	TPL_LINK
68	01	MEMORY CARD
6A	00	NO EXPANSION ROM & POWER ON SELF TEST
6C	FF	CISTPL_END
6E	FF	CISTPL_END

Command Set Table

Command	Bus Cycles Req	First Bus Cycle				Second Bus Cycle				Notes
		Operation	Address	Data		Operation	Address	Data		
				×8 Mode	×16 Mode			×8 Mode	×16 Mode	
Read Array/Reset	1	Write	DA	FFH	FFFFH					2
Intelligent Identifier	3	Write	DA	90H	9090H	Read	IA	IID	IID	2,3,4
Read Status Register	2	Write	DA	70H	7070H	Read	DA	SRD	SRD	2,3
Clear Status Register	1	Write	DA	50H	5050H					2
Erase Setup/Erase Confirm	2	Write	BA	20H	2020H	Write	BA	D0H	D0D0H	2
Erase Suspend/Erase Resume	2	Write	DA	B0H	B0B0H	Write	DA	D0H	D0D0H	2
Write Setup/Write	2	Write	WA	40H	4040H	Write	WA	WD	WD	2,3
Alternate Write Setup/Write	2	Write	WA	10H	1010H	Write	WA	WD	WD	2,3,5

Table 9

Notes :

1. Commands other than those shown above are reserved by Intel for future device implementations and should not be used.
2. DA = A device-level (or device pair) address within the card.

   BA = Address within the block of a specific device (device pair) being erased.

   WA = Address of memory location to be written.

   IA = A device-level address ; 00H for manufacture code , 01 for device code.
3. SRD = Data read from Device Status Register.

   WD = Data to be written at location WA. Data is latched on the rising edge of WE*.

   IID = Data read from intelligent identifiers.
4. Following the intelligent identifier command , two read operations access manufacturer code (89H) and device code (A2H).
5. Either 40H or 10H are recognized by the WSM as the Write Setup command.

Command Definitions

When V_{PPL} is applied to the V_{PP1} , V_{PP2} pins , read operations from the Status Register , intelligent identifiers , or array blocks are enabled. Placing V_{PPH} on V_{PP1} , V_{PP2} pins enables successful write and block erase operations as well.

Card operations are selected by writing specific commands into the Command User Interface (CUI). Command Set Tables defines this series Flash cards commands.

Read Array Command

Upon initial card powerup and after exit from deep powerdown mode , this series Flash cards default to the Read Array mode. This operation is also entered by writing FFH to the Command User Interface. Microprocessor read cycles retrieve array data. The card remains enabled for reads until the Command User Interface receives an alternate command. Once the internal Write State Machine has started a block-erase or data-write operation , the card will not recognize the Read Array command , until the WSM has completed its operation (or the Erase Suspend command is issued during erase). The Read Array command functions when V_{PP1} , $V_{PP2} = V_{PPL}$ or V_{PPH}.

Intelligent Identifier Command

After executing this command , the intelligent Identifier values can be read. Only address A0 of each device is used in this mode , all other address inputs are ignored [(Manufacturer code=89H for A_0=0) , (Device code=A2H (INTEL 28F008SA) for A_0=1)]. The device will remain in this mode until the CUI receives another command.

This information is useful by system software in determining what type of flash memory device is contained within the card and allows the correct matching of device to write and erase algorithms. System software that fully utilizes the PCMCIA specification will not use the intelligent identifier mode , as this data is available within the Card Information Structure. The Intelligent Identifier command functions when V_{PP1} , $V_{PP2} = V_{PPL}$ or V_{PPH}.

Read Status Register Command

After writing this command , a device read outputs the contents of its Status Register , regardless of the address presented to that device. The contents of this register are latched on the falling edge of OE* , CE1* (and/or CE2*) , whichever occurs last in the read cycle. This prevents possible bus errors which might occur if the contents of the Status Register changed while reading its contents. CE1* (and CE2* for odd-byte or word access) or OE* must be toggled with each subsequent status read , or the completion of a write or erase operation will not be evident. This command is executable while the WSM is operating , however , during a block-erase or data-write operation , reads from the device will automatically return status register data. Upon completion of that operation , the device remains in the Status Register read mode until the CUI receives another command. The Read Status Register command functions when V_{PP1} , $V_{PP2} = V_{PPL}$ or V_{PPH}.

Clear Status Register Command

The Erase Status and Write Status bits are set to "1"s by the Write State Machine and can only be reset by the Clear Status Register Command. These bits indicate various failure conditions. By allowing system software to control the resetting of these bits , several operations may be performed (such as cumulatively writing several bytes or erasing multiple blocks in sequence). The Status Register may then be polled to determine if an error occurred during that sequence. This adds flexibility to the way the device may be used.

Additionally , the VPP Status bit (SR.3) MUST be reset by system software before further data writes or block erases are attempted. To clear the Status Register , the Clear Status Register command is written to the Command User Interface. The Clear Status Register command functions when V_{PP1} , $V_{PP2} = V_{PPL}$ or V_{PPH}.

Erase Setup/Erase Confirm Commands

Within a device , erase is performed on one device block at a time , initiated by a two-cycle command sequence. After the system switches V_{PP} to V_{PPH} , an Erase Setup command (20H) prepares the CUI for the Erase Confirm command (D0H). The device's WSM controls the erase algorithms internally. After receiving the two-command erase sequence , the device automatically outputs Status Register data when read (See Figure 4). If the command after erase setup is not an Erase Confirm command , the CR sets the Write Failure and Erase Failure bits of the Status Register , places the device into the Read Status Register mode , and waits for another command. The Erase Confirm command enables the WSM for erase (simultaneously closing the address latches for that device's block (A_{16}-A_{19} at the device level). The CPU detects the completion of the erase operation by analyzing card-level or device -level indicators. Card-level indicators include the RY/BY* pin and the READY-BUSY* Status Register ; while device-level indicators include the specific device's Status Register. Only the Read Status Register command is valid while the erase operation is active. Upon completion of the erase sequence (see section on Status Register) the device's Status Register reflects the result of the erase operation. The device remains in the Read Status Register mode until the CUI receives an alternate command.

The two-step block-erase sequence ensures that memory contents are not accidentally erased. Erase attempts while $V_{PPL} < V_{PP} < V_{PPH}$ produce spurious results and are not recommended. Reliable block erasure only occurs when $V_{PP}=V_{PPH}$. In the absence of this voltage , memory contents are protected against erasure. If block erase is attempted while $V_{PP}=V_{PPL}$, the V_{PP} Status bit will be set to "1".

When erase completes , the Erase Status bit should be checked. If an erase error is detected , the device's Status Register should be cleared. The CUI remains in Read Status Register mode until receiving an alternate command.

Erase Suspend/Erase Resume Commands

Erase Suspend allows block erase interruption in order to read data from another block of the device or to temporarily conserve power for another system operation. Once the erase process starts , writing the Erase Suspend command to the CUI (See Figure 5) requests the WSM to suspend the erase sequence at a predetermined point in the erase algorithm. In the erase suspend state , the device continues to output Status Register data when read.

Polling the device's RY/BY* and Erase Suspend Status bits (Status Register) , or the card's READY-BUSY* Status Register for that particular device , will determine when the erase suspend mode is valid. It is important to note that the card's RY/BY* pin will also transition to V_{OH} and will generate an interrupt if this pin is connected to a system-level interrupt. At this point , a Read Array command can be written to the device's CUI to read data from blocks **other than that which is suspended**. The only other valid commands at this time are Read Status Register (70H) and Erase Resume (D0H). If V_{PP} goes low during Erase Suspend , the V_{PP} Status bit is set in the Status Register.

The Erase Resume command clears the Erase Suspend state and allows the WSM to continue with the erase operation. The device's RY/BY* Status and Erase Suspend Status bits and the card's READY-BUSY* Status Register are automatically updated to reflect the erase resume condition. The card's RY/BY* pin also returns to V_{OL}.

Write Setup/Write Commands

A data-write operation is executed by a two-command sequence. After the system switches V_{PP} to V_{PPH} , the write setup command (40H) is written to the CUI of the appropriate device , followed by a second write specifying the address and write data (latched on the rising edge of WE*). The device's WSM controls the data-write and write verify algorithms internally. After receiving the two-command write sequence , the device automatically outputs Status Register data when read (See Figure 3). The CPU detects the completion of the write operation by analyzing card-level or device-level indicators. Card-level indicators include the RY/BY* pin and the READY-BUSY* Status Register ; while device-level indicators include the specific device's Status Register. Only the Read Status Register command is valid while the write operation is active. Upon completion of the data-write sequence (see section on Status Register) the device's Status Register reflects the result of the write operation. The device remains in the Read Status Register mode until the CUI receives an alternate command.

Device Status Register Definition

Each 28F008SA device in this Series 2 Card contains a Status Register which displays the condition of its Write State Machine. The Status Register is read at any time by writing the Read Status command to the CUI. After writing this command , all subsequent Read operations output data from the Status Register , until another command is written to the CUI.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WSMS	ESS	ES	BWS	VPPS	R	R	R

Table 10

Bit 7 --- WAM Status

This bit reflects the Ready/Busy* condition of the WSM. A '1' indicates that read , block-erase or data-write operations are available. A '0' indicates that write or erase operations are in progress.

Bit 6 --- Erase Suspend Status

If an Erase Suspend command is issued during the erase operation , the WSM halts execution and sets the WSM Status bit and the Erase Suspend Status bit to a '1'. This bit remains set until the device receives an Erase Resume command , at which point the CUI resets the WSM Status bit and the Erase Suspend Status bit.

Bit 5 --- Erase Status

This bit will be cleared to 0 to indicate a successful block-erasure. When set to a '1' , the WSM has been unsuccessful at performing an erase verification. The device's CUI only resets this bit to a '0' in response to a Clear Status Register command.

Bit 4 --- Write Status

This bit will be cleared to a 0 to indicate a successful data-write operation. When the WSM fails to write data after receiving a write command , the bit is set to a '1' and can only be reset by the CUI in response to a Clear Status Register command.

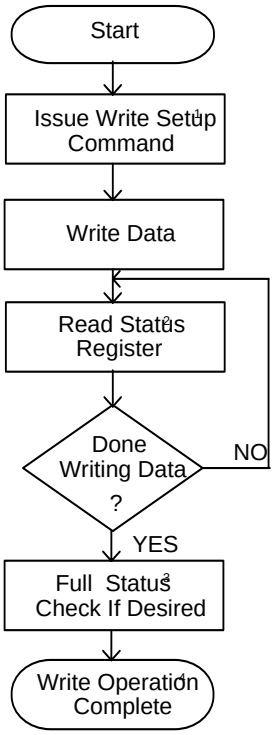
Bit 3 --- V_{PP} Status

During block-erase and data-write operations , the WSM monitors the output of the device's internal V_{PP} detector. In the event of low V_{PP} , the WSM sets ('1') the V_{PP} Status bit , the status bit for the operation in progress (either write or erase). The CUI resets these bits in response to a Clear Status Register command . Also , the WSM RY/BY* bit will be set to indicate a device ready condition. This bit MUST be reset by system software (Clear Status Register command) before further data writes or block erases are attempted.

Bit 2 , Bit 1 , Bit 0 --- Reserved for future enhancements

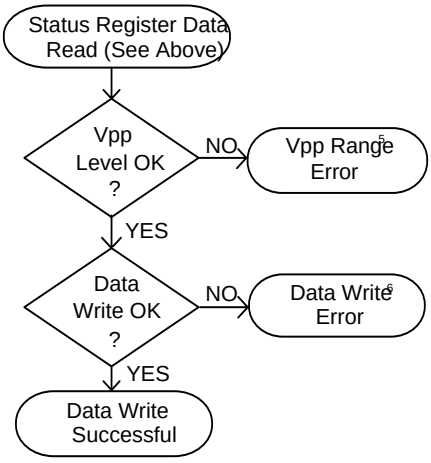
These bits are reserved for future use and should be masked out when polling the Status Register.

Device -- Level Automated Write Algorithm



Bus Operation	Command	x8 Mode	x16 Mode
Write	Write Setup	Data=40H Address=Byte Within Card to be Written	Data=4040H Address=Word Within Card to be Written
Write	Data Write	Data to be Written Address=Byte Within Card to be Written	Data to be Written Address=Word Within Card to be Written
Read	Defaults to Device Status Register Read Mode	Status Register Data. Toggle OE* CE1* or CE2* to update Status Register	Status Register Data. Toggle OE* or (CE1* and CE2*) to update Status Registers
Standby		Check SR Bit 7 1=Ready, 0=Busy	Check SR Bits 7&15 1=Ready, 0=Busy

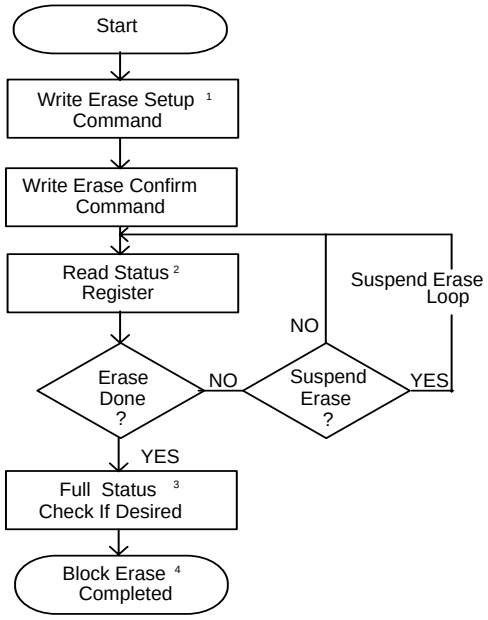
Full Status Check Procedure



Bus Operation	Command	x8 Mode	x16 Mode
Standby		Check SR Bit 3 1=V_{PP} Detected Low	Check SR Bits 3&11 1=V_{PP} Detected Low
Standby		Check SR Bit 4 1=Data Write Error	Check SR Bits 4&12 1=Data Write Error

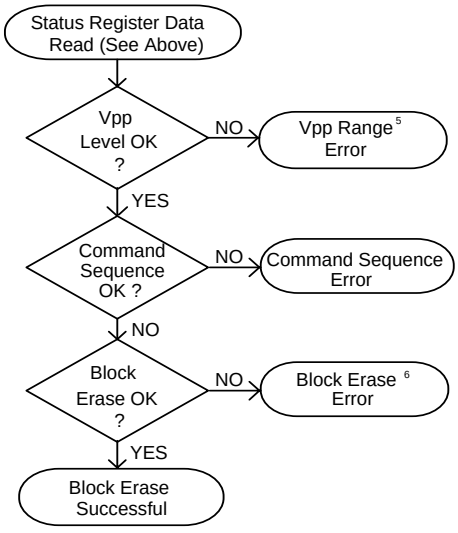
Figure 4

Device--Level Automated Erase Algorithm



Bus Operation	Command	x8 Mode	x16 Mode
Write	Erase Setup	Data=20H, Address=Block Within Card to be Erased	Data=2020H, Address=Block pair Within Card to be Erased
Write	Erase	Data=D0H, Address=Block Within Card to be Erased	Data=D0D0H, Address=Block Pair Within Card to be Erased
Read	Defaults to Device Status Register Read Mode	Status Register Data. Toggle OE* CE1* or CE2* to update Status Register	Status Register Data. Toggle OE* or (CE1* and CE2*) to update Status Register
Standby		Check SR Bit 7 1=Ready, 0=Busy	Check SR Bits 7&15 1=Ready, 0=Busy

Full Status Check Procedure



Bus Operation	Command	x8 Mode	x16 Mode
Standby		Check SR Bit 3 1=V_{PP} Detected Low	Check SR Bits 3&11 Either bit 1=V_{PP} Detected Low
Standby		Check SR Bits 4&5 Both 1=Command Sequence Error	Check SR Bit 4,5,12,13 All 1=Command Sequence Error
Standby		Check SR Bit 5 1=Block Erase Error	Check SR Bits 5&13 Both 1=Block Erase Failure

Figure 5

Erase Suspend/Resume Algorithm

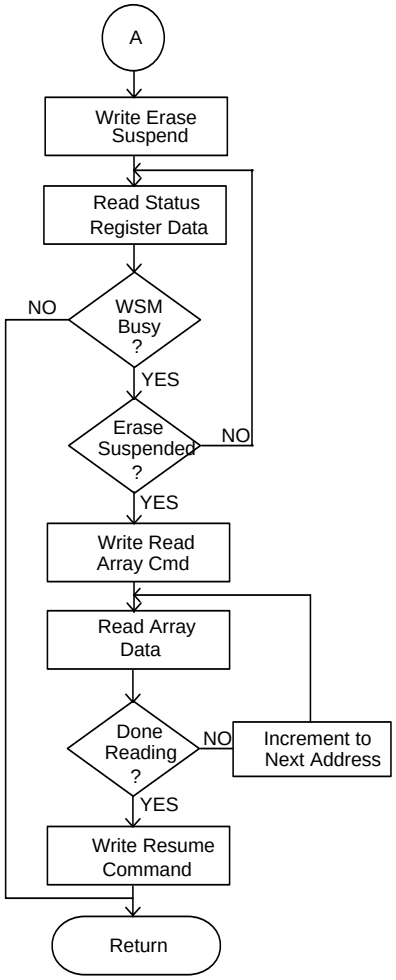


Figure 5

Bus Operation	Command	x8 Mode	x16 Mode
Write	Suspend Erase	Data=B0H Address=Desired Block to Erase Suspend	Data=B0B0H, Address=Desired Block Pair to Erase Suspend
Read		Status Register Data. Toggle OE* CE1* or CE2* to update Status Register	Status Register Data. Toggle OE* or (CE1* and CE2*) to update Status Register
Standby		Check SR Bit 7 1=Ready, 0=Busy	Check SR Bit 7&15 1=Ready, 0=Busy
Standby		Check SR Bit 6 1=Suspended, 0=In Progress	Check SR Bit 6&14 1=Suspended, 0=In Progress
Write	Read Array Cmd	Data=FFH	Data-FFFFH
Read		Read Data until finished	Read Data until finished
Write	Erase Resume	Data=D0H, Address=Valid Block Address.	Data-D0D0H, Address=Valid Block Pair Address.

Figure 6

DC Electrical Characteristics

(recommended operating conditions unless otherwise noted)

Symbol	Parameter	8-Bit Mode		16-Bit Mode		Unit	Test Condition
		min	max	min	max		
I_{LI}	Input Leakage Current	-10	10	-10	10	uA	V_{IN} = 0V to V_{CC} (Note 1)
		-70	10	-70	10	uA	V_{IN} = 0V to V_{CC} (Note 2)
I_{LO}	Output Leakage Current	-10	10	-10	10	uA	CE1* = CE2* = V_{IH} or OE* = V_{IH} , V_{OUT} = 0V to V_{CC} (Note 3)
V_{IH}	Input High Voltage	2.4	V_{CC}+0.3	2.4	V_{CC}+0.3	V	
V_{IL}	Input Low Voltage	-0.3	0.8	-0.3	0.8	V	
V_{OH}	Output High Voltage	3.8		3.8		V	I_{OH} = -2.0mA (Note 4)
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 3.2mA (Note 4)
I_{CCR}	V_{CC} Read Current		60		110	mA	Min. cycle , I_{OUT} = 0mA
I_{CCW}	V_{CC} Write Current		40		70	mA	Write in progress
I_{CCE}	V_{CC} Erase Current		40		70	mA	Block (pair) Erase in progress
I_{CCES}	V_{CC} Erase Suspend Current		10		20	mA	Erase suspended
I_{CCS}	V_{CC} Standby Current		1.5		1.5	mA	CE1* = CE2* = V_{IH} or 覓$_{CC}$-0.2V
I_{PPR}	V_{PP} Read Current		0.8		1.0	mA	V_{PP} > V_{CC}
I_{PPW}	V_{PP} Write Current		30		60	mA	Write in progress
I_{PPE}	V_{PP} Erase Current		30		60	mA	Block (pair) Erase in progress
I_{PPES}	V_{PP} Erase Suspend Current		0.4		0.8	mA	Erase Suspended
I_{PPS}	V_{PP} Standby Current		30		30	uA	V_{PP} ™$_{CC}$
V_{PPL}	V_{PP} During Read Only Operation	0	6.5	0	6.5	V	
V_{PPH}	V_{PP} During Erase / Write Operation	11.4	12.6	11.4	12.6	V	

Table 11

Note : 1.) Except CE1* , CE2* , WE* , REG* pins.

2.) For CE1* , CE2* , WE* , REG* pins.

3.) Except BVD1* , BVD2* , CD1* , CD2* pins.

4.) Except CD1* , CD2* pins.

AC Electrical Characteristics

(recommended operating conditions unless otherwise noted)

Read Cycle (Common Memory)

Symbol		Parameter	Notes	Min	Max	Unit
t_{AVAV}	t_{RC}	Read Cycle Time		200		ns
t_{AVQV}	t_a (A)	Address Access Time			200	ns
t_{ELQV}	t_a (CE)	Card Enable Access Time			200	ns
t_{GLQV}	t_a (OE)	Output Enable Access Time			100	ns
t_{EHQX}	t_{dis} (CE)	Output Disable Time (CE*)			90	ns
t_{GHQZ}	t_{dis} (OE)	Output Disable Time (OE*)			90	ns
t_{GLQX}	t_{en} (CE)	Output Enable Time (CE*)		5		ns
t_{ELQX}	t_{en} (OE)	Output Enable Time (OE*)		5		ns
t_{AXQX}	t_v (A)	Data Valid from Address Change		0		ns

Table 12

Write Cycle (Common Memory)

Symbol		Parameter	Notes	Min	Max	Unit
t_{AVAV}	t_{wc}	Write Cycle Time		200		ns
t_{WLWH}	t_w (WE)	Write Pulse Width		100		ns
t_{AVWL}	t_{su} (A)	Address Setup Time		10		ns
t_{AVWH}	t_{su} (A-WEH)	Address Setup Time for WE*		140		ns
t_{VPWH}	t_{vps}	V_{PP} Setup to WE* Going High		100		ns
t_{ELWH}	t_{su} (CE-WEH)	Card Enable Setup Time for WE*		140		ns
t_{DVWH}	t_{su} (D-WEH)	Data Setup Time for WE*		60		ns
t_{WHDX}	t_h (D)	Data Hold Time		30		ns
t_{WHAX}	t_{rec} (WE)	Write Recover Time		30		ns
t_{WHRL}		WE High to RY/BY*			120	ns
t_{WHQV1}		Duration of Data Write Operation		6		us
t_{WHQV2}		Duration of Block Erase Operation		0.3		sec
t_{QVVL}		V_{PP} Hold from Operation Complete	2	0		ns
t_{WHGL}	t_h (OE-WE)	Write Recovery before Read		10		ns

Table 13

Notes :

1. Read timing characteristics during erase and data write operation are the same as during read-only operations. Refer to AC Characteristics for Read-Only operations.

Write Cycle (Common Memory) (CE* controlled)

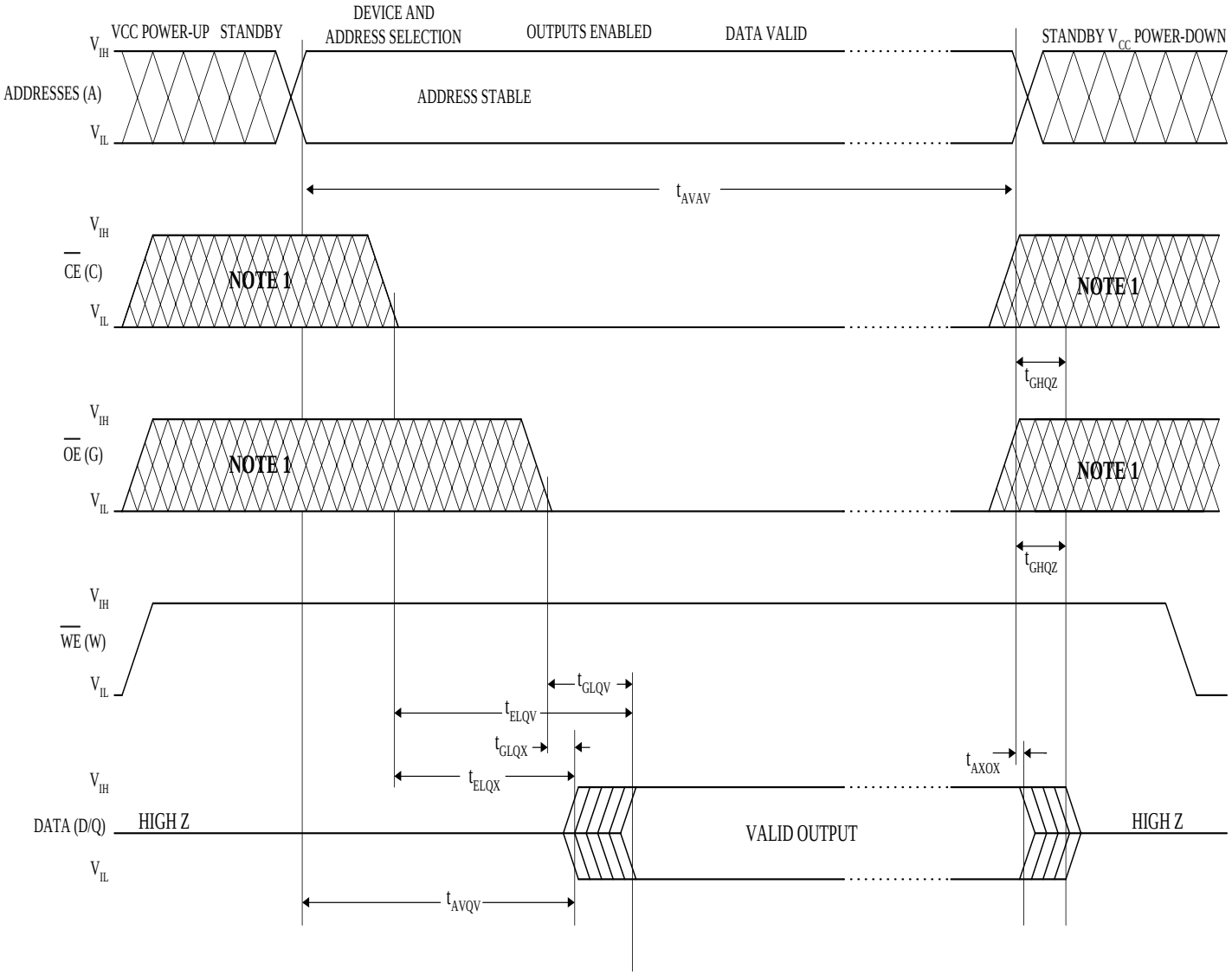
Symbol		Parameter	Notes	Min	Max	Unit
t_{AVAV}	t_{wc}	Write Cycle Time	1	200		ns
t_{ELEH}	t_w (WE)	Card Enable Pulse Width	1	120		ns
t_{AVEL}	t_{su} (A)	Address Setup Time	1	20		ns
t_{AVEH}	t_{su} (A-WEH)	Address Setup Time for CE*	1	140		ns
t_{VPEH}	t_{vps}	VPP Setup to CE* Going High	1	100		ns
t_{WLEH}	t_{su} (CE-WEH)	Write Enable Setup Time for CE*	1	140		ns
t_{DVEH}	t_{su} (D-WEH)	Data Setup Time for CE*	1	60		ns
t_{EHDX}	t_h (D)	Data Hold Time	1	30		ns
t_{EHAX}	t_{rec} (WE)	Write Recover Time	1	30		ns
t_{EHRL}		CE* High to RY/BY*	1		120	ns
t_{EHQV1}	Duration of Data Write	Duration of Data Write Operation	1	6		us
t_{EHQV2}	Duration of Erase	Duration of Block Erase Operation	1	0.3		sec
t_{QVVL}		V_{PP} Hold from Operation Complete	1,2	0		ns
t_{EHGL}	t_h (OE-WE)	Write Recovery before Read	1	10		ns

Table 14

Notes :

1. Read timing characteristics during erase and data write operation are the same as during read-only operations. Refer to AC Characteristics for Read-Only operations.
2. Refer to text on Data-Write and Block-Erase Operations.

Read Cycle Timing Diagram (Common Memory)



NOTE 1: The hatched area may be either high or low.

Figure 7

Write Cycle Timing Diagram (Common Memory)

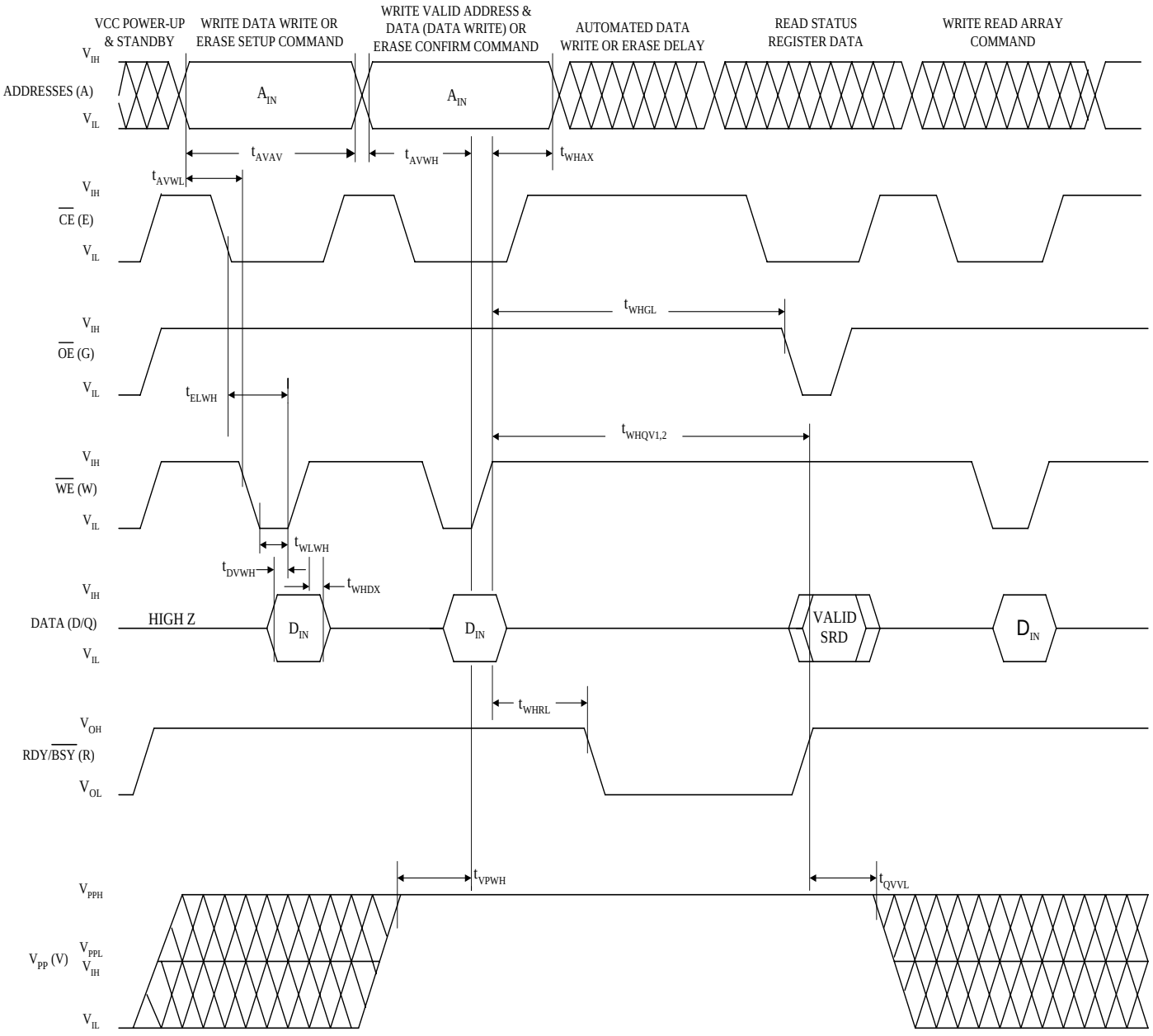


Figure 8

Write Cycle Timing Diagram (Common Memory)

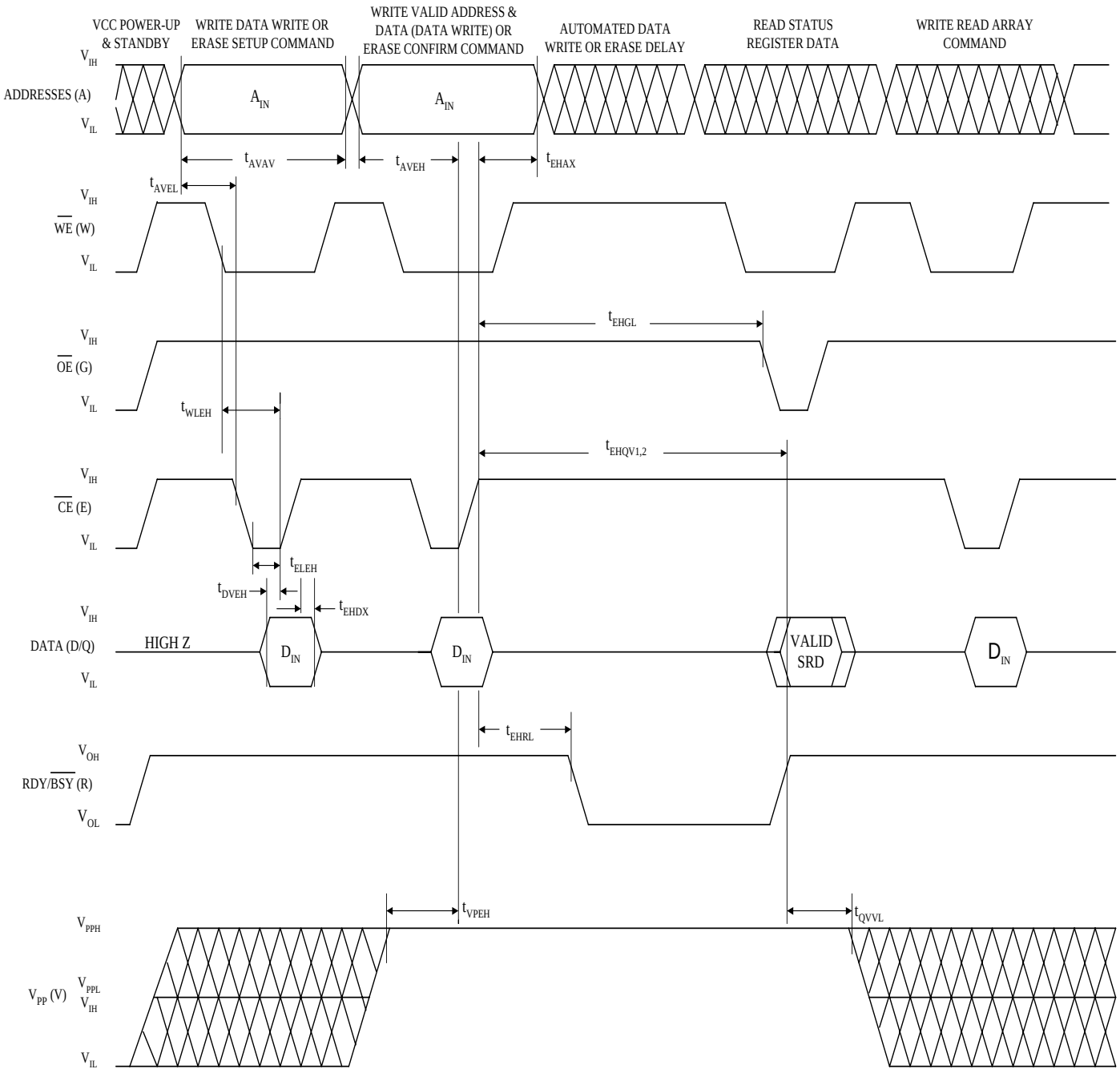


Figure 9

Block Erase and Data Write Performance

Parameter	Min.	Typ.	Max.	Unit	Notes
Block Pair Erase Time		1.6	10	sec	2
Block Pair Write Time		0.6	2.1	sec	2

Table 15

Notes :

1. Individual blocks can be erased 100000 times.
2. Excludes System-Level Overhead.
3. Typical condition is 25° C , 12.0V V_{PP}.

AC Electrical Characteristics (Attribute Memory)

(recommended operating conditions unless otherwise noted)

Read Cycle (Attribute Memory)

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{cr}	Read Cycle Time	300		ns	
$t_a(A)$	Address Access Time		300	ns	
$t_a(CE)$	Card Select Access Time		300	ns	
$t_a(OE)$	Output Enable Access Time		150	ns	
$t_{dis}(CE)$	Output Disable Time (from CE*)		100	ns	
$t_{dis}(OE)$	Output Disable Time (from OE*)		100	ns	
$t_{en}(CE)$	Output Enable Time (from CE*)	5		ns	
$t_{en}(OE)$	Output Enable Time (from OE*)	5		ns	
$t_v(A)$	Data Hold Time (from address changed)	0		ns	

Table 16

Write Cycle (Attribute Memory)

Symbol	Parameter	Min.	Max.	Unit	Test Condition
$t_{\mathbf{CW}}$	Write Cycle Time		1	ms	
$t_{\mathbf{AS}}$	Address Setup Time	30		ns	
$t_{\mathbf{AH}}$	Address Hold Time	50		ns	
$t_{\mathbf{WP}}$	Write Pulse Width	120		ns	
$t_{\mathbf{CS}}$	Card Enable Time to WE*	15		ns	
$t_{\mathbf{CH}}$	Card Enable Hold Time from WE* High	0		ns	
$t_{\mathbf{DS}}$	Data Setup Time	70		ns	
$t_{\mathbf{DH}}$	Data Hold Time	30		ns	
$t_{\mathbf{OES}}$	OE* Setup Time	30		ns	
$t_{\mathbf{OEH}}$	OE* Hold Time	30		ns	

Table 17

Read Cycle Timing Diagram (Attribute Memory) (REG*=VIL , WE*=VIH)

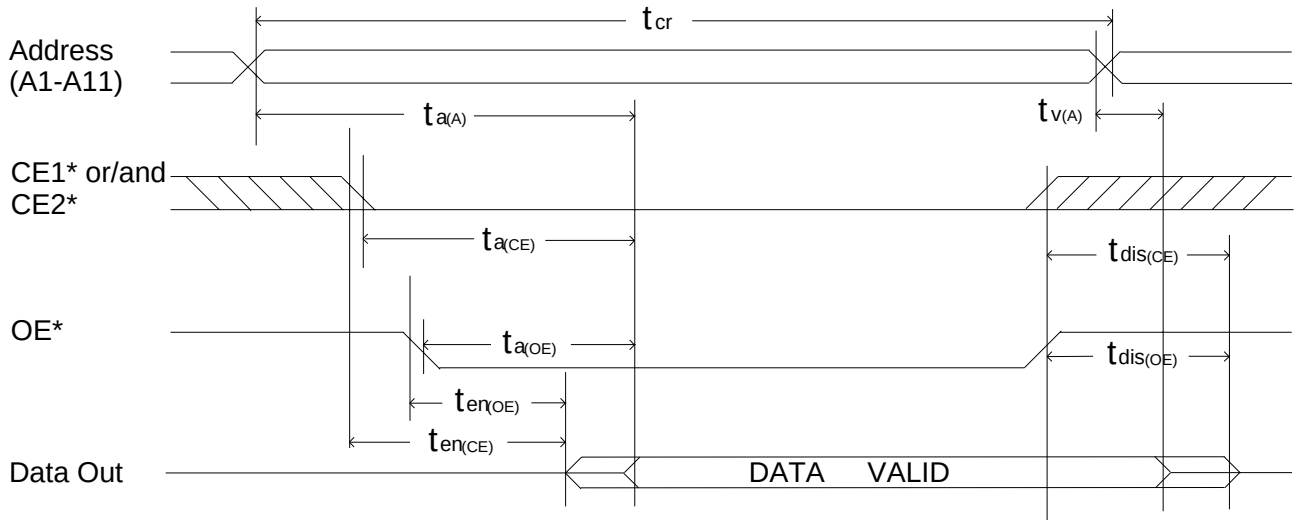


Figure 10

Write Cycle Timing Diagram (Attribute Memory) (REG*=VIL)

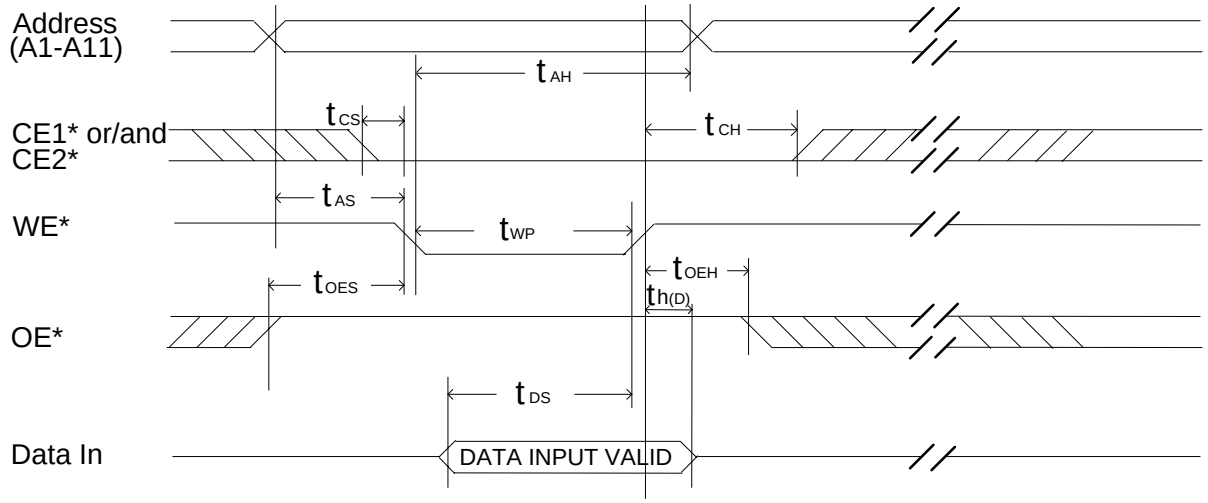
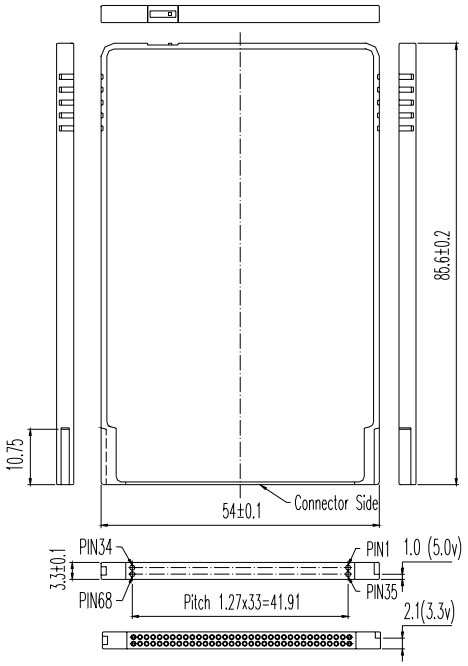
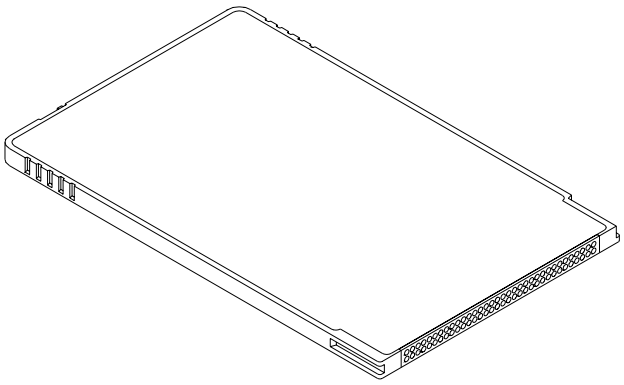


Figure 11

Outline Dimensions (Unit : mm)





FLASH CARD (Write Protect)