



Tiger Series MINI- IDE Flash Disk

Industrial Application

Product Specification V1.1

Dec 2008



Document History

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Contents

INDUSTRIAL APPLICATION	1
1. INTRODUCTION.....	7
1.1 GENERAL DESCRIPTION.....	7
1.2 FEATURES	8
2. PRODUCT SPECIFICATION.....	9
2.1 OPERATION AND ENVIRONMENT DESCRIPTION	9
2.2 PHYSICAL DESCRIPTION.....	10
3. PRODUCT MODEL.....	11
3.1 PART NUMBER DEFINITION	11
3.2 40/44-PIN MINI IDE PLAIN FORM PICTURES AND PART NUMBER	14
3.3 40-PIN MINI IDE L-FORM PICTURES AND PART NUMBER.....	14
3.4 44-PIN MINI IDE L-FORM PICTURES AND PART NUMBER.....	17
4. SUPPORT FLASH MEDIA	21
4.1 SUPPORTED NAND FLASH TYPE	21
4.2 LOGICAL FORMAT PARAMETERS (CHS).....	21
5. BLOCK DIAGRAM.....	22
5.1 CONTROLLER ARCHIVE.....	22
5.2 FLASH CARD ARCHIVE.....	22
6. SPECIFICATION AND FEATURES.....	23
6.1 ELECTRICAL SPECIFICATION	23
6.1.1 <i>Absolute Maximum Ratings</i>	23
6.1.2 <i>General DC Characteristic</i>	23
6.1.3 <i>DC Electrical Characteristics for 5 Volts Operation</i>	23
6.1.4 <i>DC Electrical Characteristics for 3.3 Volts Operation</i>	24
6.1.5 <i>True IDE Mode I/O (Read/Write) Timing Specification</i>	24
6.1.6 <i>True IDE Ultra DMA Mode I/O (Read/Write) Timing Specification</i>	25
6.1.6.1 Ultra DMA Data-In Burst Initiation Timing.....	26
6.1.6.2 Sustained Ultra DMA Data-In Burst Timing	27
6.1.6.3 Ultra DMA Data-In Burst Host Pause Timing.....	27
6.1.6.4 Ultra DMA Data-In Burst Device Termination Timing	28
6.1.6.5 Ultra DMA Data-In Burst Host Termination Timing	28
6.1.6.6 Ultra DMA Data-In Burst Host Termination Timing	29
6.1.6.7 Sustained Ultra DMA Data-Out Burst Timing	29
6.1.6.8 Ultra DMA Data-Out Burst Device Pause Timing.....	30



Tiger Series MINI-IDE Industrial Application

C-ONE TECHNOLOGY Corp.

6.1.6.9	Ultra DMA Data-Out Burst Device Termination Timing.....	30
6.1.6.10	Ultra DMA Data-Out Burst Host Termination Timing.....	31
6.2	POWER MANAGEMENT.....	31
6.2.1	Normal Mode.....	31
6.2.2	Power down Mode.....	31
6.3	PHYSICAL SPECIFICATION.....	32
6.3.1	MIDE 40 PIN P-FORM WITH HOUSING OUTLINE DIMENSIONS.....	32
6.3.2	MIDE 40 PIN L-FORM WITHOUT HOUSING OUTLINE DIMENSIONS.....	33
6.3.3	MIDE 44-PIN P-FORM WITH HOUSING OUTLINE DIMENSION.....	34
6.3.4	MIDE 44-PIN L-FORM WITHOUT HOUSING OUTLINE DIMENSIONS.....	35
7.	PIN ASSIGNMENT.....	36
7.1	PIN TYPE.....	36
7.2	INTERFACE SIGNALS DESCRIPTION.....	37
7.3	INSTALLING THE SSD DRIVE IN A TWO-DRIVE CONFIGURATION.....	39
8.	ATA SPECIFIC REGISTER DEFINITIONS.....	41
8.1	TRUE IDE MODE.....	41
8.2	ATA REGISTERS.....	41
8.2.1	Data Register.....	41
8.2.2	Error Register.....	42
8.2.3	Feature Register.....	42
8.2.4	Sector Count Register.....	42
8.2.5	Sector Number Register.....	43
8.2.6	Cylinder Low Register.....	44
8.2.7	Cylinder High Register.....	44
8.2.8	Drive Head Register.....	45
8.2.9	Status Register.....	46
8.2.10	Alternate Status Register.....	46
8.2.11	Device Control Register.....	47
8.2.12	Drive Address Register.....	47
9.	ATA COMMANDS.....	48
9.1	CHECK POWER MODE - 98H OR E5H.....	48
9.2	EXECUTE DRIVE DIAGNOSTIC - 90H.....	49
9.3	ERASE SECTOR(S) - C0H.....	50
9.4	FORMAT TRACK - 50H.....	51
9.5	IDENTIFY DRIVE - ECH.....	52
9.6	IDLE - 97H OR E3H.....	53
9.7	IDLE IMMEDIATE - 95H OR E1H.....	54
9.8	INITIALIZE DRIVE PARAMETERS - 91H.....	55
9.9	READ BUFFER - F4H.....	56



9.10	READ LONG SECTOR(S) - 22H OR 23H.....	57
9.11	READ MULTIPLE - C4H.....	58
9.12	READ SECTORS(S) – 20H OR 21H.....	59
9.13	READ VERIFY SECTOR(S) – 40H OR 41H.....	60
9.14	RECALIBRATE - 1XH.....	61
9.15	REQUEST SENSE - 03H.....	62
9.16	SEEK - 7XH.....	63
9.17	SET FEATURE - EFH.....	64
9.18	SET MULTIPLE MODE - C6H.....	65
9.19	SET SLEEP MODE - 99H OR E6H.....	66
9.20	STANDBY - 96H OR E2H.....	67
9.21	STANDBY IMMEDIATE 94H OR E0H.....	68
9.22	TRANSLATE SECTOR - 87H.....	69
9.23	WEAR LEVEL - F5H.....	70
9.24	WRITE BUFFER - E8H.....	71
9.25	WRITE LONG SECTOR(S) 32H OR 33H.....	72
9.26	WRITE MULTIPLE - C5H.....	73
9.27	WRITE MULTIPLE WITHOUT ERASE – CDH.....	74
9.28	WRITE SECTOR(S) - 30H OR 31H.....	75
9.29	WRITE SECTOR(S) WITHOUT ERASE - 38H.....	76
9.30	WRITE VERITY - 3CH.....	77
10.	ERROR POSTING.....	78
11.	IDENTIFY DRIVE INFORMATION.....	79
12.	ATA PROTOCOL OVERVIEW.....	84
12.1	PIO DATA IN COMMANDS.....	84
12.2	PIO DATA OUT COMMANDS.....	84
12.3	NON DATA COMMANDS.....	84
14.	ULTRA DMA DATA-IN COMMANDS.....	85
14.1.	INITIATING AN ULTRA DMA DATA-IN BURST.....	85
14.2.	THE DATA-IN TRANSFER.....	85
14.3.	PAUSING AN ULTRA DMA DATA-IN BURST.....	86
14.3.1.	Device pausing an Ultra DMA data-in burst.....	86
14.3.2.	Host pausing an Ultra DMA data-in burst.....	86
14.3.3.	Terminating an Ultra DMA data-in burst.....	86
14.3.3.1.	Device terminating an Ultra DMA data-in burst.....	86
14.3.3.2.	Host terminating an Ultra DMA data-in burst.....	87
14.4.	ULTRA DMA DATA-OUT COMMANDS.....	89
14.4.1.	Initiating an Ultra DMA data-out burst.....	89
14.4.2.	The data-out transfer.....	89



Tiger Series MINI-IDE Industrial Application

C-ONE TECHNOLOGY Corp.

14.4.3. Pausing an Ultra DMA data-out burst.....	90
14.4.3.1 Host pausing an Ultra DMA data-out burst.....	90
14.4.4. Terminating an Ultra DMA data-out burst.....	90
14.4.4.1 Host terminating an Ultra DMA data-out burst.....	90
14.4.4.2 Device terminating an Ultra DMA data-out burst.....	91
14.5. ULTRADMA CRC RULES.....	92
15.SYSTEM ENVIRONMENTAL SPECIFICATIONS.....	94
15.1 TEMPERATURE TEST FLOW.....	94
15.2 ALTITUDE TEST.....	95



1. Introduction

1.1 General Description

C-ONE's Tiger series MINI- IDE Card uses NAND-Type flash memory devices, which leads to its remarkable high performance and comes with capacities from 128 MB to 48GB unformatted.

Compliant with ISA (Industrial Standard Architecture) bus interface standard, the S-CN IDE Card performs sequential read/write for each sector (512 bytes) count. It also conforms to IDE Specification and is designed with precision mechanics to enable host devices to read/write from the IDE interface into Flash Media. It can operate with a 5V single power from the host side.

The card provides extraordinary memory medium for PC , C-ONE's IDE Card has been approved through various compatibility tests.



1.2 Features

- ✧ IDE interface
 - ATA command set compatible
 - Support for 8-bit or 16-bit host data transfer
 - Program and auto-wait-state initiation for compatibility with any IORDY supporting host
 - Compatibility with host ATA disk I/O BIOS, DOS/Windows file system, utilities, and application software
- ✧ Extremely rugged and reliable
 - Advanced defect block management
 - Support background erased operation
- ✧ 5 Volt power supply, very low power consumption
 - Internal self-diagnostic program operates at V_{CC} power on
 - Auto sleep mode
- ✧ High reliability based on internal ECC (Error Correcting Code) function
- ✧ Error Correcting of 4 bits random error per sector
- ✧ Automatic on-the-fly, in-buffer Error Correcting
- ✧ Zero-power data retention, no batteries required
- ✧ 3 variations of mode access
 - Memory card mode
 - I/O card mode
 - True IDE mode
 - PIO Mode 4
 - UDMA mode 4
 - supported Multi word DMA Mode 2 .

2. Product Specification

2.1 Operation and environment description

Operating Voltage	DC Input Power	5V ± 10%	
Typical Power Consumptions:	5V	Read Mode: 40 mA(Max)	
		Write Mode: 60 mA(Max)	
		Standby Mode: 6.5 mA(Approach values)	
		Read/ Write Peak: 100mA	
Environment conditions	Operating Temperature	Extended Temp.	-20°C to +85°C
		Industrial Temp.	-40°C to +85°C
	Storage Temperature	Extended Temp.	-40°C to +90°C
		Industrial Temp.	-50°C to +90°C
	Humidity Operation	5% to 95% (Non-condensing)	
	Humidity Non-operation	5% to 95% (Non-condensing)	
	Shock Operation	3000-G (Max.)	
	Shock Non-operation	3000-G (Max.)	
	Vibration Operation	30-G (Peak to peak to maximum)	
Vibration Non-operation	30-G (Peak to peak to maximum)		
Operation System supported Compatibility (Microsoft Product)	DOS		
	Windows 98	Windows Vista	
	Windows NT	Windows 2000	Windows XP

2.2 Physical description

1. Weight and Measures (unit: mm)	MIDE 40-Pin (P or L form)	Weight: 12 g
		Pin-pitch: 2.54 mm
	MIDE 44-Pin (P or L form)	Weight: 12 g
		Pin-pitch: 2.0 mm
2. Storage Capacities	Capacity	256MB to 8GB
3. Performance:	Data Transfer Rates	Read speed up to 35 Mbytes/sec (Max)
		Write speed up to 32 Mbytes/sec (Max)
	Data Access Time	<1.5 ms
4. Reliability:	MTBF	3,000,000 power-on hours
	Error Rate	Less than 1 bit error in 10^{14} bits read (Min.)
	ECC	Error Correcting of 4 bits random error per sector
	Endurance	3,000,000 Write/Erase cycle



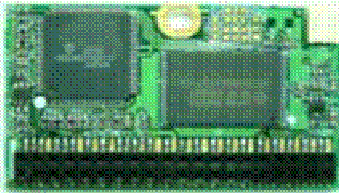
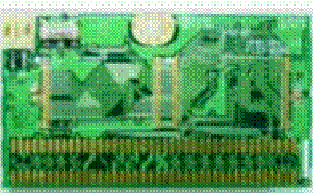
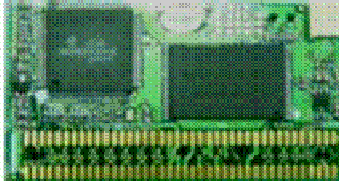
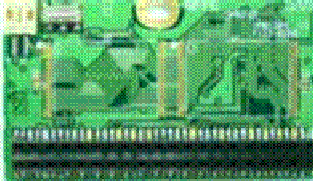
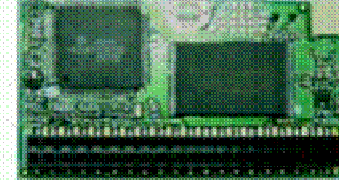
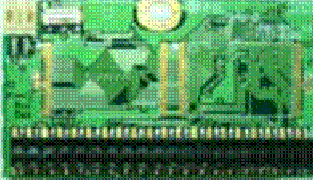
3. Product Model

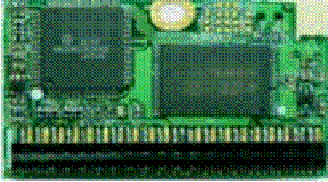
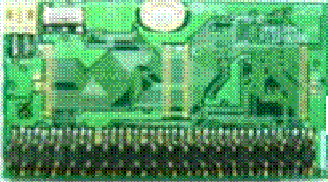
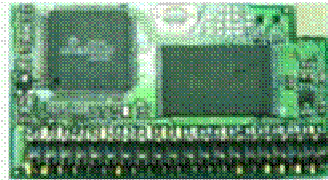
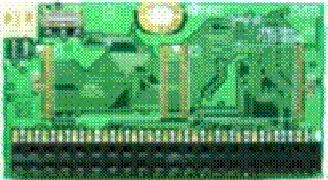
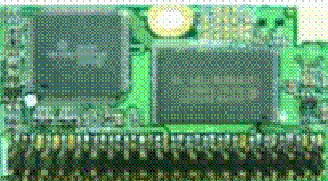
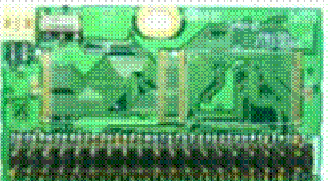
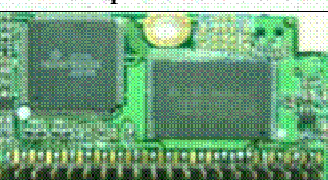
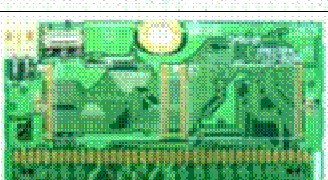
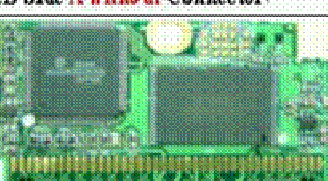
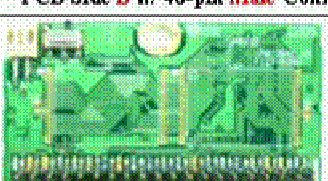
3.1 Part Number Definition

X₁X₂X₃X₄X₅X₆X₇X₈



Code	Definition	symbol	Description
X1X2	Card Type	IA	40-pin Mini IDE
		IB	44-pin Mini IDE
X3	Solution	M	Tiger Series
X4X5X6	Capacity	256	256MB
		512	512MB
		01G	1GB
		02G	2GB
		04G	4GB
		08G	8GB
X7	Temperature Range	C	Commerical Grade 0 ~ 70
		L	Light Grade -20 ~ 85
		H	Heavy Grade -40 ~ 85
X8	Appearance	Please see below	

X8	Plain-Form Housing	L-form withouthousing
power cable	0	1~8
20 pin support 5V	A	B~I

Part Number ^①	PCB Side A w/ 40-pin Female Connector ^②	PCB Side B without Connector
IAXXXX-X1 IAXXXX-XB		
Part Number ^①	PCB Side A without Connector ^②	PCB Side B w/ 40-pin Female Connector ^③
IAXXXX-X2 IAXXXX-XC		
Part Number ^①	PCB Side A w/ 40-pin Female Connector ^②	PCB Side B w/ 40-pin Female Connector ^③
IAXXXX-X3 IAXXXX-XD		

Part Number ^①	PCB Side A w/ 40-pin Female Connector ^②	PCB Side B w/ 40-pin Male Connector ^③
IAXXXX-X4 IAXXXX-XE		
Part Number ^①	PCB Side A w/ 40-pin Male Connector ^②	PCB Side B 40-pin Female Connector ^③
IAXXXX-X5 IAXXXX-XF		
Part Number ^①	PCB Side A w/ 40-pin Male Connector ^②	PCB Side B w/ 40-pin Male Connector ^③
IAXXXX-X6 IAXXXX-XG		
Part Number ^①	PCB Side A w/ 40-pin Male Connector ^②	PCB Side B without Connector ^③
IAXXXX-X7 IAXXXX-XH		
Part Number ^①	PCB Side A without Connector ^②	PCB Side B w/ 40-pin Male Connector ^③
IAXXXX-X8 IAXXXX-XI		

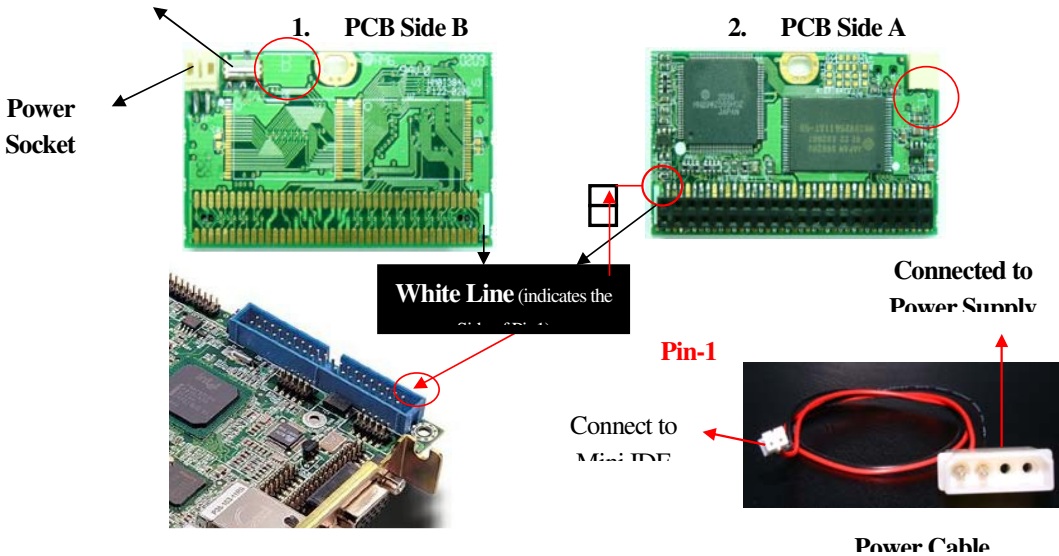
3.2 40/44-Pin Mini IDE Plain Form Pictures and Part Number

40-pin Mini IDE Plain Form		44-pin Mini IDE Plain Form	
			
Cheetah Pro Solution Supports Commercial Temperature 0°C ~ +70°C Supports Wide Temperature -20°C ~ +85°C			
Mini IDE	40-pin Plain Form		44pin Plain Form
Capacity	W/ 4-pin Power Cable	Support +5Vcc on-pin 20	Support Vcc power in
128MB-48GB	IANXXX-C0 IANXXX-L0	IANXXX-CA IANXXX-LA	IBNXXX-CA IBNXXX-LA






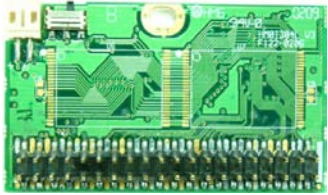
3.3 40-pin Mini IDE L-Form Pictures and Part Number

IANXXX-C1 (Standard Model)

Switch for Master/Slave

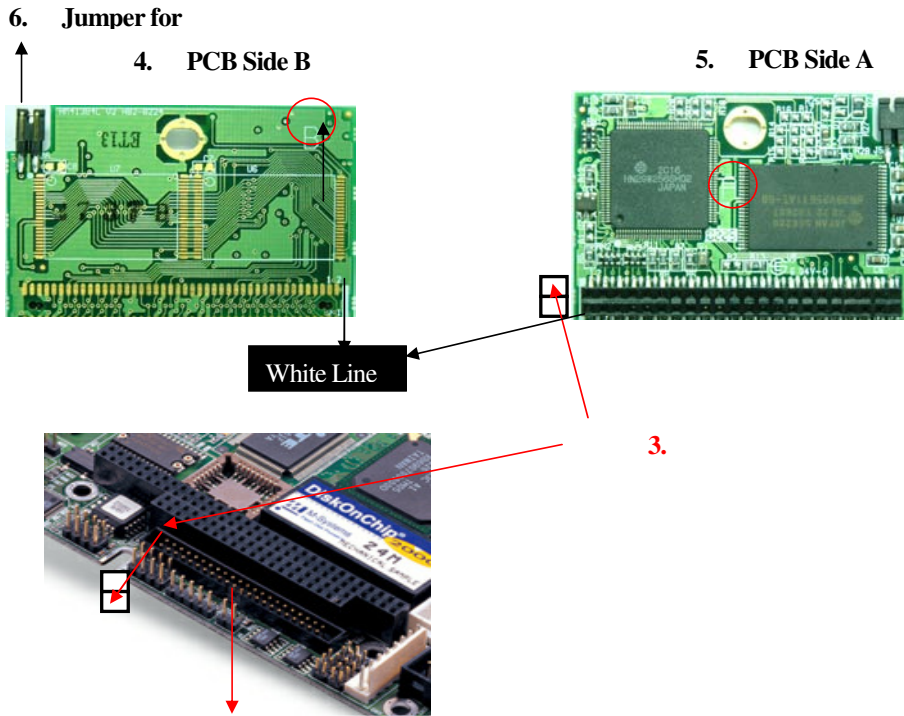


Part Number	PCB Side A w/ 40-pin Female Connector	PCB Side B without Connector
IANXXX-C/L/H 1	 P-1	
Part Number	PCB Side A without Connector	PCB Side B w/ 40-pin Female Connector
IANXXX-C/L/H 2		 P-1
Part Number	PCB Side A w/ 40-pin Female Connector	PCB Side B w/ 40-pin Female Connector
IANXXX-C/L/H 3	 P-1	 P-1
Part Number	PCB Side A w/ 40-pin Female Connector	PCB Side B w/ 40-pin Male Connector
IANXXX-C/L/H 4	 P-1	 P-1
Part Number	PCB Side A w/ 40-pin Male Connector	PCB Side B 40-pin Female Connector
IANXXX-C/L/H 5	 P-1	 P-1
Part Number	PCB Side A w/ 40-pin Male Connector	PCB Side B w/ 40-pin Male Connector

<p style="text-align: center;">IANXXX -C/L/H6</p>	<div style="display: flex; align-items: center; justify-content: center;"> <div style="border: 1px solid black; padding: 2px; margin-right: 5px;">P-1</div>  </div>	<div style="display: flex; align-items: center; justify-content: center;">  <div style="border: 1px solid black; padding: 2px; margin-left: 5px;">P-1</div> </div>
<p style="text-align: center;">Part Number</p>	<p style="text-align: center;">PCB Side A w/ 40-pin Male Connector</p>	<p style="text-align: center;">PCB Side B without Connector</p>
<p style="text-align: center;">IANXXX -C/L/H7</p>	<div style="display: flex; align-items: center; justify-content: center;"> <div style="border: 1px solid black; padding: 2px; margin-right: 5px;">P-1</div>  </div>	<div style="display: flex; align-items: center; justify-content: center;">  </div>
<p style="text-align: center;">Part Number</p>	<p style="text-align: center;">PCB Side A without Connector</p>	<p style="text-align: center;">PCB Side B w/ 40-pin Male Connector</p>
<p style="text-align: center;">IANXXX -C/L/H8</p>		<div style="display: flex; align-items: center; justify-content: center;">  <div style="border: 1px solid black; padding: 2px; margin-left: 5px;">P-1</div> </div>

3.4 44-pin Mini IDE L-Form Pictures and Part Number

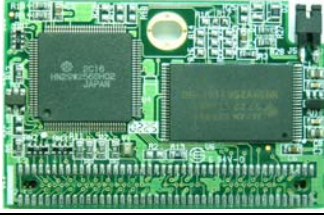
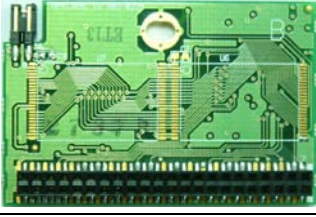

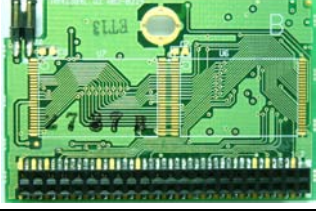
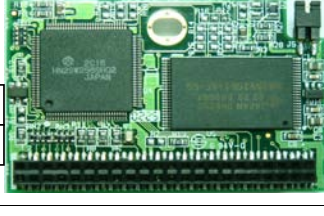
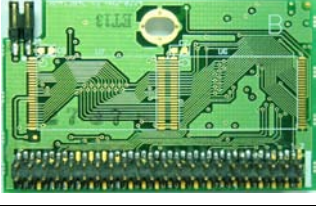


IBNXXX-CB (Standard Model)


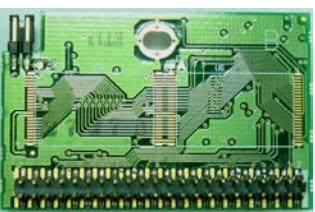


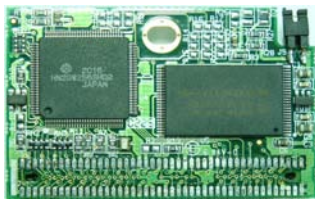
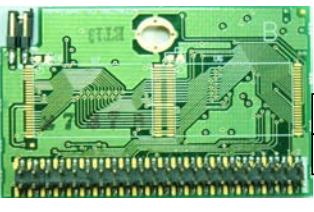


Key-pin for Safety Plug-in

Part Number	PCB Side A w/ 40-pin Female Connector	PCB Side B without Connector
IBNXXX-C/L/HB		

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Part Number	PCB Side A without Connector	PCB Side B w/ 44-pin Feale Connector
IBNXXX-C/L/H C		 <div style="border: 1px solid black; width: 30px; height: 20px; margin-left: 10px; margin-top: 10px; text-align: center; font-size: 8px;">P-1</div>
Part Number	PCB Side A with 44-pin Feale Connector	PCB Side B w/ 44-pin Female Connector
IBNXXX-C/L/H D	<div style="border: 1px solid black; width: 30px; height: 20px; margin-right: 10px; margin-bottom: 10px; text-align: center; font-size: 8px;">P-1</div> 	 <div style="border: 1px solid black; width: 30px; height: 20px; margin-left: 10px; margin-top: 10px; text-align: center; font-size: 8px;">P-1</div>
Part Number	PCB Side A w/ 44-pin Female Connector	PCB Side B w/ 44-pin Male Connector
IBNXXX-C/L/H E	<div style="border: 1px solid black; width: 30px; height: 20px; margin-right: 10px; margin-bottom: 10px; text-align: center; font-size: 8px;">P-1</div> 	 <div style="border: 1px solid black; width: 30px; height: 20px; margin-left: 10px; margin-top: 10px; text-align: center; font-size: 8px;">P-1</div>
Part Number	PCB Side A w/ 44-pin Male Connector	PCB Side B w/ 44-pin Female Connector
IBNXXX-C/L/H F	<div style="border: 1px solid black; width: 30px; height: 20px; margin-right: 10px; margin-bottom: 10px; text-align: center; font-size: 8px;">P-1</div> 	 <div style="border: 1px solid black; width: 30px; height: 20px; margin-left: 10px; margin-top: 10px; text-align: center; font-size: 8px;">P-1</div>

Part Number	PCB Side w/ 44-pin Male Connector	PCB Side B w/ 44-pin Male Connector
IBNXXX -C/L/HG		
Part Number	PCB Side w/ 44-pin Male Connector	PCB Side B without Connector
IBNXXX -C/L/HH		
Part Number	PCB Side A without Connector	PCB Side B w/ 40-pin Male Connector
IBNXXX -C/L/HI		

Cheetah Pro Solution			
Supports Commercial Temperature 0°C ~ +70°C			
Supports Wide Temperature -20°C ~ +85°C			
Mini IDE	40-pin L-form		44-pin L-form
Connector Type	W/ 4-pin Power Cable	Support +5Vcc on-pin 20	Support Vcc power in
1	IANXXX-C1	IANXXX-CB	IBNXXX-CB
	IANXXX-L1	IANXXX-LB	IBNXXX-LB
	IANXXX-H1	IANXXX-HB	IBNXXX-HB
2	IANXXX-C2	IANXXX-CC	IBNXXX-CC
	IANXXX-L2	IANXXX-LC	IBNXXX-LC
	IANXXX-H2	IANXXX-HC	IBNXXX-HC
3	IANXXX-C3	IANXXX-CD	IBNXXX-CD
	IANXXX-L3	IANXXX-LD	IBNXXX-LD
	IANXXX-H3	IANXXX-HD	IBNXXX-HD
4	IANXXX-C4	IANXXX-CE	IBNXXX-CE
	IANXXX-L4	IANXXX-LE	IBNXXX-LE
	IANXXX-H4	IANXXX-HE	IBNXXX-HE



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5	IANXXX-C5 IANXXX-L5 IANXXX-H5	IANXXX-CF IANXXX-LF IANXXX-HF	IBNXXX-CF IBNXXX-LF IBNXXX-HF
6	IANXXX-C6 IANXXX-L6 IANXXX-H6	IANXXX-CG IANXXX-LG IANXXX-HG	IBNXXX-CG IBNXXX-LG IBNXXX-HG
7	IANXXX-C7 IANXXX-L7 IANXXX-H7	IANXXX-CH IANXXX-LH IANXXX-HH	IBNXXX-CH IBNXXX-LH IBNXXX-HH
8	IANXXX-C8 IANXXX-L8 IANXXX-H8	IANXXX-CI IANXXX-LI IANXXX-HI	IBNXXX-CI IBNXXX-LI IBNXXX-HI



4. Support Flash Media

4.1 Supported NAND Flash Type

4-1-1. Single Level Cell (SLC) NAND Flash

Unit: bits

Flash Capacity	1Giga	2Giga	4Giga	8Giga	16Giga	32Giga	64Giga
Operation Voltage	3.3V						

4-1-2. Multi Level Cell (MLC) NAND Flash

Unit: bits

Flash Capacity	2Giga	4Giga	8Giga	16Giga	32Giga	64Giga	128Giga
Operation Voltage	3.3V						

4.2 Logical Format Parameters (CHS)

✧ Card Capacity

Unit: Bytes

Card Density ^{*4}	128M	256M	512M	1GB	2GB	3GB
Cylinder	251	503	1007	2015	4030	6046
Heads	16	16	16	16	16	16
Sectors/Track ^{*2}	63	63	63	63	63	63
Total Sectors/Card ^{*3}	253,008	507,024	1,006,992	2,014,992	4,029,984	6,044,976
Capacity ^{*5}	129,540,096	259,596,288	515,579,904	1,031,675,904	2,063,351,808	3,095,027,712

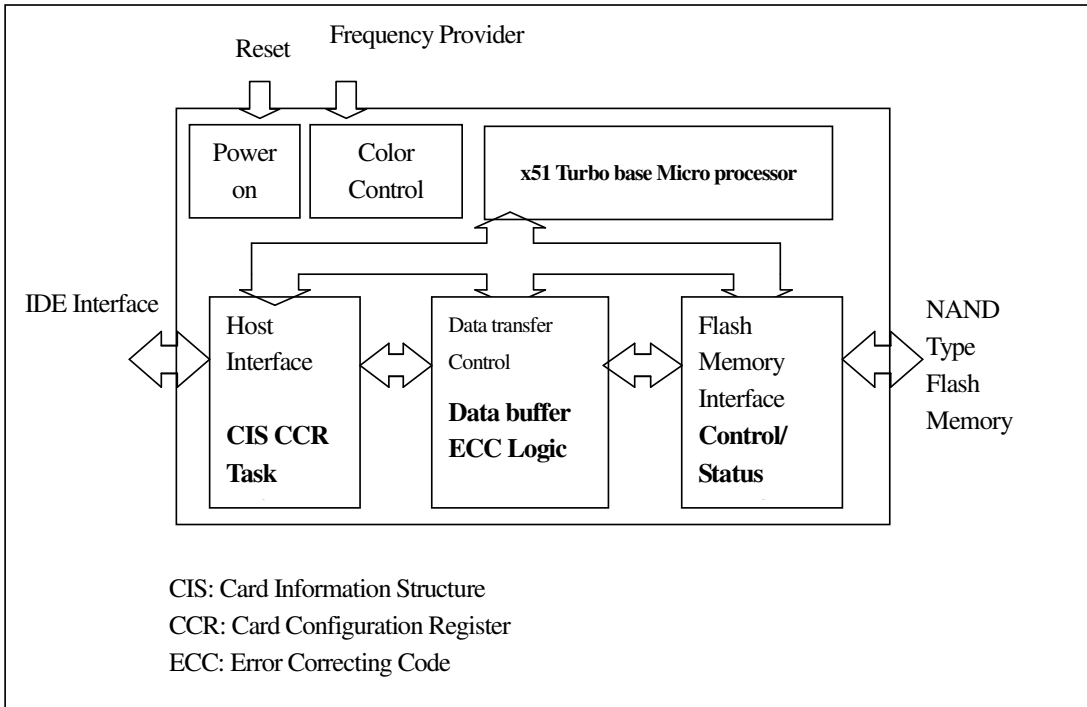
Unit: Bytes

Card Density ^{*4}	4GB	8GB	16GB	32GB	48GB
Cylinder	8060	16120	32240	64480	96720
Heads	16	16	16	16	16
Sectors/Track ^{*2}	63	63	63	63	63
Total Sectors/Card ^{*3}	8,059,968	16,119,936	32,239,872	64,479,744	96,719,616
Capacity ^{*5}	4,126,703,616	8,253,407,232	16,506,814,464	33,013,628,928	49,520,443,938

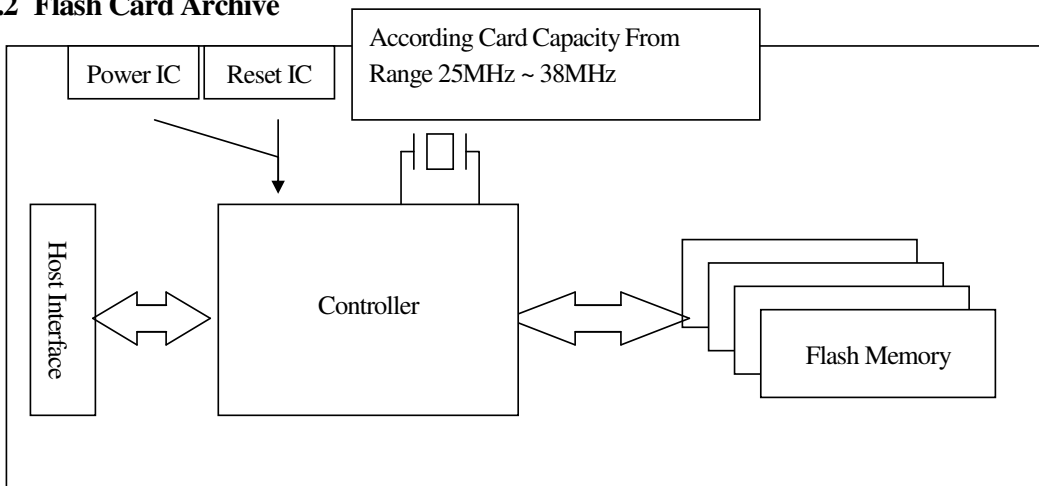
PS. Only supplies the references, all take material product

5. Block Diagram

5.1 Controller Archive



5.2 Flash Card Archive



6. Specification and Features

6.1 Electrical Specification

6.1.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Power supply	-0.3 to 6	V
V_{IN}	Input voltage	-0.3 to $V_{CC}+0.3$	V
V_{OUT}	Output voltage	-0.3 to $V_{CC}+0.3$	V
T_{STG}	Storage temperature	-50 to 90	°C
T_{opr}	Operating temperature	-40 to 85	°C

6.1.2 General DC Characteristic

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	Input capacitance				15	pF
C_{OUT}	Output capacitance				15	pF

6.1.3 DC Electrical Characteristics for 5 Volts Operation

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Input voltage		0		V_{CC}	V
V_{CC}	Power supply		4.5	5.0	5.5	V
T_{STG}	Storage temperature		-50		90	°C
T_{OPR}	Operating temperature		-40		85	°C
V_{IL}	Input low voltage	CMOS			0.8	V
V_{IH}	Input high voltage	CMOS	2.4			V
V_{OL}	Output low voltage	$I_{OL}=8mA$			0.4	V
V_{OH}	Output high voltage	$I_{OH}=-8mA$	$V_{CC}-0.8$			V

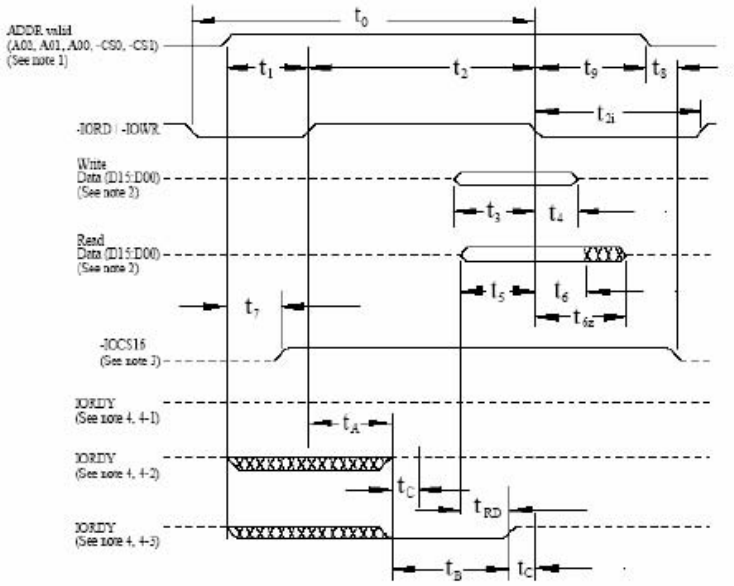


6.1.4 DC Electrical Characteristics for 3.3 Volts Operation

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{IN}	Input voltage		0		V _{CC}	V
V _{DD}	Power supply		3.0	3.3	3.6	V
T _{STG}	Storage temperature		-50		90	°C
T _{OPR}	Operating temperature		-40		85	°C
V _{IL}	Input low voltage	CMOS			0.6	V
V _{IH}	Input high voltage	CMOS	2.4			V
V _{OL}	Output low voltage	I _{OL} =8mA			0.4	V
V _{OH}	Output high voltage	I _{OH} =-8mA	V _{DD} -0.8			V

6.1.5 True IDE Mode I/O (Read/Write) Timing Specification

True IDE Mode I/O (Read/Write Timing Specification)	item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
		(ns)	(ns)	(ns)	(ns)	(ns)
t ₀	Cycle time (min)	600	383	240	180	120
t ₁	Address Valid to -IORD/-IOWR setup (min)	70	50	30	30	25
t ₂	-IORD/-IOWR (min)	165	125	100	80	70
t ₂	-IORD/-IOWR (min) Register (8 bit)	290	290	290	80	70
t _{2i}	-IORD/-IOWR recovery time (min)	-	-	-	70	25
t ₃	-IOWR data setup (min)	60	45	30	30	20
t ₄	-IOWR data hold (min)	30	20	15	10	10
t ₅	-IORD data setup (min)	50	35	20	20	20
t ₆	-IORD data hold (min)	5	5	5	5	5
t _{6Z}	-IORD data tristate (max)	30	30	30	30	30
t ₇	Address valid to -IOCS16 assertion (max)	90	50	40	n/a	n/a
t ₈	Address valid to -IOCS16 released (max)	60	45	30	n/a	n/a
t ₉	-IORD/-IOWR to address valid hold	20	15	10	10	10
t _{RD}	Read Data Valid to IORDY active (min), if IORDY initially low after t _A	0	0	0	0	0
t _A	t _A IORDY Setup time	35	35	35	35	35
t _B	IORDY Pulse Width (max)	1250	1250	1250	1250	250

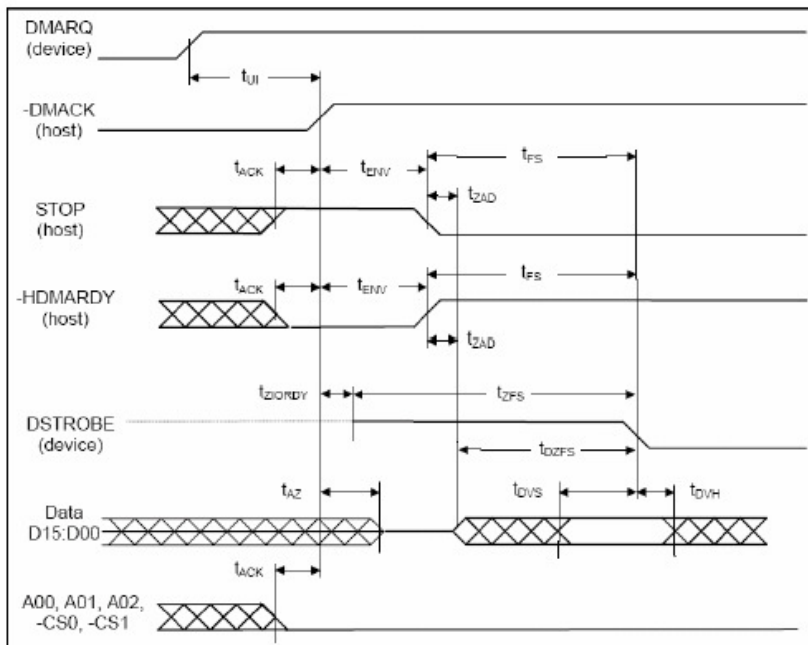


6.1.6 True IDE Ultra DMA Mode I/O (Read/Write) Timing Specification

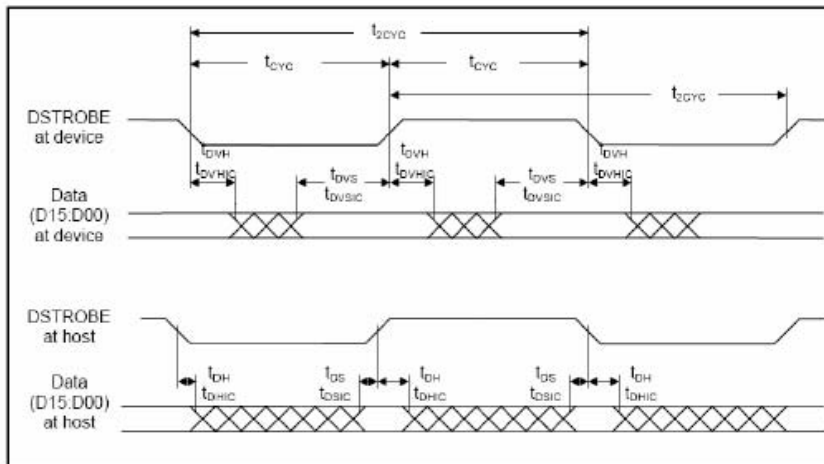
Name	UDMA Mode 0 (ns)		UDMA Mode 1 (ns)		UDMA Mode 2 (ns)		UDMA Mode 3 (ns)		UDMA Mode 4 (ns)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t2CYCTYP	240		160		120		90		60	
CYC	112		73		54		39		25	
t2CYC	230		153		115		86		57	
tDS	15.0		10.0		7.0		7.0		5.0	
tDH	5.0		5.0		5.0		5.0		5.0	
tDVS	70.0		48.0		31.0		20.0		6.7	
tDVH	6.2		6.2		6.2		6.2		6.2	
tCS	15.0		10.0		7.0		7.0		5.0	
tCH	5.0		5.0		5.0		5.0		5.0	
tCVS	70.0		48.0		31.0		20.0		6.7	
tCVH	6.2		6.2		6.2		6.2		6.2	
tZFS	0		0		0		0		0	
tDZFS	70.0		48.0		31.0		20.0		6.7	
tFS		230		200		170		130		120
tLI	0	150	0	150	0	150	0	100	0	100

Name	UDMA Mode 0 (ns)		UDMA Mode 1 (ns)		UDMA Mode 2 (ns)		UDMA Mode 3 (ns)		UDMA Mode 4 (ns)	
tMLI	20		20		20		20		20	
tUI	0		0		0		0		0	
tAZ		10		10		10		10		10
tZAH	20		20		20		20		20	
tZAD	0		0		0		0		0	
tENV	20	70	20	70	20	70	20	55	20	55
tRFS	75		70		60		60		60	
tRP	160		125		100		100		100	
tIORDYZ		20		20		20		20		20
tZIORDY	0		0		0		0		0	
tACK	20		20		20		20		20	
tSS	50		50		50		50		50	

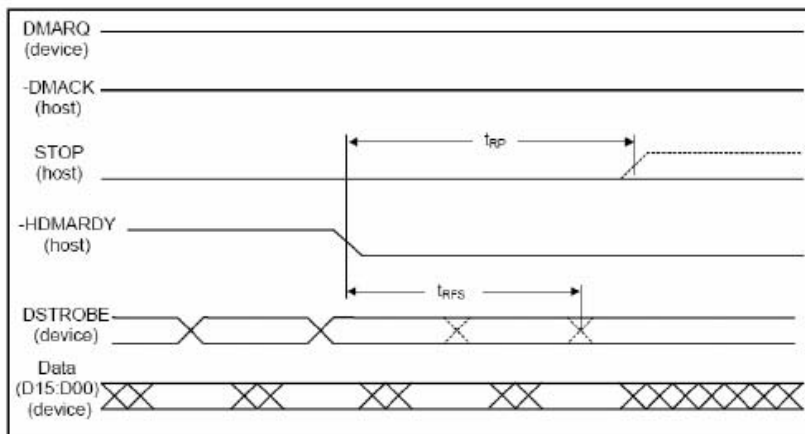
6.1.6.1 Ultra DMA Data-In Burst Initiation Timing



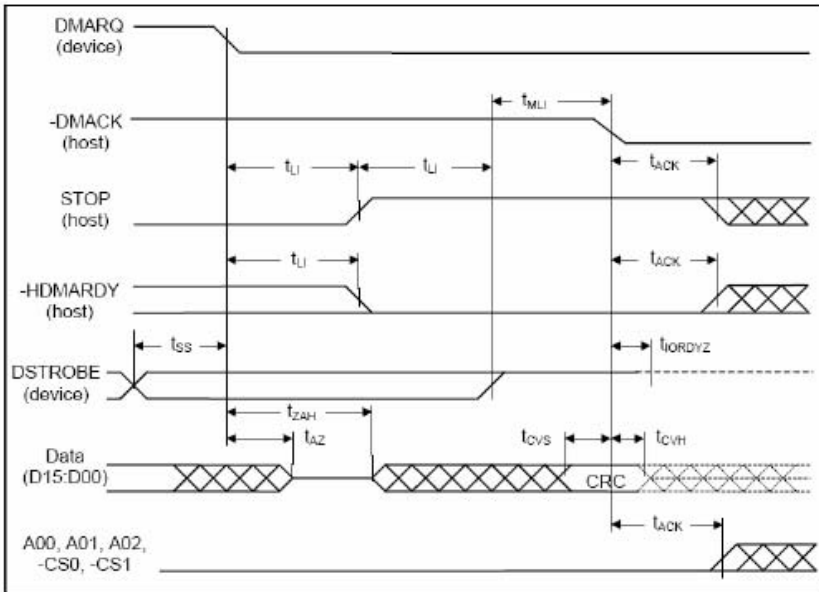
6.1.6.2 Sustained Ultra DMA Data-In Burst Timing



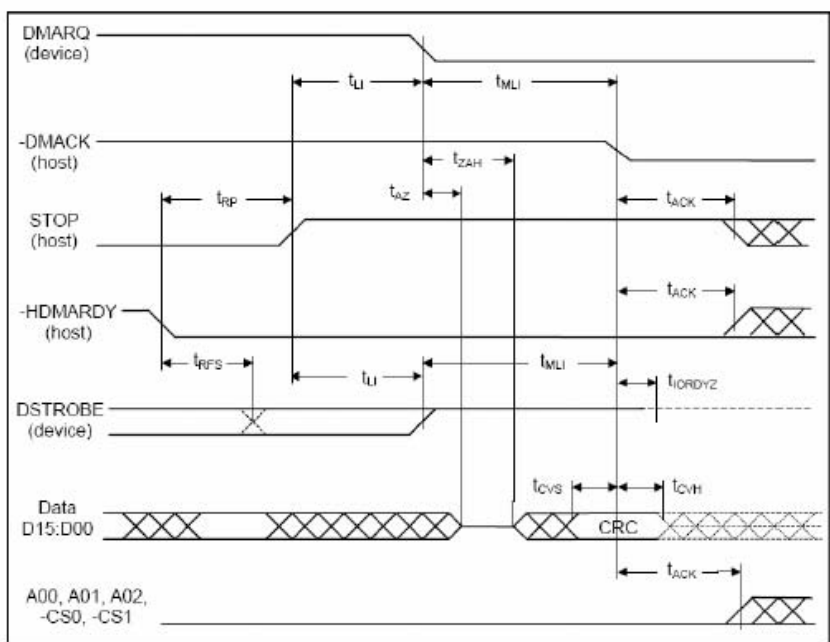
6.1.6.3 Ultra DMA Data-In Burst Host Pause Timing



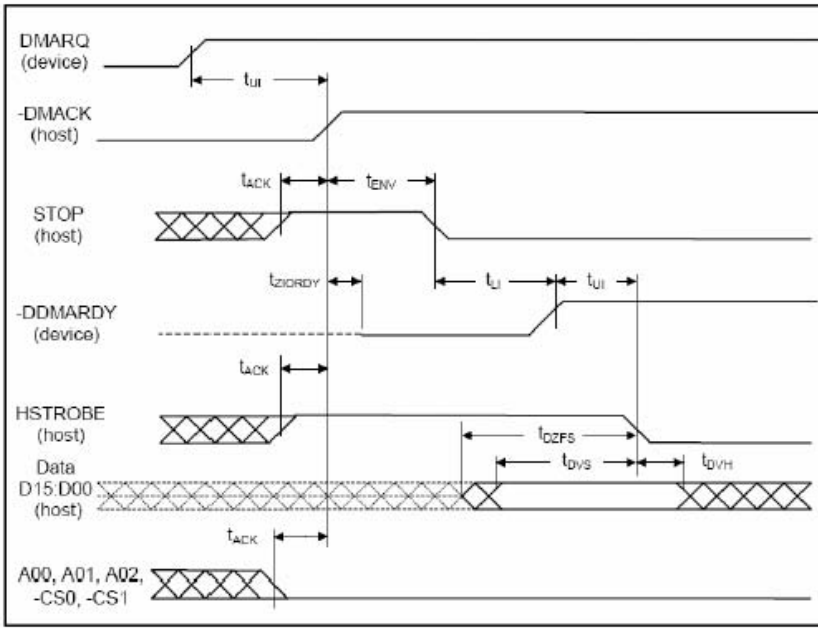
6.1.6.4 Ultra DMA Data-In Burst Device Termination Timing



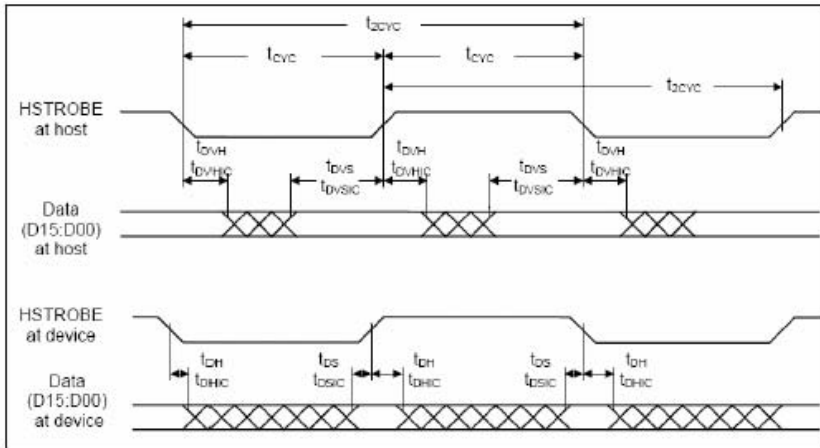
6.1.6.5 Ultra DMA Data-In Burst Host Termination Timing



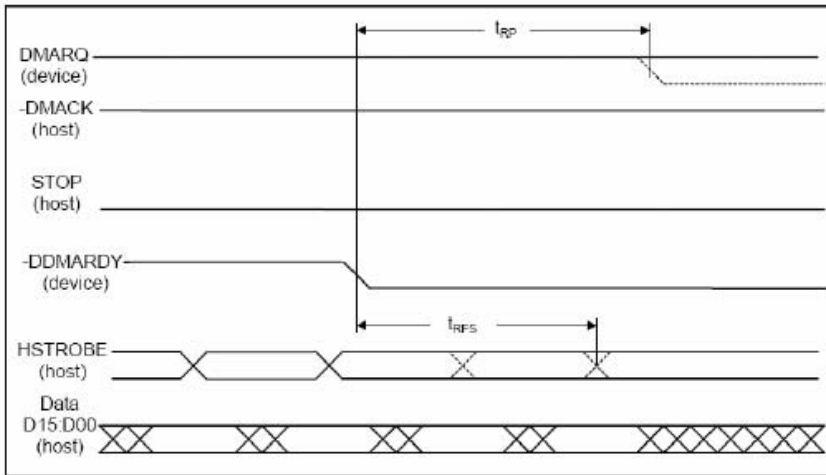
6.1.6.6 Ultra DMA Data-In Burst Host Termination Timing



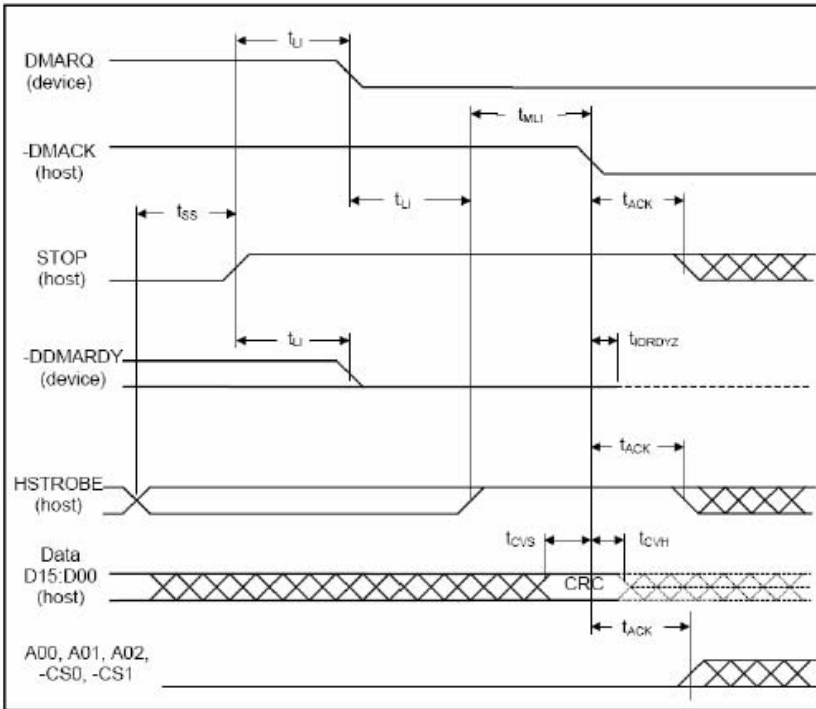
6.1.6.7 Sustained Ultra DMA Data-Out Burst Timing



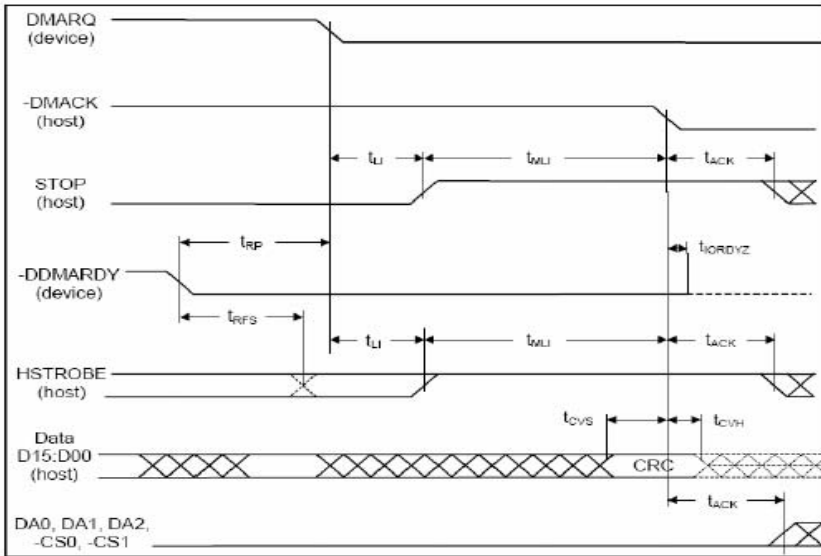
6.1.6.8 Ultra DMA Data-Out Burst Device Pause Timing



6.1.6.9 Ultra DMA Data-Out Burst Device Termination Timing



6.1.6.10 Ultra DMA Data-Out Burst Host Termination Timing



6.2 Power Management

6.2.1 Normal Mode

The host can reduce the power consumption of the card by changing its status with the following Power Command.

Sleep mode consumes the lowest power. Response time for the card to change from sleep mode to the active state is about 30 ms or less.

Standby mode, the response time is about 5ms or less. This is due to the interface of the card that accepts the command although can't access the media immediately

Idle mode, the card can respond and access the media immediately. The card needs longer time in this mode than in its active mode in order to active several circuits that were not used in the active mode.

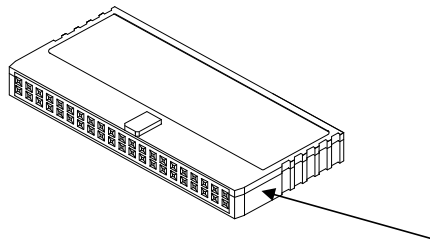
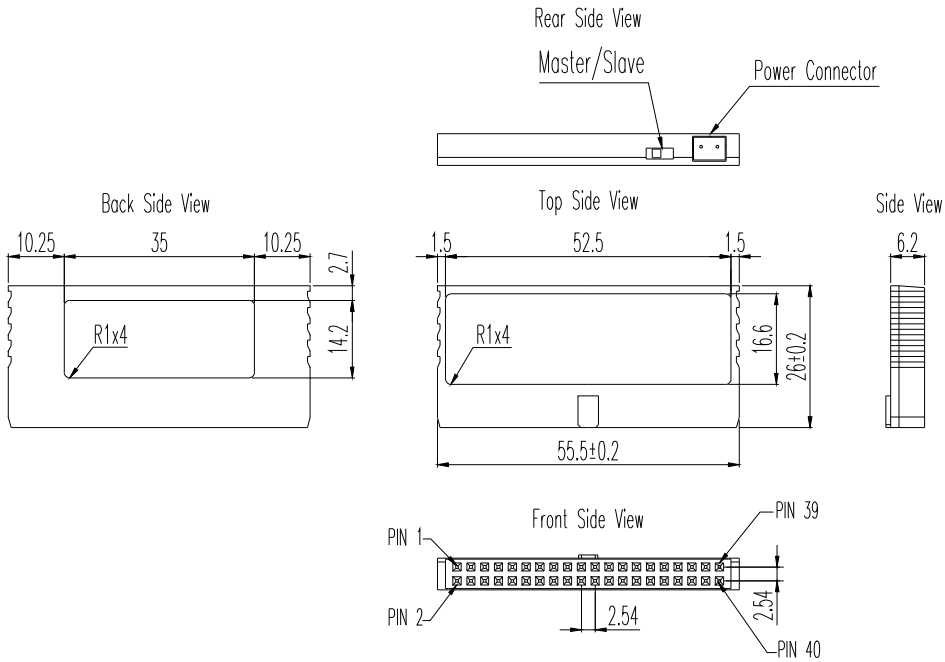
Active mode, the card can respond and access the media immediately, and the commands are processed with no delay.

6.2.2 Power down Mode

This card can set itself into Power Down mode. To enable this mode, it is needed to use the Information Change command, which is a vender unique command. The advantage of using this mode is the ability to move automatically into Sleep mode after command completion.

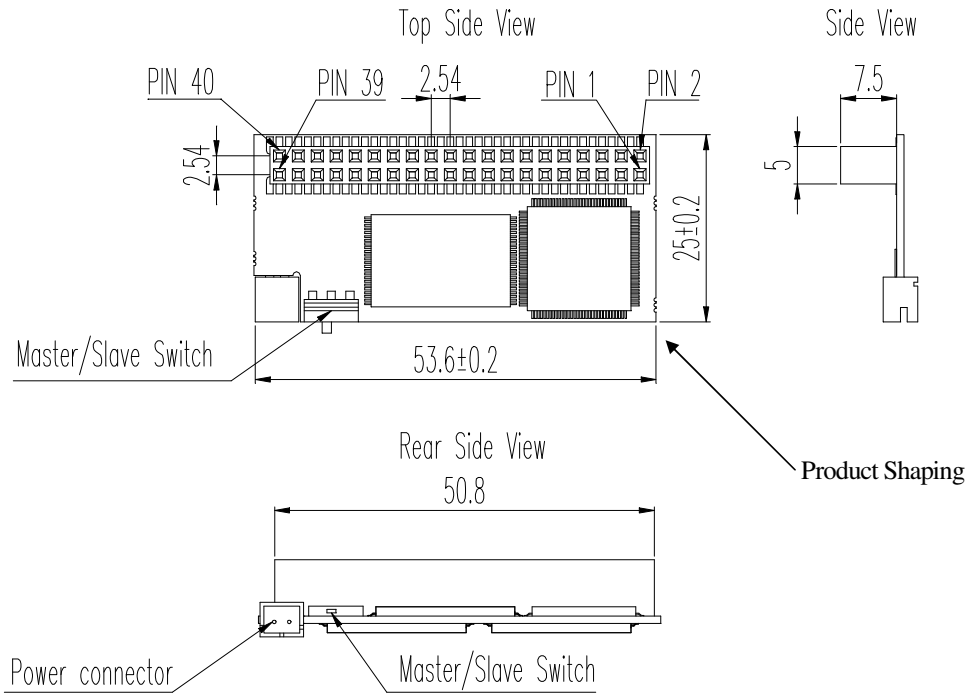
6.3 Physical Specification

6.3.1 MIDE 40 pin P-form with housing outline dimensions

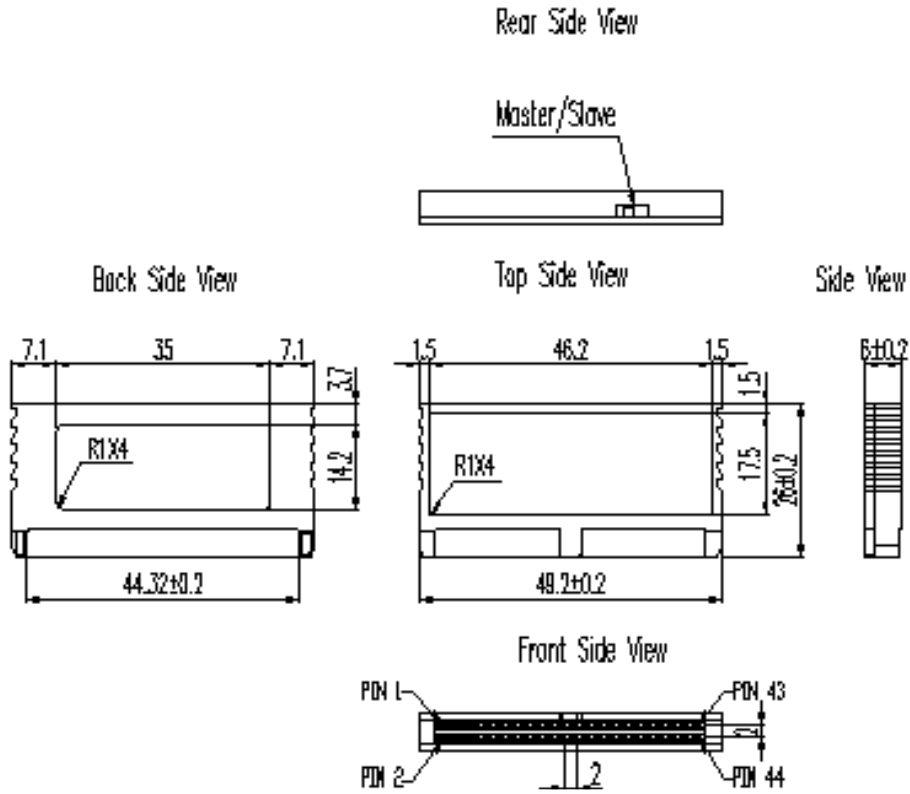


Produ
ct

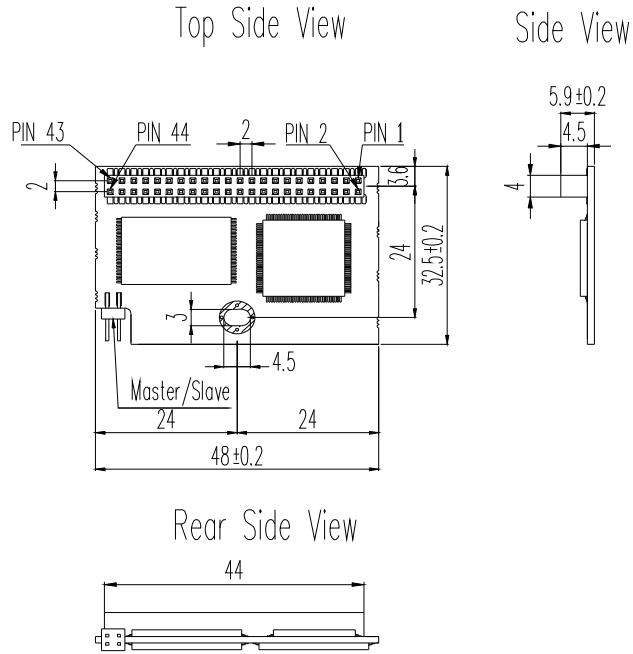
6.3.2 MIDE 40 pin L-form without housing outline dimensions



6.3.3 MIDE 44-pin P-form with housing outline dimension



6.3.4 MIDE 44-pin L-form without housing outline dimensions





7. Pin Assignment

7.1 Pin Type

Pin Num.	Pin Symbol	Pin Type	Pin Num.	Pin Symbol	Pin Type
1	#Reset	I	2	GND	Ground
3	Data 7	I/O	4	Data 8	I/O
5	Data 6	I/O	6	Data 9	I/O
7	Data 5	I/O	8	Data 10	I/O
9	Data 4	I/O	10	Data 11	I/O
11	Data 3	I/O	12	Data 12	I/O
13	Data 2	I/O	14	Data 13	I/O
15	Data 1	I/O	16	Data 14	I/O
17	Data 0	I/O	18	Data 15	I/O
19	GND	Ground	20	Key	Cut Pin
21	DMARQ	O	22	GND	Ground
23	#IOW	I	24	GND	Ground
25	#IOR	I	26	GND	Ground
27	IORDY	I	28	CSEL	I
29	DMACK	I	30	GND	Ground
31	IRQ	O	32	#IOCS16	O
33	A1	I	34	#PDIAG	I/O
35	A0	I	36	A2	I
37	#CS0	I	38	#CS1	I
39	#DASP	I/O	40	GND	Ground
41	Vcc	Supply Voltage	42	Vcc	Supply Voltage
43	GND	Ground	44	TYPE	

Note1: # means low active.

Note2: Pin 41 to 44 NC for 40-pin product.



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7.2 Interface Signals Description

Signal Name	Pin	I/O	Description
#RESET	1	I	HOST RESET Reset signal from the host that is active on power up and inactive thereafter.
Data (15-0)	3 - 18	I/O	HOST DATA15-0 These 16 lines carry the Data between the controller and the host. The low 8 lines transfer commands, status, and ECC information between the host and the controller.
DMARQ	21	O	DMA REQUEST When ready to transfer data to or from the host, this signal used for DMA data transfers between host and device, shall be asserted by the device.
#IOW	23	I	I/O WRITE This strobe pulse is used to clock data or commands on the host data bus into the controller. The clocking will occur on the negative to positive edge of the signal (trailing edge).
#IOR	25	I	I/O READ This is a read strobe generated by the host. This signal gates data or status on the host bus and strobes the data from the controller into the host on the low to high transition (trailing edge).
IORDY	27	I	I/O READY This signal is negated to extend the host transfer cycle of any host register access (Read or Write) when the device is not ready to respond to a data transfer request.
Vcc	41,42	--	5V Power supply



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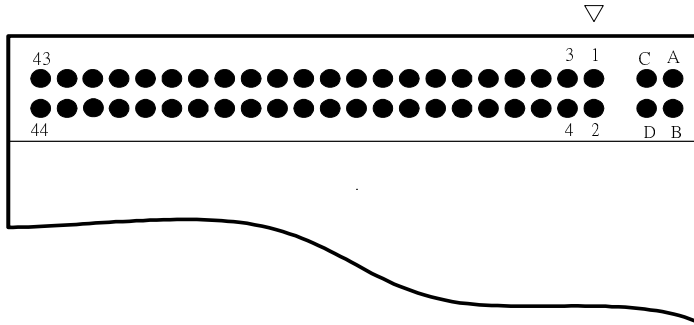
Signal Name	Pin	I/O	Description
CSEL	28	I	CABLE SELECT When grounded, the device is configured as a Master. When opened, this device is configured as a Slave.
DMACK	29	I	DMA ACKNOWLEDGE This signal shall respond to DMARQ by the host to initiate DMA transfers.
IRQ	31	O	INTERRUPT REQUEST This is an interrupt request from the controller to the host, asking for service. The output of this signal is tri-stated when the interrupt are disabled by the host.
#IOCS16	32	O	I/O SELECT 16 This open drain output is asserted low to indicate to the host the current cycle is a 16-bit word data transfer.
#PDIAG	34	I/O	PASS DIAGNOSTIC After an Execute Diagnostic command to indicate to the master it has passed its diagnostics, this bi-directional open drain signal is asserted by the slave.
A (2-0)	33,35,36	I	HOST ADDRESS 2-0 These address lines are used to select the registers within the controller task file.
#CS0	37	I	HOST CHIP SELECT 0 A chip select signal used to select the controller task file.
#CS1	38	I	HOST CHIP SELECT 1 A chip select signal that is used to select the control and diagnostic register.
#DASP	39	I/O	DISK ACTIVE/SLAVE PRESENT This open drain output signal is asserted low any time the drive is active. In a master/slave configuration, the slave uses it to inform the master of its present.
NC	20	-	These pins are reserved for the connector keys.
GND	2,19,22,24,26,3	--	GROUND

	0,40,43								
--	---------	--	--	--	--	--	--	--	--

7.3 Installing The SSD Drive In a Two-Drive Configuration

If Pin A and Pin B are jumped, the drive is in Cable Select mode.
 If both pins A and B remain open, the SSD drive is configured as a Master in a Master/Slave configuration or as the only drive in a single drive system. Pins A and B are pulled-up input pins that are shorted together internally (Pins C and D are ground).

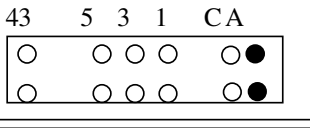
If the SSD drive is installed as the second, or Slave, drive in a two-drive configuration, either pin AC or



none of the pins should be grounded. These pins will configure the SSD drive as a Slave device.

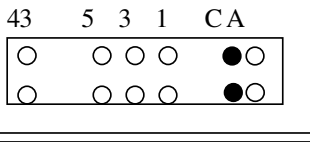
Master/Slave Configuration Pins

Cable Select:

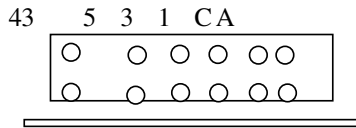


If Pin A and Pin B are jumped, the drive is in Cable Select

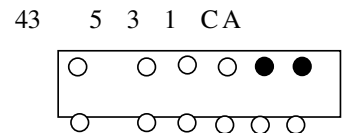
Master:



Slave:



44 6 4 2 DB



If all pins A, B, C, and D are open, or Pin A and Pin C are jumped, the drive is in Slave mode



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If Pin C and Pin D are jumped,
the drive is in Master mode



8. ATA Specific Register Definitions

As we described the adapter provides several kinds of addressing modes, Memory mode, I/O mode, and True IDE. Below are described the procedures access for accessing each mode the Task File registers.

8.1 True IDE Mode

True IDE Mode

#CS0	#CS1	DA2	DA1	DA0	#IORD = "0"	#IOWR = "0"
1	1	X	X	X	Hi-Z	Not Used
1	0	0	X	X	Hi-Z	Not Used
1	0	1	0	X	Hi-Z	Not Used
0	0	X	X	X	Invalid	Invalid
1	0	1	1	0	Alternate Status	Device Control
1	0	1	1	1	Device Address	Not Used
0	1	0	0	0	Data	Data
0	1	0	0	1	Error	Feature
0	1	0	1	0	Sector Count	Sector Count
0	1	0	1	1	Sector Number	Sector Number
0	1	1	0	0	Cylinder Low	Cylinder Low
0	1	1	0	1	Cylinder High	Cylinder High
0	1	1	1	0	Drive/Head	Drive/Head
0	1	1	1	1	Status	Command

8.2 ATA Registers

8.2.1 Data Register

The Data register is a 16-bit register used to transfer data blocks between the ATA data buffer and the host. In addition, the Format Track command uses this register to transfer the sector-information. Setting this mode requires calling the Set Features command.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
D7	D6	D5	D4	D3	D2	D1	D0

bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8
D15	D14	D13	D12	D11	D10	D9	D8

8.2.2 Error Register

The Error Register contains additional information about the source of an error. The information in the register is only valid when an error is indicated in ERR-bit (bit-0 = 1) of the Status Register. This register is valid when the BSY bit in Status register and Alternate status register are set to “0”(Ready).

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
BBK	UNC	MC[0]	IDNF	MCR[0]	ABRT	TONF[0]	AMNF
BBK		Bad Block mark detected in the requested sector ID field - Not supported					
UNC		Non-Correctable data error encountered					
MC[0]		Removable media access ability has changed - not supported (is 0)					
IDNF		Requested sector ID-field Not Found					
MCR[0]		Media Change Request indicates that the removable-media drive's latch has changed, indicating that the user wishes to remove the media - not supported (is 0)					
ABRT		Drive status error or Aborted invalid command					
TONF[0]		Track 0 Not Found during a <i>Recalibrate</i> command - Not supported					
AMNF		Address Mark Not Found after finding the correct ID field - Not supported					

8.2.3 Feature Register

This register enables drive-specific features. See the Set Features or Get/Set Features command descriptions.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
Feature byte							

8.2.4 Sector Count Register

The Sector Count Register contains the number of data sectors requested to be transferred during a read or write operation between the host and the adapter. A zero register value specifies 256 sectors. The command was successful if this register is zero at command completion. If the request is not completed, the register contains the number of sectors left to be transferred.



This register's initial values is "01H"

Some commands (e.g. Initialize Drive Parameters or Format Track) may redefine the register's contents.)

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
Sector count byte							

8.2.5 Sector Number Register

In the CHS (Cylinder, Head, Sector) mode, the Sector Number register contains the subsequent command's starting sector number, which can be from 1 to the maximum number of sectors per track. In LBA (logical block address) mode, this register contains LBA bits 0-7, which are updated at command completion. See the command descriptions for register contents at command completion (whether successful or unsuccessful).

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
SN7	SN6	SN5	SN4	SN3	SN2	SN1	SN0
LBA7	LBA6	LBA5	LBA4	LBA3	LBA2	LBA1	LBA0
SN0 – SN7		Sector number byte (8-bits)					
LBA0 – LBA7		LBA bits 0 to 7					



8.2.6 Cylinder Low Register

In the CHS mode, the Cylinder Low Register contains the cylinder number low-8 bits and reflects their status at command completion. In LBA mode, this register contains LBA bits 8-15 and reflects their status at command completion.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
CL7	CL6	CL5	CL4	CL3	CL2	CL1	CL0
LBA15	LBA14	LBA13	LBA12	LBA11	LBA10	LBA9	LBA8
CL0 – CL7	Cylinder Low byte (8-bits)						
LBA8 – LBA15	LBA bits 8 to 15						

8.2.7 Cylinder High Register

In the CHS mode, the Cylinder High Register contains the cylinder numbers high-8 bits and reflects their status at command completion. In LBA mode, this register contains LBA bits 16-23 and reflects their status at command completion.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
LBA23	LBA22	LBA21	LBA20	LBA19	LBA18	LBA17	LBA16
CH0 – CH7	Cylinder High byte (8-bits)						
LBA16 – LBA23	LBA bits 16 to 23						



8.2.8 Drive Head Register

The Drive/Head Register is used to select the drive and head (heads minus 1, when executing Initialize Drive Parameters command). It is also used to select the LBA addressing instead of the CHS addressing.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
1	LBA	1	DRV	HS3	HS2	HS1	HS0
HS0-HS3/ DRV		Head number. Drive select number. When DRV=0, the master drive is selected. When DRV=1, the Slave drive is selected.					
LBA24-LBA27		MSB of the LBA addressing.					
LBA		Address mode select. 0 = CHS (Cylinder, Head, Sector) mode. 1 = LBA (Logical Block Address) mode. Logical Block address interrupted as follows: LBA07-LBA00 :Sector Number Register D7-D0 LBA15-LBA08:Cylinder Low Register D7-D0 LBA23-LBA16:Cylinder High Register D7-D0 LBA27-LBA24:Drive/Head Register HS3-HS0					

8.2.9 Status Register

This register contains the adapter status. The contents of this register are updated to reflect the current state of the adapter and the progress of any command being executed by the adapter. When the BSY bit is equal to zero, the other bits in this register are valid. When the BSY bit is equal to one, the other bits in this register are not valid. When the register is read, the interrupt (#IREQ pin) is cleared.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
BSY	DRDY	DWF	DSC	DRQ	CORR	0	ERR
ERR		When set, indicates that an error has occurred during the previous command execution. The bits in the Error Register indicate the cause.					
IDX		Index is not used – always set to Zero.					
CORR		Indicates that a data error was corrected; transfer is not terminated.					
DRQ		Data Request. When set, indicates that the adapter is ready to transfer a word or byte of data between the host and the adapter.					
DSC		Drive Seek Complete. When set, indicates that the requested sector was found.					
DWF		Drive Write Fault status. When set, indicates that an error has occurred during write.					
DRDY		Indicates whether the adapter is capable of performing drive operations (commands). This bit is cleared at power up and remains cleared until the drive is ready to accept a command. On error, DRDY changes only after the host reads the Status register.					
BSY		This signal is set during the time the adapter accesses the command buffer or the registers. During this time the host is locked out from accessing the command register and buffer. As long as this bit is set no bits in the register are valid.					

8.2.10 Alternate Status Register

The Alternate Status Register contains command block status information (see Status register). Unlike the Status register, reading this register does not acknowledge or clear an interrupt.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
BSY	DRDY	DWF	DSC	DRQ	CORR	0	ERR

8.2.11 Device Control Register

The Device Control Register is used to control the drive interrupt request and issue an ATA soft reset to the drive.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
---	---	---	---	1	SRST	#IEN	0
#IEN		INTERRUPT ENABLE: When set (0), it enables interrupts to the host (using the #IREQ tri-state pin). When inactive (1) or drive is not selected, it disables all pending interrupts (#IREQ in high-Z). This bit is ignored in Memory mode.					
SRST		SOFT RESET: When set, forces the ATA to perform an AT disk control soft reset operation.					

8.2.12 Drive Address Register

This register reflects the drive and its heads. This register is provides for compatibility with the AT disk interface. It's recommended that this register is not mapped into this host's I/O space because of potential conflicts on bit7.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
High-Z	#WTG	#HS3	#HS2	#HS1	#HS0	#DS1	#DS0
#DS0		When set (0), it indicates that drive 0 is active and selected.					
#DS1		When set (0), it indicates that drive 1 is active and selected.					
#HS0 - #HS3		Negation of the head number in the Drive/Head Register.					
#WTG		When set (0), it indicates that a write operation is in progress, otherwise it is inactive (1) - not supported.					

Note: Addressing Mode Descriptions - The adapter, on a command by command basis, can operate in either CHS or LBA addressing modes. Identify Drive Information tells the host whether the drive supports LBA mode. The host selects LBA mode via the Drive/Head Register. Sector number, Cylinder Low, Cylinder High, and Drive/Head Register bits HS3=0 contain the zero-based LBA. The drive's sectors are linearly mapped with: LBA = 0 => Cylinder 0, head 0, sector 1. Regardless of the translation mode, a sector LBA address does not change. $LBA = (Cylinder * no\ of\ heads + heads) * (sectors/track) + (Sector - 1)$.



9. ATA Commands

9.1 Check Power Mode - 98H or E5H

This command checks the current power mode of the adapter. When this command is issued and the adapter is in standby mode, or is being set to standby mode, or during a recovery from standby mode is attempted, adapter sets the BSY bit in the Status register and sets the Sector Count Register to "00H". Then the BSY bit in the Status register is cleared. When the adapter is in the Idle mode, it sets the BSY bit in the Status register and sets "FFH" in the Sector Count Register. Then the BSY bit in the Status register is cleared. An interrupt is issued after the BSY bit is cleared.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Command	98H or E5H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Sector Count	Power Mode Code.(00H or 80H or FFH)							
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
						V		



9.2 Execute Drive Diagnostic - 90H

This command performs self-diagnostics on various internal components of the adapter. Results of the test are reported in the Error Register. Note that the bit definitions for the Error Register do not apply with this command. Instead, the value in the Error Register is a diagnostic code, defined in the table below.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head				DEV				
Command	90H							

OUTPUTS: The diagnostic code written into the Error Register is an 8-bit code as shown in the table below.

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V		V				V
Error	Diagnostic code, see table below							

Code	Description
01H	No error detected
02H	Format Media error
03H	Sector buffer error
04H	ECC logic error
05H	Controlling microprocessor error



9.3 Erase Sector(s) - C0H

This command is processed as a NOP command.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	[LBA mode only] The number of sectors to be formatted on the track, must be set to FFH							
Sector Number	[LBA mode only] LBA[7:0] of the first sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] of the starting sector/LBA			
Command	C0H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V				V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V			V		V		V



9.4 Format Track - 50H

This command is processed as a NOP command.

INPUTS

Register	7	6	5	4	3	2	1	0
Features								
Sector Count	[LBA mode only] The number of sectors to be formatted on the track. Must be set to FFH							
Sector Number	[LBA mode only] LBA[7:0] of the first sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] of the starting sector/LBA			
Command	50H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V				V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
				V		V		V



9.5 Identify Drive – ECH

The Identify Drive command enables the host to receive parameter information from the adapter. When the command is issued, the adapter sets the BSY bit, prepares to transfer the 256 words of adapter identification data to the host, sets the DRQ bit, clears the BSY bit, and generates an interrupt. The host can then transfer the data by reading the Data register. All reserved bits or words are all zero. See following table for the identify drive information for this adapter

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head				DEV				
Command	ECH							

OUTPUTS

Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
Status	V	V	V	V	V			V
	BBK	UNC	MC	IDNF	MCR	ABRT	TKONF	AMNF
Error						V		



9.6 Idle - 97H or E3H

Although this command is supported for backward compatibility, it has no actual function. The adapter will always return a 'good' status at the completion of this command.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	Time-out Parameter. This parameter is ignored by the adapter							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head				DEV				
Command	97H or E3H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TKONF	AMNF
						V		



9.7 Idle Immediate - 95H or E1H

Although this command is supported for backward compatibility, it has no actual function. The adapter will always return a 'good' status at the completion of this command.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head				DEV				
Command	95H or E1H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
						V		



9.8 Initialize Drive Parameters - 91H

Initialize Drive Parameters allows the host to alter the number of sectors per track and the number of heads per cylinder. This command does not check the validity of counts of sectors and heads. If an invalid value is set, an error will be reported when another command attempts an invalid access.

The Sector Count Register specifies the number of logical sectors per logical track, and the Device/Head register specifies the maximum head number.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	Number of sectors							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head				DEV	Max Head (no. of head = 1)			
Command	91H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V		V	V			V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF



9.9 Read Buffer - E4H

The Read Buffer command enables the host to read the current contents of the adapter's sector buffer. This command has the same protocol as the Read Sector(s) command.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head		LBA		DEV				
Command	E4H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TKONF	AMNF
						V		



9.10 Read Long Sector(s) - 22H or 23H

Read Long (w/ and w/o retry) is similar to the Read Sectors command, except that the content of the Sector Count Register is ignored and only one sector is read. The 512 data bytes and 4 ECC bytes are read into the buffer (with no ECC correction) and then transferred to the host.

The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be read. The Sector Count Register shouldn't specify a value other than 1.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	The number of sectors/logical blocks to transfer. This should be set to 01 for compatibility							
Sector Number	Sector[7:0] or LBA[7:0] of the sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the sector/LBA to transfer							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] of the sector/LBA to transfer			
Command	22H (retries enabled) or 23H (retries disabled)							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Sector Count	00 if the command proceed without error, else the number of untransferred sectors.							
Sector Number	Sector[7:0] or LBA[7:0] of the last sector read							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the last sector read							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the last sector read							
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TKONF	AMNF
	V			V		V		V



9.11 Read Multiple - C4H

This command functions like the Read Sector(s) command, but instead of issuing interrupts for each sector, interrupts are issued when a block containing the counts of sectors, defined by the Set Multiple command is, transferred. Also, the DRQ required for the transfer only has to be set at the start of the data block and does not affect other sectors. When the Read Multiple command is issued, the requested sectors (not the block counts or the sector counts in a block) are written into the Sector Count Register. Errors occurring during command execution are reported at the start of a block transfer or at the start of transfer of part of a block. However, the transfer continues even if DRQ is set and the data is corrupted. After the data transfer, the content of the task file with the block data containing the sectors where the error occurred is not defined. To obtain valid error information the host has to request a re-transmission. The next block or part of a block is transferred only if the error is correctable. For all other errors the command is aborted after transferring a block containing an error. The Read Multiple command is supported for backward compatibility. If R/W Multiple commands have been enabled by a previous valid Set Multiple command, the Read Multiple command is identical to the Read Sectors operation except that several sectors are transferred as a block to the Host without the intervening Host handshaking. The block count stands for the number of sectors to be transferred as a block. It is established using the Set Multiple command. Although the Set Multiple, and R/W Multiple commands are supported, the only valid block count is one.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	The number of sectors/logical blocks to transfer							
Sector Number	Sector[7:0] or LBA[7:0] of the sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the sector/LBA to transfer							
Device/Head		LBA		DEV	Head number or LBA			
Command	C4H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V	V		V
Sector Count	The first sector where the first unrecoverable error occurred							
Sector Number	Sector[7:0] or LBA[7:0] of the last good sector transferred							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] last good sector transferred			
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	V	V	V	V	V	V	V



9.12 Read Sectors(s) – 20H or 21H

The Cylinder Low, Cylinder High, Device/Head and Sector Number or LBA registers specify the starting sector address to be read. The Sector Count Register specifies the number of sectors to be transferred.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	The number of sectors/logical blocks to transfer							
Sector Number	Sector[7:0] or LBA[7:0] of the sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the sector/LBA to transfer							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] of the sector/LBA to transfer			
Command	20H (retry enabled) or 21H (retries disabled)							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V	V		V
Sector Count	The first sector where the first unrecoverable error occurred							
Sector Number	Sector[7:0] or LBA[7:0] of the last good sector transferred							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] last good sector transferred			
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	V	V	V	V	V		V



9.13 Read Verify Sector(s) – 40H or 41H

The Read Verify Sectors command verifies one or more sectors on the card by transferring data from the Flash media to the data buffer in the card and verifying that the ECC is correct. It is performed identically to the Read Sectors command, except that DRQ is not asserted, and no data is transferred to the host. If an uncorrectable error occurs, the Read Verify command will be terminated at the failing sector. The task file registers contain the CHS, or LBA of the sector in which the error occurred.

The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be verified. The Sector Count Register specifies the number of sectors to be verified.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	The number of sectors/logical blocks to verify							
Sector Number	Sector[7:0] or LBA[7:0] of the first sector/LBA to verify							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the sector/LBA to verify							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to verify							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] of the sector/LBA to verify			
Command	40H (retries enabled) or 41H (retries disabled)							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V	V		V
Sector Count	The first sector where the first unrecoverable error occurred							
Sector Number	Sector[7:0] or LBA[7:0] of the sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] of the sector/LBA to transfer			
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TKONF	AMNF
	V	V	V	V	V	V		V



9.14 Recalibrate - 1XH

The adapter performs only the interface timing and register operations. When this command is issued, the adapter sets BSY and waits for an appropriate length of time after which it clears BSY and issues an interrupt. When this command ends normally, the adapter is initialized.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head				DEV				
Command	1XH							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
		V	V	V				V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
						V		



Tiger Series MINI-IDE Industrial Application

C-ONE TECHNOLOGY Corp.

9.15 Request Sense - 03H

This command requests extended error information for the previous command. The table below defines the valid extended error codes. Those codes are placed in the Error Register.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head				DEV				
Command	03H							

OUTPUTS

The diagnostic code written into the Error Register is an 8-bit code as shown in the table below.

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V		V				V
Error	Sense code, see table below							

Code	Description
00H	No error detected
01H	Self test OK (No error)
03H	Write/Erase failed
09H	Miscellaneous Error - N/A
20H	Invalid Command
21H	Invalid Address (requested Head or Sector invalid)
2FH	Address Overflow (address too large)
35H, 36H	Supply or generate Voltage Out of Tolerance
11H	Uncorrectable ECC Error
18H	Corrected ECC Error - N/A
05H, 30H-34H, 37H, 3EH	Self Test Diagnostic Failed
10H, 14H	ID Not Found - N/A
3AH	Spare Sectors Exhausted
1FH	Data Transfer Error / Aborted Command
0CH, 38H, 3BH, 3CH, 3FH	Corrupted Media Format - N/A



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9.16 Seek - 7XH

This command seeks and picks up the head to track specified in the Task File registers. Actually the adapter performs only an interface timing and register information.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	(Valid in LBA mode only) LBA[7:0] of the track							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the track							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the track							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] of the track			
Command	7XH							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TKONF	AMNF
			V	V	V	V		



9.17 Set Feature - EFH

This command is used by the host to establish or select from the specific features listed below.(after a power up or a hardware reset) An ATA software reset does not set the features to default. The feature code is set to 81H, this mode is the default mode.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	Feature number according to the table below							
Sector Count	Configuration required							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head				DEV				
Command	EFH							

Feature Codes

Code	Description
01H	Enable 8-bit data transfers
55H	Disable Read Look Ahead
66H	Disable reverting to power on defaults
81H	Disable 8-bit data transfers
BBH	4 bytes of ECC apply on read long/write long commands
CCH	Enable reverting to power on defaults

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TKONF	AMNF
						V		



9.18 Set Multiple Mode - C6H

The Set Multiple command allows the adapter to perform Read Multiple and Write Multiple operations. It also sets the block count (counts of sectors making up a block) for these commands. The sector count per block is placed in the Sector Count Register. The adapter supports only blocks with one sector.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	Sector Count per Block(= 1)							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head				DEV				
Command	C6H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
						V		



9.19 Set Sleep Mode - 99H or E6H

This is the only command that allows the host to set the adapter into Sleep mode. When the adapter is set to sleep mode, the adapter clears the BSY line and issues an interrupt. The adapter enters sleep mode and the only method to make the adapter active again (back to normal operation) is by performing a hardware reset or software reset.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head				DEV				
Command	99H/E6H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
						V		



9.20 Standby - 96H or E2H

This command sets the adapter in Standby mode. If the Sector Count Register is a value other than 0H, an Auto Power Down is enabled and when the adapter returns to the idle mode, the timer starts a countdown. The time is set in the Sector Count Register.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	Time period value							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head				DEV				
Command	96H or E2H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TKONF	AMNF
						V		



9.21 Standby Immediate 94H or E0H

This command sets the adapter into standby mode.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head				DEV				
Command	94H or E0H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TKONF	AMNF
						V		



9.22 Translate Sector - 87H

This command allows the host a method of determining the exact number of times a sector was used (erased). The controller responds with the 512-byte buffer of information that includes the Hot Count, if available, for the sector. This command is not supported in this adapter and will always return the Hot Count as "00".

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	Sector Count							
Sector Number	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] of the starting sector/LBA			
Command	87H							

OUTPUTS

The diagnostic code written into the Error Register is an 8-bit code as shown in the table below.

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V				V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V			V		V		

Address	Information
00H - 01H	Cylinder MSB (00H), Cylinder LSB (01H)
02H	Head
03H	Sector
04H - 06H	LBA MSB (04H) - LSB (06H)
07H - 12H	Reserved
13H	Erased Flag (FFH) = Erased; (00H) = Not Erased
14H - 17H	Reserved
18H - 1AH	Hot Count MSB (18H) - LSB (1AH)
1BH - 1FFH	Reserved



Tiger Series MINI-IDE Industrial Application

C-ONE TECHNOLOGY Corp.

9.23 Wear Level - F5H

This command is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always return the value "00H", indicating that wear leveling is not needed.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head				DEV				
Command	F5H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Sector Count	Always "00H"							
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	V	V	V	V	V		V



9.24 Write Buffer - E8H

This command enables the host to rewrite the contents of the adapter data buffer in the adapter with the desired data sting. This data buffer can be accessed by and read by the Read Buffer Command.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head				DEV				
Command	E8H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TKONF	AMNF
						V		



9.25 Write Long Sector(s) 32H or 33H

This command operates in the same way as the Write Sector command except that it writes data and ECC bytes for long commands directly from the sector buffer. ECC bytes for long commands are byte writes that consist of a 4-byte fixed length data. This command can write only one sector at a time.

INPUT

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	"01h"							
Sector Number	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] of the starting sector/LBA			
Command	32H or 33H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
		V	V	V	V	V		
Sector Count	Bit-0 if the command proceeded successfully, other – untransferred sectors count							
Sector Number	Sector[7:0] or LBA[7:0] of the last good sector transferred							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V			V		V		



9.26 Write Multiple - C5H

This command functions in the same way as the Write Sector command. When this command is issued, the adapter sets the BSY within 400nsec. Interrupts are not issued for every sector but after one block consisting of the counts of sectors defined by the Set Multiple command is transferred. The DRQ required for the transfer only has to be set at the beginning of the block and does not affect other sectors.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	Sector Count							
Sector Number	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
Device/Head		LBA		DEV	H[3:0] or LB[27:24] of the starting sector/LBA			
Command	C5H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Sector Count	Bit-0 if the command proceeded successfully, other – untransferred sectors count							
Sector Number	Sector[7:0] or LBA[7:0] of the last good sector transferred							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V		V	V	V	V		V



9.27 Write Multiple without Erase – CDH

This command is similar to the Write Multiple command with the exception that an implied erase before using this command. Please note that before using this command it is required to erase the respective sectors using the Erase Sector command.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	Sector Count							
Sector Number	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
Device/Head		LBA		DEV	H[3:0] or LB[27:24] of the starting sector/LBA			
Command	CDH							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Sector Count	Bit-0 if the command proceeded successfully, other – untransferred sectors count							
Sector Number	Sector[7:0] or LBA[7:0] of the last good sector transferred							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V		V	V	V	V		V



9.28 Write Sector(s) - 30H or 31H

This command allows the host to write the specified number (1 to 256) of sectors in the Sector Count Register. A sector count of 0 indicates a write request of 256 sectors. The write operation starts from the sector specified in the Sector Number register. The command ends execution by placing the cylinder, head and sector number of the last written sector in the Task File registers.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	Sector Count							
Sector Number	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] of the starting sector/LBA			
Command	30H or 31H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Sector Count	Bit-0 if the command proceeded successfully, other – untransferred sectors count							
Sector Number	Sector[7:0] or LBA[7:0] of the last good sector transferred							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V		V	V	V	V		V



9.29 Write Sector(s) without Erase - 38H

This command is similar to the Write Sector command with the exception that an implied erase before using this command. Please note that before using this command it is required to erase the respective sectors using the Erase Sector command.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	Sector Count							
Sector Number	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] of the starting sector/LBA			
Command	38H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Sector Count	Bit-0 if the command proceeded successfully, other – untransferred sectors count							
Sector Number	Sector[7:0] or LBA[7:0] of the last good sector transferred							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V			V		V		V



9.30 Write Verity - 3CH

This command is similar to the Write Sector command with the exception that each sector is verified immediately after writing.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	Sector Count							
Sector Number	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] of the starting sector/LBA			
Command	3CH							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Sector Count	Bit-0 if the command proceeded successfully, other – untransferred sectors count							
Sector Number	Sector[7:0] or LBA[7:0] of the last good sector transferred							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TKONF	AMNF
	V			V		V		V

10. Error Posting

Command	Error Register						Status Register				
	BB	UNC	IDN	ABR	T0N	AMN	DRD	EFW	DSC	CORR	ERR
Check Power Mode				y			y	y	y		y
Execute Drive Diags											y
Format Track			y	y			y	y	y		y
Identify Drive				y			y	y	y		y
Idle				y			y	y	y		y
Idle Immediate				y			y	y	y		y
Initialize Drive							y	y	y		
params				y	y		y	y	y		y
Recalibrate				y			y	y	y		y
Read Buffer	y	y	y	y		y	y	y	y	y	y
Read Long	y	y	y	y		y	y	y	y	y	y
Read Multiple	y	y	y	y		y	y	y	y	y	y
Read Sector(s)	y	y	y	y		y	y	y	y	y	y
Read Verify Sector(s)			y	y			y	y	y		y
Seek				y			y	y	y		y
Set Features				y			y	y	y		y
Set Multiple Mode				y			y	y	y		y
Sleep				y			y	y	y		y
Standby				y			y	y	y		y
Standby Immediate				y			y	y	y		y
Write Buffer	y		y	y			y	y	y		y
Write Long	y		y	y			y	y	y		y
Write Multiple	y		y	y			y	y	y		y
Write Sector(s)				y			y	y	y		y
Invalid Command											

註解[JCL1]:



11. Identify Drive Information

Word	Data	Description
0	045AH	General configuration bit-significant information Bits Description 15-14 10=ATAPI device 11=Reserved 13 Reserved 12-8 Field indicates command packet set used by device 7 1=removable media device 6-5 00=Device shall set DRQ to one within 3 ms of receiving PACKET command. 01=Obsolete. 10=Device shall set DRQ to one within 50 us of PACKET command. 11=Reserved 4-3 Reserved. 2 Incomplete response 1-0 00=12 byte command packet 01=16 byte command packet 1x=Reserved
1	Note 1	Number of Cylinders
2	0000h	Reserved
3	Note 1	Number of Heads
4	0000H	Obsolete
5	XXXXH	Obsolete
6	Note 1	Number of sectors per track
7-8	XXXXH	Number of sectors per card (Word 7= MSW, Word 8= LSW)
9	XXXXH	Obsolete
10-19	XXXXH	20 ASCII char serial number.
20	0002H	Obsolete
21	0002H	Obsolete
22	0004H	ECC bytes passed on Read/Write Long Commands
23-26	XXXXH	Firmware revision in ASCII chars.
27-46	XXXXH	Model Number (Vendor Unique)
47	0001H	Maximum Block Count=1 for Read/Write Multiple command
48	0000H	Reserved
49	2F00H	Capabilities: LBA supported (bit 9). Capabilities: LBA supported (bit 9).



Tiger Series MINI-IDE Industrial Application

C-ONE TECHNOLOGY Corp.

Word	Data	Description
		15 0 =interleave DMA not supported 14 0 =command queuing not supported 13 1 =overlap operation supported 12 0 =ATA software reset required (Obsolete) 11 0 =IORDY not supported 10 0 =IORDY maybe enable 9 0 =LBA not supported 8 0 =DMA not Supported 7-0 Vendor specification
50	0000H	Reserved
51	0200H	PIO data transfer cycle timing mode
52	0000H	Obsolete
53	0003H	Translation Parameters Vaild (bit0:Word54 to 58 are valid, bit1:Word 64 to 70 are valid) 15-3 Reserved 2 1 = the field reported in word 88 are valid 0 = the field reported in word 88 are not valid 1 1 = the field reported in word 64-70 are valid 0 = the field reported in word 64-70 are not valid 0 1 = the field reported in word 54-58 are valid 0 = the field reported in word 54-58 are not valid
54	Note 1	Number of Current Cylinders
55	Note 1	Number of Current Heads
56	Note 1	Number of Current Sectors Per Track
57	Note 1	LSW of the Current Capacity in Sectors
58	Note 1	MSW of the Current Capacity in Sectors
59	0100H	Multiple sector setting If bit 8 is set to one, bits 7-0 reflect the number of sector currently set to transfer on a READ/WRITE MULTIPLE command. This filed may default to the preferred value for the device. Command Code: C6h
60	Note 1	LSW of the total number of user addressable LBA's
61	Note 1	MSW of the total number of user addressable LBA's
62	0000H	Reserved
63	0001H	15-11 Reserved 10 1 =Multiword DMA mode 2 is selected 0 =Multiword DMA mode 2 is not selected 9 1 = Multiword DMA mode 1 is selected 0 =Multiword DMA mode 1 is not selected



Tiger Series MINI-IDE Industrial Application

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Word	Data	Description
		<p>8 1= Multiword DMA mode 0 is selected 0=Multiword DMA mode 0 is not selected</p> <p>7-3 Reserved</p> <p>2 0= Multiword DMA mode 2 and below are not supported</p> <p>1 0= Multiword DMA mode 1 and below are not supported</p> <p>0 1= Multiword DMA mode 0 is supported Multiword DMA mode selected.</p>
64	0003H	<p>Advanced PIO Modes supported (bit0: PIO-3, bit1:PIO4,supported)</p> <p>15-8 Reserved</p> <p>7-0 Supported</p> <p>Bits 7 through 0 of word 64 of the Identify Device parameter information is defined as the PIO data and register transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one.</p> <p>Of these bits, bits 7 through 2 are Reversed for future PIO modes. Bit 0, if set to one, indicated that the device supports PIO mode 3. All device except CFA and PCMCIA device shall support PIO mode 3 and shall set bit 0 to one. Bit 1, if set to one, indicated that the device support PIO mode 4.</p>
65	01E0H (DMA 2) 0000H (PIO 4)	<p>Minimum Multiword DMA transfer cycle time per word</p> <p>15-0 Cycle time in nanoseconds</p> <p>If this field is supported, bit 1 of word 53 shall be set to one. Any device that supports Multiword DMA mode 1 or above shall support this field, and the value in word 65 shall not be less than the minimum cycle time for the fastest DMA mode supported by the device.</p> <p>If bit 1 of word 53 is set to one because a device supports a field in words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.</p>
66	01E0H 0000H (PIO 4)	<p>Manufacturer's recommended Multiword DMA transfer cycle time</p> <p>15-0 Cycle time in nanoseconds</p> <p>If this field is supported, bit 1 of word 53 shall be set to one, Any device that supports Multiword DMA mode 1 or above shall support this field, and the value in word 66 shall not be less than the value in word 65.</p>
67	0078H	Minimum PIO transfer cycle time without flow control



Tiger Series MINI-IDE Industrial Application

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Word	Data	Description
		15-0 Cycle time in nanoseconds
68	0078H	Minimum PIO transfer cycle time with IORDY flow control 15-0 Cycle time in nanoseconds
69-79	0000H	Reserved (for feature command overlap and queuing)
80-81	0000H ...	Reserved for CFA
82	0000H	Features/Command sets supported
83	0000H	Feature/Command sets supported
84	0000H	Features/Command sets supported
85	0000H	Features/Command sets supported
86	0000H	Feature/Command sets supported
87	0000H	Features/Command sets supported
88	0700H	15-14 Reserved 13 1= Ultra DMA mode 5 is selected 0 =Ultra DMA mode 5 is not selected 12 1= Ultra DMA mode 4 is selected 0 =Ultra DMA mode 4 is not selected 11 1= Ultra DMA mode 3 is selected 0 =Ultra DMA mode 3 is not selected 10 1= Ultra DMA mode 2 is selected 0 =Ultra DMA mode 2 is not selected 9 1= Ultra DMA mode 1 is selected 0 =Ultra DMA mode 1 is not selected 8 1= Ultra DMA mode 0 is selected 0 =Ultra DMA mode 0 is not selected 7-6 Reserved 5 0 = Ultra DMA mode 5 and below are not supported 4 1 = Ultra DMA mode 4 and below are supported 3 1 = Ultra DMA mode 3 and below are supported 2 1 = Ultra DMA mode 2 and below are supported 1 1 = Ultra DMA mode 1 and below are supported 0 1 = Ultra DMA mode 0 is supported
89	0000H	Time required for Security erase unit completion
90	0000H	Time required for Enhanced security erase unit completion
91	XXXXH	Current Advanced power management value
92 - 127	0000H	Reserved
128	0000H	Security status
129 - 159	0000H	Vendor unique bytes
160	0000H	Power requirement description



Tiger Series MINI-IDE Industrial Application

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Word	Data	Description
161	0000H	Reserved
162	0000H	Key management schemes supported
163 - 255	0000H	Total 166 Bytes Reserved
Note1:	Variable by capacity	

12. ATA Protocol Overview

Command classes are grouped according to protocols described for command execution. For all commands, the host must first check for `BYS=0` before proceeding further. For most commands, the host should not proceed until `DRDY=1`.

12.1 PIO Data In Commands

Execution includes one more 512 bytes data-sector drive-to-host transfer. If the drive presents error status, it prepares to transfer data at the host's discretion. The host writes parameters to the Feature, Sector Count, Sector Number, Cylinder, and Drive/Head register. The host writes the Command Register's command code. The drive sets `BSY` and prepares for data transfer when a data sector is available; the drive sets `DRQ`, clears `BSY`, and asserts interrupt. At interrupt, the host reads the Status register, the drive negates interrupt, and the host reads one data-sector from Data Register. The drive clears `DRQ`. If another sector is required, the drive sets `BSY` and repeats the data transfer from 4.

12.2 PIO Data Out Commands

Execution includes one or more 512 bytes host-to-drive data-sector transfers. The host writes parameters to the Features, Sector Count, Sector Number, Cylinder, and Drive/Head Registers. The host writes the Command register's command code. The drive sets `DRQ` when it can accept the first sector of data

The host writes one sector of data to the Data register. The Drive clears `DRQ` and sets `BSY`. At sector processing complete, the drive clears `BSY` and asserts interrupt. If another sector transfer is required, the drive also sets `DRQ`. The host reads the Status register after detecting interrupt. The drive negates the interrupt if another sector transfer is required, the sequence repeats from 4.

12.3 Non Data Commands

Command execution involves no data transfer. The host writes parameters to the Features, Sector Count, Sector Number, Cylinder, and Drive/Head registers. The host writes the Command register's command code. The Drive sets `BSY`. When the drive completes sector processing, it clears `BSY` and asserts interrupt. The host reads the Status register after detecting interrupts the drive negates the interrupt.

14. Ultra DMA data-in commands

14.1. Initiating an Ultra DMA data-in burst

The following steps shall occur in the order they are listed unless otherwise specified.

- a) The host shall keep DMACK- in the negated state before an Ultra DMA burst is initiated.
- b) The device shall assert DMARQ to initiate an Ultra DMA burst when DMACK- is negated. After assertion of DMARQ the device shall not negate DMARQ until after the first negation of DSTROBE.
- c) Steps (c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP.
- d) The host shall negate HDMARDY-.
- e) The host shall negate CS0-, CS1-, DA2, DA1, and DA0. The host shall keep CS0-, CS1-, DA2, DA1, and DA0 negated until after negating DMACK- at the end of the burst.
- f) Steps (c), (d), and (e) shall have occurred at least t_{ACK} before the host asserts DMACK-. The host shall keep DMACK- asserted until the end of an Ultra DMA burst.
- g) The host shall release DD(15:0) within t_{AZ} after asserting DMACK-.
- h) The device may assert DSTROBE t_{ZORDY} after the host has asserted DMACK-. Once the device has driven DSTROBE the device shall not release DSTROBE until after the host has negated DMACK- at the end of an Ultra DMA burst.
- i) The host shall negate STOP and assert HDMARDY- within t_{ENV} after asserting DMACK-. After negating STOP and asserting HDMARDY-, the host shall not change the state of either signal until after receiving the first negation of DSTROBE from the device (i.e., after the first data word has been received).
- j) The device shall drive DD(15:0) no sooner than t_{ZAD} after the host has asserted DMACK-, negated STOP, and asserted HDMARDY-.
- k) The device shall drive the first word of the data transfer onto DD(15:0). This step may occur when the device first drives DD(15:0) in step (j).
- l) To transfer the first word of data the device shall negate DSTROBE within t_{FS} after the host has negated STOP and asserted HDMARDY-. The device shall negate DSTROBE no sooner than t_{DVS} after driving the first word of data onto DD(15:0).

14.2. The data-in transfer

The following steps shall occur in the order they are listed unless otherwise specified.

- a) The device shall drive a data word onto DD(15:0).
- b) The device shall generate a DSTROBE edge to latch the new word no sooner than t_{DVS} after changing the state of DD(15:0). The device shall generate a DSTROBE edge no more frequently than t_{CYC} for the



Tiger Series MINI-IDE Industrial Application

C-ONE TECHNOLOGY Corp.

selected Ultra DMA mode. The device shall not generate two rising or two falling DSTROBE edges more frequently than t_{2cyc} for the selected Ultra DMA mode.

- c) The device shall not change the state of DD(15:0) until at least t_{DVH} after generating a DSTROBE edge to latch the data.
- d) The device shall repeat steps (a), (b), and (c) until the Ultra DMA burst is paused or terminated by the device or host.

14.3. Pausing an Ultra DMA data-in burst

The following steps shall occur in the order they are listed unless otherwise specified.

14.3.1. Device pausing an Ultra DMA data-in burst

- a) The device shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
- b) The device shall pause an Ultra DMA burst by not generating additional DSTROBE edges. If the host is ready to terminate the Ultra DMA burst.
- c) The device shall resume an Ultra DMA burst by generating a DSTROBE edge.

14.3.2. Host pausing an Ultra DMA data-in burst

- a) The host shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
- b) The host shall pause an Ultra DMA burst by negating HDMARDY-.
- c) The device shall stop generating DSTROBE edges within t_{RFS} of the host negating HDMARDY-.
- d) When operating in Ultra DMA modes 2, 1, or 0: If the host negates HDMARDY- within t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero or one additional data words; or, if the host negates HDMARDY- greater than t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero, one or two additional data words. While operating in Ultra DMA modes 4 or 3 the host shall be prepared to receive zero, one, two or three additional data words after negating HDMARDY-. The additional data words are a result of cable round trip delay and t_{RFS} timing for the device.
- e) The host shall resume an Ultra DMA burst by asserting HDMARDY-.

14.3.3. Terminating an Ultra DMA data-in burst

14.3.3.1. Device terminating an Ultra DMA data-in burst

Burst termination is completed when the termination protocol has been executed and DMACK- negated. The device shall terminate an Ultra DMA burst before command completion.

The following steps shall occur in the order they are listed unless otherwise specified.



- The device shall initiate termination of an Ultra DMA burst by not generating additional DSTROBE edges.
- The device shall negate DMARQ no sooner than t_{SS} after generating the last DSTROBE edge. The device shall not assert DMARQ again until after DMACK- has been negated.
- The device shall release DD(15:0) no later than t_{AZ} after negating DMARQ.
- The host shall assert STOP within t_{LI} after the device has negated DMARQ. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
- The host shall negate HDMARDY- within t_{LI} after the device has negated DMARQ. The host shall continue to negate HDMARDY- until the Ultra DMA burst is terminated. Steps (d) and (e) may occur at the same time.
- The host shall drive DD(15:0) no sooner than t_{ZAH} after the device has negated DMARQ. For this step, the host may first drive DD(15:0) with the result of the host CRC calculation (see 9.15);
- If DSTROBE is negated, the device shall assert DSTROBE within t_{LI} after the host has asserted STOP. No data shall be transferred during this assertion. The host shall ignore this transition on DSTROBE. DSTROBE shall remain asserted until the Ultra DMA burst is terminated.
- If the host has not placed the result of the host CRC calculation on DD(15:0) since first driving DD(15:0) during (f), the host shall place the result of the host CRC calculation on DD(15:0) (see 9.15).
- The host shall negate DMACK- no sooner than t_{MLI} after the device has asserted DSTROBE and negated DMARQ and the host has asserted STOP and negated HDMARDY-, and no sooner than t_{DVS} after the host places the result of the host CRC calculation on DD(15:0).
- The device shall latch the host's CRC data from DD(15:0) on the negating edge of DMACK-.
- The device shall compare the CRC data received from the host with the results of the device CRC calculation. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command the device shall report the first error that occurred (see 9.15).
- The device shall release DSTROBE within t_{ORDYZ} after the host negates DMACK-.
- The host shall not negate STOP nor assert HDMARDY- until at least t_{ACK} after negating DMACK-.
- The host shall not assert DIOR-, CS0-, CS1-, DA2, DA1, or DA0 until at least t_{ACK} after negating DMACK.

14.3.3.2. Host terminating an Ultra DMA data-in burst

The following steps shall occur in the order they are listed unless otherwise specified.

- a) The host shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.
- b) The host shall initiate Ultra DMA burst termination by negating HDMARDY-. The host shall continue to negate HDMARDY- until the Ultra DMA burst is terminated.
- c) The device shall stop generating DSTROBE edges within t_{RFS} of the host negating HDMARDY-.
- d) When operating in Ultra DMA modes 2, 1, or 0: If the host negates HDMARDY- within t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero or one additional



Tiger Series MINI-IDE Industrial Application

C-ONE TECHNOLOGY Corp.

data words; or, if the host negates HDMARDY- greater than t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero, one or two additional data words. While operating in Ultra DMA modes 4 or 3 the host shall be prepared to receive zero, one, two or three additional data words after negating HDMARDY-. The additional data words are a result of cable round trip delay and t_{RFS} timing for the device.

- e) The host shall assert STOP no sooner than t_{RP} after negating HDMARDY-. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
- f) The device shall negate DMARQ within t_{LI} after the host has asserted STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.
- g) If DSTROBE is negated, the device shall assert DSTROBE within t_{LI} after the host has asserted STOP. No data shall be transferred during this assertion. The host shall ignore this transition on DSTROBE. DSTROBE shall remain asserted until the Ultra DMA burst is terminated.
- h) The device shall release DD(15:0) no later than t_{AZ} after negating DMARQ.
- i) The host shall drive DD(15:0) no sooner than t_{ZAH} after the device has negated DMARQ. For this step, the host may first drive DD(15:0) with the result of the host CRC calculation .
- j) If the host has not placed the result of the host CRC calculation on DD(15:0) since first driving DD(15:0) during (9), the host shall place the result of the host CRC calculation on DD(15:0).
- k) The host shall negate DMACK- no sooner than t_{MLI} after the device has asserted DSTROBE and negated DMARQ and the host has asserted STOP and negated HDMARDY-, and no sooner than t_{DVS} after the host places the result of the host CRC calculation on DD(15:0).
- l) The device shall latch the host's CRC data from DD(15:0) on the negating edge of DMACK-.
- m) The device shall compare the CRC data received from the host with the results of the device CRC calculation. If a miscompare error occurs during one or more Ultra DMA burst for any one command, at the end of the command, the device shall report the first error that occurred.
- n) The device shall release DSTROBE within t_{ORDYZ} after the host negates DMACK-.
- o) The host shall neither negate STOP nor assert HDMARDY- until at least t_{ACK} after the host has negated DMACK-.
- p) The host shall not assert DIOR-, CS0-, CS1-, DA2, DA1, or DA0 until at least t_{ACK} after negating DMACK.



14.4. Ultra DMA data-out commands

14.4.1. Initiating an Ultra DMA data-out burst

The following steps shall occur in the order they are listed unless otherwise specified.

- a) The host shall keep DMACK- in the negated state before an Ultra DMA burst is initiated.
- b) The device shall assert DMARQ to initiate an Ultra DMA burst when DMACK- is negated.
- c) Steps (c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP.
- d) The host shall assert HSTROBE.
- e) The host shall negate CS0-, CS1-, DA2, DA1, and DA0. The host shall keep CS0-, CS1-, DA2, DA1, and DA0 negated until after negating DMACK- at the end of the burst.
- f) Steps (c), (d), and (e) shall have occurred at least t_{ACK} before the host asserts DMACK-. The host shall keep DMACK- asserted until the end of an Ultra DMA burst.
- g) The device may negate DDMARDY- t_{ZORDY} after the host has asserted DMACK-. Once the device has negated DDMARDY-, the device shall not release DDMARDY- until after the host has negated DMACK- at the end of an Ultra DMA burst.
- h) The host shall negate STOP within t_{ENV} after asserting DMACK-. The host shall not assert STOP until after the first negation of HSTROBE.
- i) The device shall assert DDMARDY- within t_{LJ} after the host has negated STOP. After asserting DMARQ and DDMARDY- the device shall not negate either signal until after the first negation of HSTROBE by the host.
- j) The host shall drive the first word of the data transfer onto DD(15:0). This step may occur any time during Ultra DMA burst initiation.
- k) To transfer the first word of data: the host shall negate HSTROBE no sooner than t_{UI} after the device has asserted DDMARDY-. The host shall negate HSTROBE no sooner than t_{DVS} after the driving the first word of data onto DD(15:0).

14.4.2. The data-out transfer

The following steps shall occur in the order they are listed unless otherwise specified.

- a) The host shall drive a data word onto DD(15:0).
- b) The host shall generate an HSTROBE edge to latch the new word no sooner than t_{DVS} after changing the state of DD(15:0). The host shall generate an HSTROBE edge no more frequently than t_{CYC} for the selected Ultra DMA mode. The host shall not generate two rising or falling HSTROBE edges more frequently than t_{2CYC} for the selected Ultra DMA mode.
- c) The host shall not change the state of DD(15:0) until at least t_{DVH} after generating an HSTROBE edge to latch the data.



- d) The host shall repeat steps (a), (b), and (c) until the Ultra DMA burst is paused or terminated by the device or host.

14.4.3. Pausing an Ultra DMA data-out burst

The following steps shall occur in the order they are listed unless otherwise specified.

14.4.3.1 Host pausing an Ultra DMA data-out burst

- a) The host shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
- b) The host shall pause an Ultra DMA burst by not generating an HSTROBE edge. If the host is ready to terminate the Ultra DMA burst.
- c) The host shall resume an Ultra DMA burst by generating an HSTROBE edge .

12.4.3.2. Device pausing an Ultra DMA data-out burst

- a) The device shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
- b) The device shall pause an Ultra DMA burst by negating DDMARDY-.
- c) The host shall stop generating HSTROBE edges within t_{RFS} of the device negating DDMARDY-.
- d) When operating in Ultra DMA modes 2, 1, or 0: If the device negates DDMARDY- within t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero or one additional data words; or, if the device negates DDMARDY- greater than t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero, one or two additional data words. While operating in Ultra DMA modes 4 or 3 the device shall be prepared to receive zero, one, two or three additional data words after negating DDMARDY-. The additional data words are a result of cable round trip delay and t_{RFS} timing for the host.
- e) The device shall resume an Ultra DMA burst by asserting DDMARDY-.

14.4.4. Terminating an Ultra DMA data-out burst

14.4.4.1 Host terminating an Ultra DMA data-out burst

The following steps shall occur in the order they are listed unless otherwise specified.

- a) The host shall initiate termination of an Ultra DMA burst by not generating additional HSTROBE edges.
- b) The host shall assert STOP no sooner than t_{SS} after the last generated an HSTROBE edge. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
- c) The device shall negate DMARQ within t_{LJ} after the host asserts STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.
- d) The device shall negate DDMARDY- within t_{LJ} after the host has negated STOP. The device shall not assert DDMARDY- again until after the Ultra DMA burst termination is complete.



- e) If HSTROBE is negated, the host shall assert HSTROBE within t_{LI} after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition on HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.
- f) The host shall place the result of the host CRC calculation on DD(15:0)
- g) The host shall negate DMACK- no sooner than t_{MLI} after the host has asserted HSTROBE and STOP and the device has negated DMARQ and DDMARDY-, and no sooner than t_{DVS} after placing the result of the host CRC calculation on DD(15:0).
- h) The device shall latch the host's CRC data from DD(15:0) on the negating edge of DMACK-.
- i) The device shall compare the CRC data received from the host with the results of the device CRC calculation. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command, the device shall report the first error that occurred.
- j) The device shall release DDMARDY- within t_{ORDYZ} after the host has negated DMACK-.
- k) The host shall neither negate STOP nor negate HSTROBE until at least t_{ACK} after negating DMACK-.
- l) The host shall not assert DIOW-, CS0-, CS1-, DA2, DA1, or DA0 until at least t_{ACK} after negating DMACK.

14.4.4.2 Device terminating an Ultra DMA data-out burst

Burst termination is completed when the termination protocol has been executed and DMACK- negated. The device shall terminate an Ultra DMA burst before command completion. The following steps shall occur in the order they are listed unless otherwise specified.

- a) The device shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.
- b) The device shall initiate Ultra DMA burst termination by negating DDMARDY-.
- c) The host shall stop generating an HSTROBE edges within t_{RFS} of the device negating DDMARDY-.
- d) When operating in Ultra DMA modes 2, 1, or 0: If the device negates DDMARDY- within t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero or one additional data words; or, if the device negates DDMARDY- greater than t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero, one or two additional data words. While operating in Ultra DMA modes 4 or 3 the device shall be prepared to receive zero, one, two or three additional data words after negating DDMARDY-. The additional data words are a result of cable round trip delay and t_{RFS} timing for the host.
- e) The device shall negate DMARQ no sooner than t_{RP} after negating DDMARDY-. The device shall not assert DMARQ again until after DMACK- is negated.
- f) The host shall assert STOP within t_{LI} after the device has negated DMARQ. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
- g) If HSTROBE is negated, the host shall assert HSTROBE within t_{LI} after the device has negated



Tiger Series MINI-IDE Industrial Application

C-ONE TECHNOLOGY Corp.

DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition of HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.

- h) The host shall place the result of the host CRC calculation on DD(15:0).
- i) The host shall negate DMACK- no sooner than t_{MLI} after the host has asserted HSTROBE and STOP and the device has negated DMARQ and DDMARDY-, and no sooner than t_{DVS} after placing the result of the host CRC calculation on DD(15:0).
- j) The device shall latch the host's CRC data from DD(15:0) on the negating edge of DMACK-.
- k) The device shall compare the CRC data received from the host with the results of the device CRC calculation. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command, the device shall report the first error that occurred.
- l) The device shall release DDMARDY- within t_{IORDYZ} after the host has negated DMACK-.
- m) The host shall neither negate STOP nor HSTROBE until at least t_{ACK} after negating DMACK-.
- n) The host shall not assert DIOW-, CS0-, CS1-, DA2, DA1, or DA0 until at least t_{ACK} after negating DMACK.

14.5. Ultra DMA CRC rules

The following is a list of rules for calculating CRC, determining if a CRC error has occurred during an Ultra DMA burst, and reporting any error that occurs at the end of a command.

- 1) Both the host and the device shall have a 16-bit CRC calculation function.
- 2) Both the host and the device shall calculate a CRC value for each Ultra DMA burst.
- 3) The CRC function in the host and the device shall be initialized with a seed of 4ABAh at the beginning of an Ultra DMA burst before any data is transferred.
- 4) For each STROBE transition used for data transfer, both the host and the device shall calculate a new CRC value by applying the CRC polynomial to the current value of their individual CRC functions and the word being transferred. CRC is not calculated for the return of STROBE to the asserted state after the Ultra DMA burst termination request has been acknowledged.
- 5) At the end of any Ultra DMA burst the host shall send the results of the host CRC calculation function to the device on DD(15:0) with the negation of DMACK-.
- 6) The device shall then compare the CRC data from the host with the calculated value in its own CRC calculation function. If the two values do not match, the device shall save the error. A subsequent Ultra DMA burst for the same command that does not have a CRC error shall not clear an error saved from a previous Ultra DMA burst in the same command. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, the device shall report the first error that occurred. If the device detects that a CRC error has occurred before data transfer for the command is complete, the device may complete the transfer and report the error or abort the command and report the error.



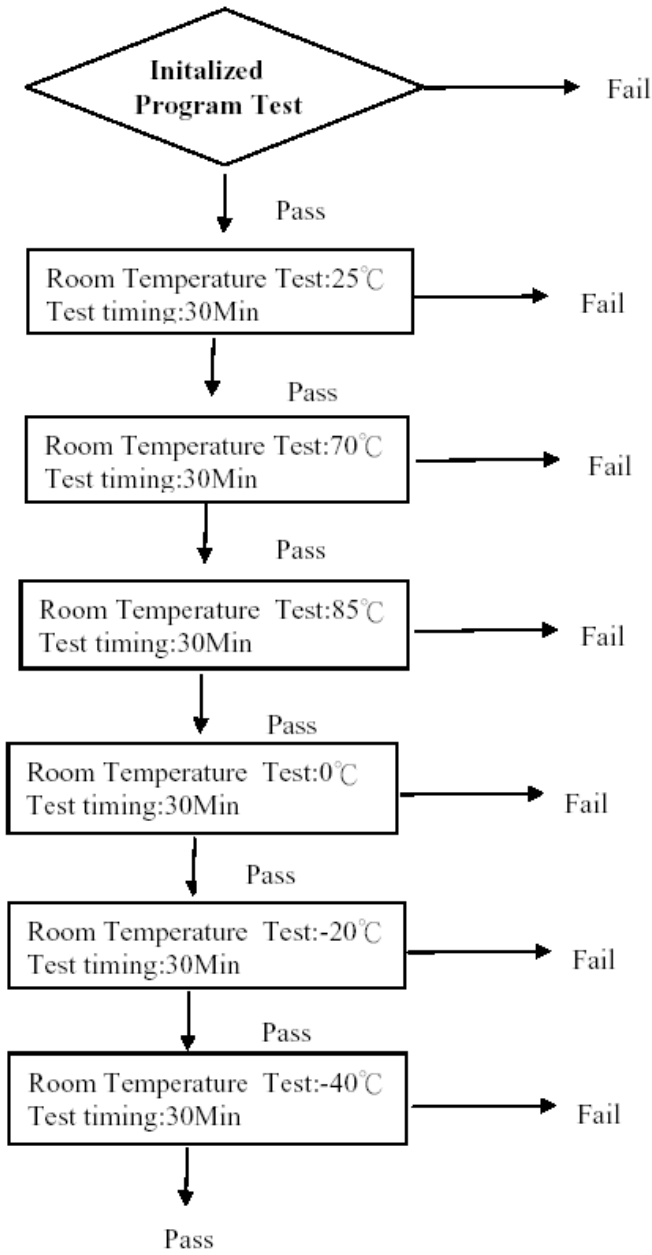
- 7) For READ DMA, WRITE DMA, READ DMA QUEUED, or WRITE DMA QUEUED commands:
When a CRC error is detected, the error shall be reported by setting both ICRC and ABRT (bit 7 and bit 2 in the Error register) to one. ICRC is defined as the “Interface CRC Error” bit. The host shall respond to this error by re-issuing the command.
- 8) For a REQUEST SENSE packet command (see SPC T10/955D for definition of the REQUEST SENSE command):
When a CRC error is detected during transmission of sense data the device shall complete the command and set CHK to one. The device shall report a Sense key of 0Bh (ABORTED COMMAND). The device shall preserve the original sense data that was being returned when the CRC error occurred. The device shall not report any additional sense data specific to the CRC error. The host device driver may retry the REQUEST SENSE command or may consider this an unrecoverable error and retry the command that caused the Check Condition.
- 9) For any packet command except a REQUEST SENSE command:
If a CRC error is detected, the device shall complete the command with CHK set to one. The device shall report a Sense key of 04h (HARDWARE ERROR). The sense data supplied via a subsequent REQUEST SENSE command shall report an ASC/ASCQ value of 08h/03h (LOGICAL UNIT COMMUNICATION CRC ERROR). Host drivers should retry the command that resulted in a HARDWARE ERROR.
- 10) A host may send extra data words on the last Ultra DMA burst of a data-out command. If a device determines that all data has been transferred for a command, the device shall terminate the burst. A device may have already received more data words than were required for the command. These extra words are used by both the host and the device to calculate the CRC, but, on an Ultra DMA data-out burst, the extra words shall be discarded by the device.
- 11) The CRC generator polynomial is: $G(X) = X^{16} + X^{12} + X^5 + 1$. Table 46 describes the equations for 16-bit parallel generation of the resulting polynomial (based on a word boundary).

NOTE Since no bit clock is available, the recommended approach for calculating CRC is to use a word clock derived from the bus strobe. The combinational logic is then equivalent to shifting sixteen bits serially through the generator polynomial where DD0 is shifted in first and DD15 is shifted in last.

NOTE If excessive CRC errors are encountered while operating in an Ultra mode, the host should select a slower Ultra mode. Caution: CRC errors are detected and reported only while operating in an Ultra mode.

15. System Environmental Specifications

15.1 Temperature Test Flow





Tiger Series MINI-IDE Industrial Application
C-ONE TECHNOLOGY Corp.

15.2 Altitude Test

Altitude		Product
Altitude(relative to sea level)	Operating &Non- Operating	80,000 feet maximum