Memoright
Product Data Sheet

M1200

BGA 169/153 Balls
up to 104 MB/sec Bus Transfer Rate
Business Temperature Grade

Revision: 1.1

Date: October 2012
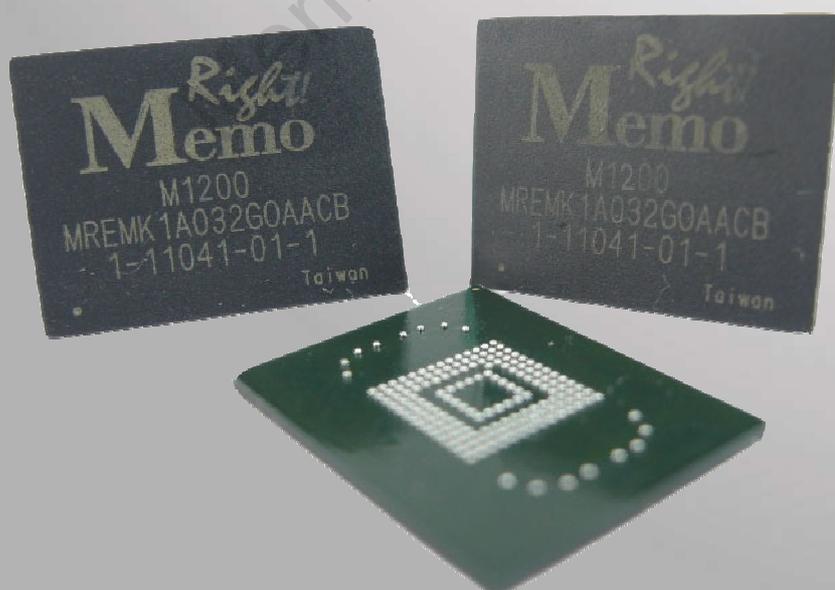
e-MMC 4.41 Embedded Flash Memory – M1200 Series

2Gbytes ~ 64Gbytes

1. Features

◆ **General Features**

- **Embedded with e-MMC Flash Controller and NAND flash**
- **Complies with e-MMC Specification version 4.41**
- **Write-Block Length 512**
- **Support Command Class 0~7**
- **Mechanical design complies with JEDEC Standard No. JESD84-A441**
- **Support multiple data bus widths including 1bit, 4bit and 8bit**
- **Support clock frequency mode: 0-20MHz, 0-26MHz and 0-52 MHz**
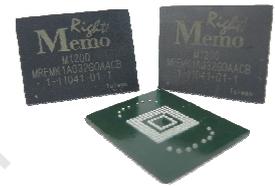
◆ **Form Factor**

- **e-MMC 4.41 Embedded Flash Memory**
- **AA type:12 mm x 16 mm, BA type:11.5 mm x 13 mm**
- **BGA 169 Ball, BGA 153 Ball**
- **Complies with JEDEC MO-276C Specification**

◆ **Available Capacities**

- **2 GB to 64 GB (MLC NAND Flash)**

◆ **Highly integrated controller for NAND Flash memory**

- **MLC NAND Flash**

◆ **Voltages**

- **Core Voltage (VCC) 2.7V~3.6V**
- **I/O (VCCQ) voltage, either: 1.7V~1.95V or 2.7V~3.6V**

◆ **ECC**

- **Internal Error Correction support: BCH: 70bit/1KB correction ECC**

◆ **High Performance**

- **Up to 104 MB/s Bus transfer rate (DDR Mode)**

◆ **High Reliability**

- **MTBF ﹥ 2,100,000 hours**
- **Endurance: ﹥ 3 years sequential write (for a half drive's capacity write per day)**

◆ **Temperature Ranges**

- **Business Temperature Range: -25℃ ~+85℃**
- **Storage Temperature Range: - 40℃ ~+85℃**

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2. Contents

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3. Ordering Information

The following Table 1 lists the part No. for Memoright M1200 series SSDs.

Table 1: Business temperature product list

BGA 169 Ball, 12mm x 16mm			
Part Number	**Capacity**	**Flash Type**	**Form Factor**
MREMK3B016GTHAAB00	16 GB*	MLC	BGA 169 ball
MREMK3B032GTHAAB00	32 GB*	MLC	BGA 169 ball
MREMK3B064GTHAAB00	64 GB*	MLC	BGA 169 ball

BGA 153 Ball, 11.5mm x 13mm			
Part Number	**Capacity**	**Flash Type**	**Form Factor**
MREMK3B002GOBBAB00	2 GB*	MLC	BGA 153 ball
MREMK3B004GOBBAB00	4 GB*	MLC	BGA 153 ball
MREMK3B008GOBBAB00	8 GB*	MLC	BGA 153 ball
MREMK3B016GOBBAB00	16 GB*	MLC	BGA 153 ball

* 1 GB=1,000,000,000 Bytes

For latest ordering information, please consult Memoright's sales representatives or check on our website:

http://www.memoright.com

3.1 Part Number Decoder

MR	EMK3B	****	**	**	B	00
1	2	3	4	5	6	7

MR: Memoright

EMK3B: M1200 Series

Capacity
002G: 2 GB
004G: 4 GB
008G: 8 GB
016G: 16 GB
032G: 32 GB
064G: 64 GB

00: Standard Product

Temperature Option
B: Business (-25℃~+85℃)

**: BA: BGA 11.5mmx13mm
    AA: BGA 12mmx16mm

**: MLC
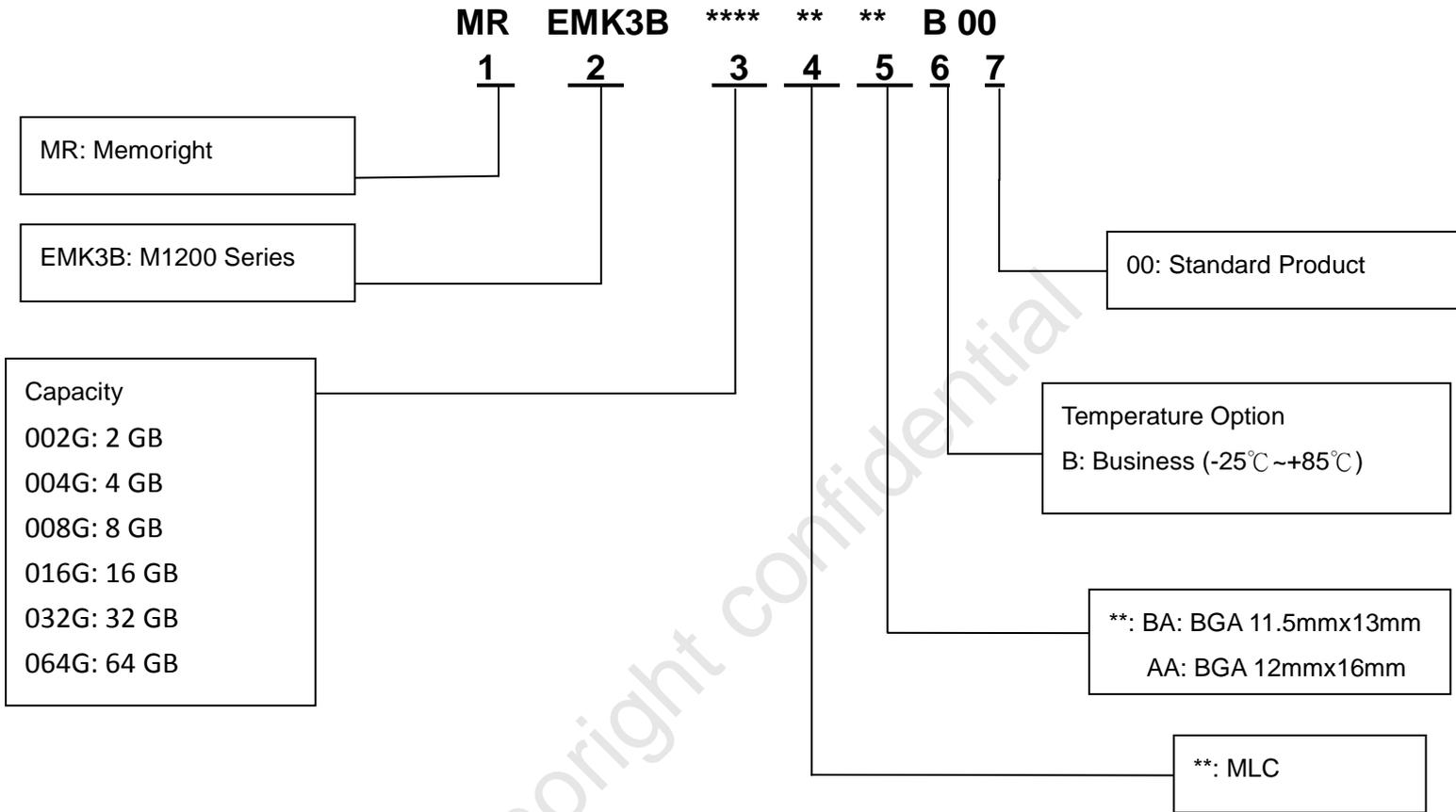
4. General Description

Memoright M1200 series is an eMMC 4.41 compliance embedded flash memory module that **integrates a slim controller** and MLC NAND flash into a **BGA package** for various consumer electronics applications such as smart phones, Tablet PC, GPS, etc.

Memoright M1200 series provides low power mode to greatly **extend battery lifetime** and to **achieve high performance** for up to 64GB storage capacity that makes it an ideal solution for multimedia handsets. M1200 integrates advanced MLC flash management technology to achieve balance between cost and performance. It supports three clock frequencies including **0-20MHz, 0-26MHz and 0-52MHz** and also supports for three different data bus width modes**(1bit, 4bit and 8bit)**. Besides, it i**ntegrates several patented method such as dynamic & static wear-leveling and advance block management** to **achieve highest data reliability and maximized flash life expectancy**.

Memoright M1200's various advantages such as high performance, capacity and reliability make it the best eMMC storage solution for several consumer electronics devices such as mobile PC and personal handheld devices.

4.1   Physical Description

The important component of Memoright M1200 embedded Flash Memory integrates a Flash controller and NAND Flash memory modules. The Memoright M1200 e-MMC embedded Flash memory solution is provided in BGA 169 ball and BGA 153 ball packages.

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4.2   System Performance

Table 2: System Performance Table

System Performance		Max.	Unit
Data transfer Rate (e-MMC 4.41)		104	MB/s
Sustained Sequential Read Rate	2 GB	40*	MB/s
	4 GB	40*	MB/s
	8 GB	80*	MB/s
	16 GB	80*	MB/s
	32 GB	80*	MB/s
	64 GB	80*	MB/s
Sustained Sequential Write Rate	2 GB	8*	MB/s
	4 GB	10*	MB/s
	8 GB	15*	MB/s
	16 GB	25*	MB/s
	32 GB	25*	MB/s
	64 GB	25*	MB/s
4KB Random Read IOPS	2 GB	2,000	IOPS
4KB Random Read IOPS	4 GB	3,000	IOPS
4KB Random Read IOPS	8 GB	3,000	IOPS
4KB Random Read IOPS	16 GB	3,000	IOPS
4KB Random Read IOPS	32 GB	3,000	IOPS
4KB Random Read IOPS	64 GB	3,000	IOPS
4KB Random Write IOPS	2 GB	400	IOPS
4KB Random Write IOPS	4 GB	300	IOPS
4KB Random Write IOPS	8 GB	300	IOPS
4KB Random Write IOPS	16 GB	300	IOPS
4KB Random Write IOPS	32 GB	300	IOPS
4KB Random Write IOPS	64 GB	300	IOPS

*1 GB=1024 Mega Bytes

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4.3 Environmental Specifications

4.3.1 Recommended Operating Conditions

Table 3: Recommended Operating Conditions

Parameter	Value
Business Operating Temperature	-25℃ to +85℃
Temperature Gradient (℃ per hour max, non-condensing)	20℃ (operating)
Temperature Gradient (℃ per hour max, non-condensing)	30℃ (non-operating)
Power Supply Voltage Range (High Voltage Range)	2.7V to 3.6V
Power Supply Voltage Range (Low Voltage Range)	1.7V to 1.95V

4.3.2 Power Consumption (*)

Table 4: Power Consumption

Current/Power Consumption	Max. Current High Voltage Range	Max. Current Low Voltage Range	Unit
Sleep Mode Current	250	240	μA
Read Power	200	200	mA
Write Power	200	200	mA

* All value are tested under room temperature 25℃ @ 3.3V

4.3.3 Recommended Storage Conditions

Table 5: Recommended Storage Conditions

Parameter	Value
Business Storage Temperature	-40℃ to +85℃

4.3.4 Shock, Vibration and Humidity

Table 6: Shock, Vibration and Humidity

Parameter	Value
Humidity, Moisture Sensitivity Level	3
Relative Humidity Gradient	30% per hour max
Vibration	10G (Peak, 10~2000Hz)
Shock (Operating)	1000G, (0.5ms duration, half sine wave)
Shock (Non-Operating)	1500G, (0.5ms duration, half sine wave)

4.4 Reliability

Table 7: Reliability

Parameter	Value
Mean Time Between Failures (MTBF)	> 2,100,000 hours (Calculation mode: Telcordia SR-332 Issue 1 Method 1, Case 1)

4.5   Physical Dimensions

Physical Dimensions	AA Type	BA Type	Unit
Length	12	11.5	mm
Width	16	13	mm
Thickness(Max.)	1.2	1.1	mm

5. Functional Block Diagram

Figure 1: Functional Block Diagram

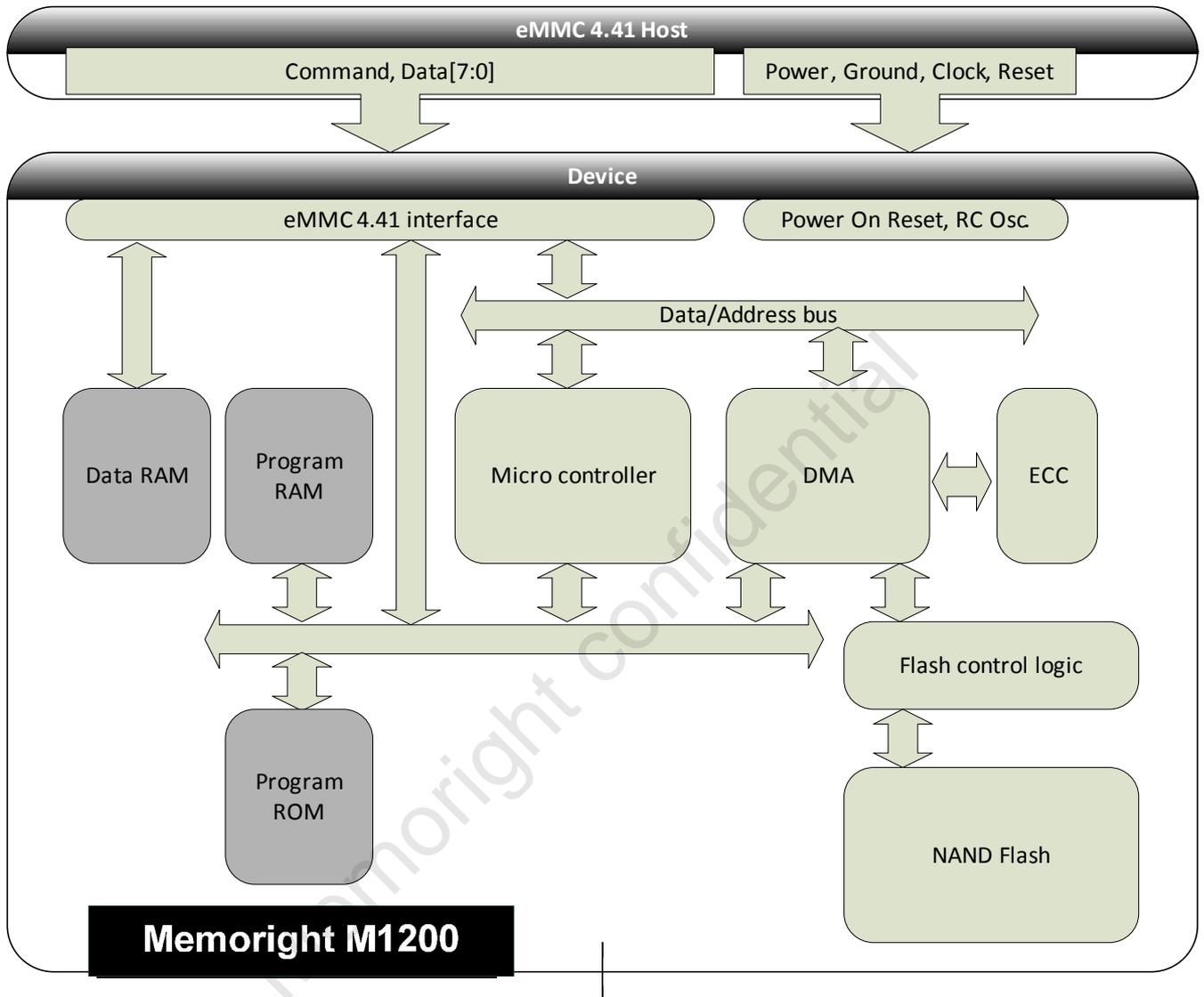**Memoright Corp.**
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6. Physical Dimension Diagram
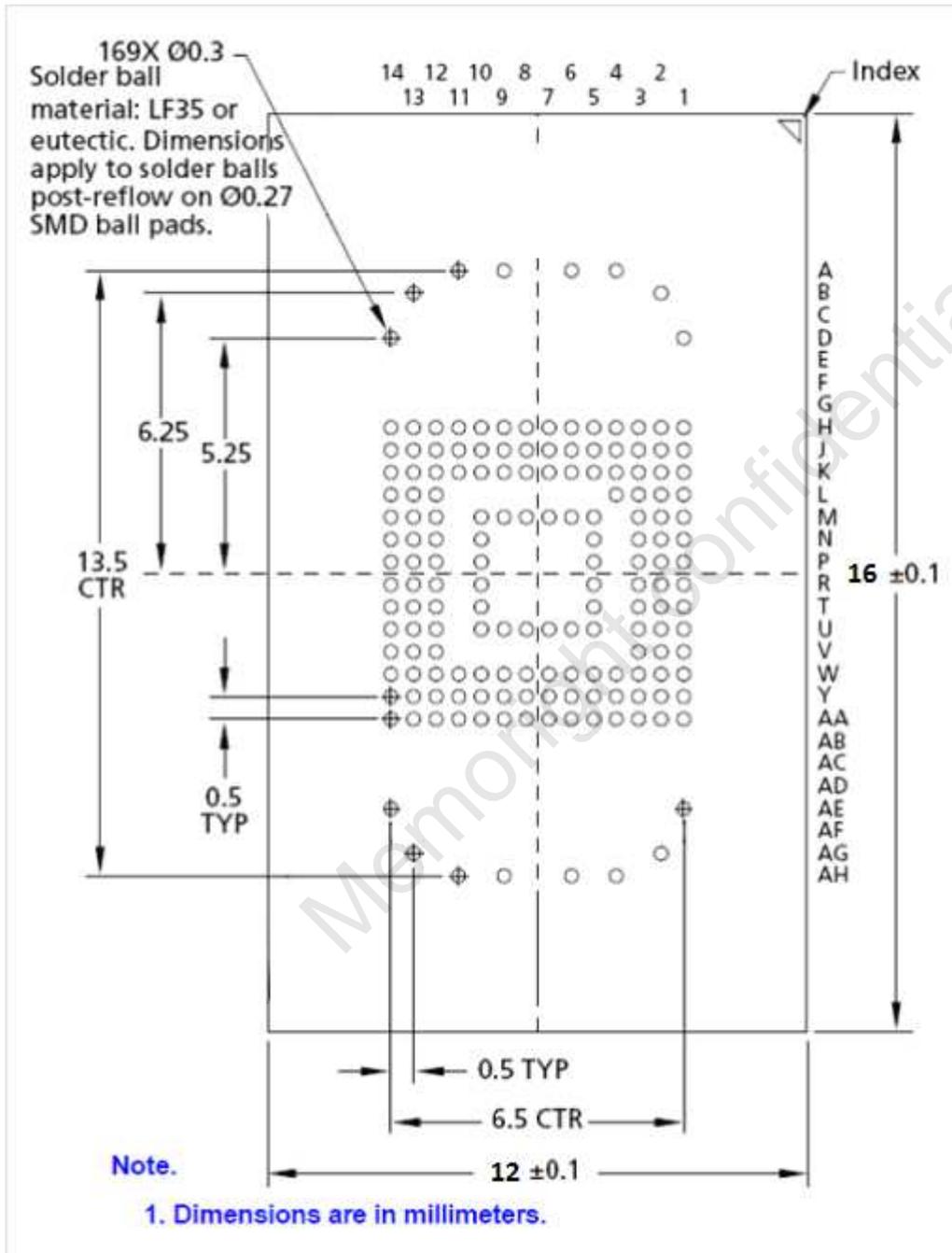
6.1 Rear View: AA format

Figure 2: Physical Dimension (Rear View: AA format)
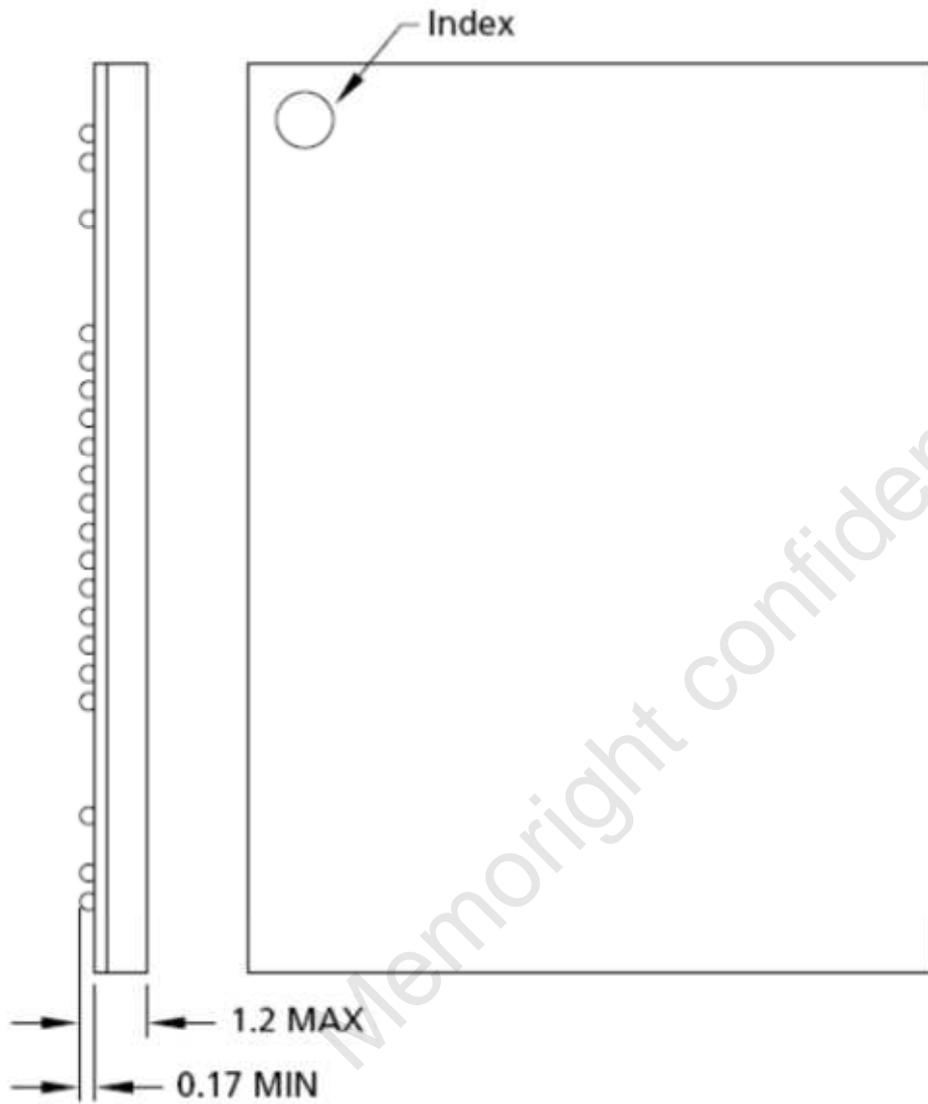
6.2 Side/Front View: AA format
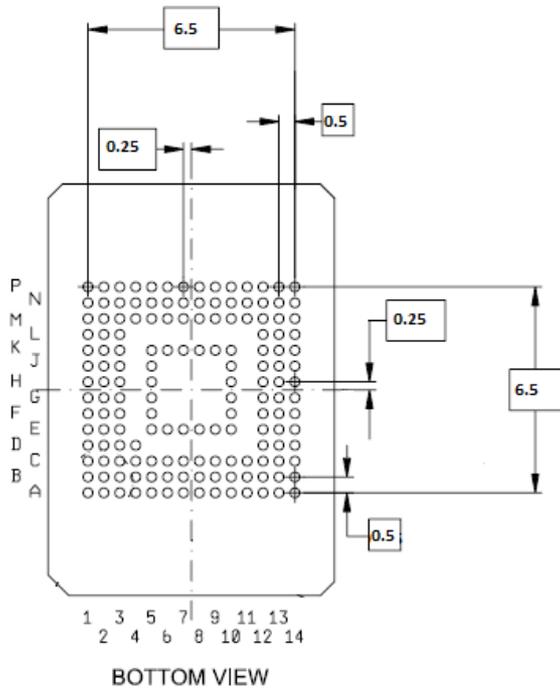

Figure 3 Physical Dimension (Side/Front View: AA format)

Physical Dimensions		Unit
Length	12	mm
Width	16	mm
Thickness(Max.)	1.2	mm

6.3 Rear View: BA format

Figure 4 Rear View: BA format

6.4 Side/Front View: BA format
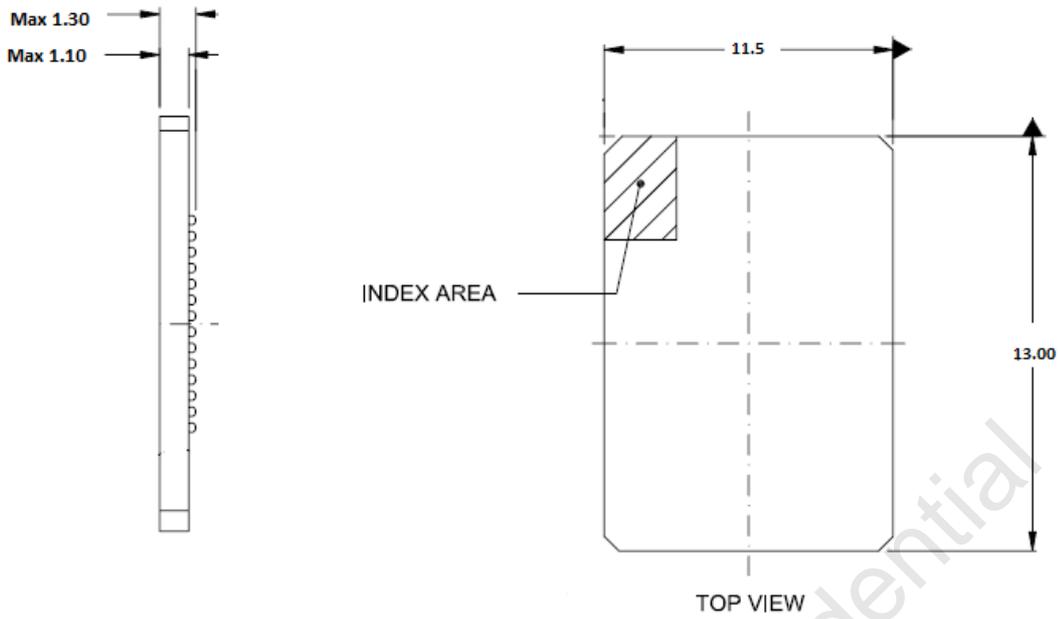
Figure 5 Side/Front View: BA format

Physical Dimensions		Unit
Length	11.5	mm
Width	13	mm
Thickness (Max.)	1.1	mm

7. Electrical Interface

7.1 M1200 Ball Array (Top-View, Ball-Down)
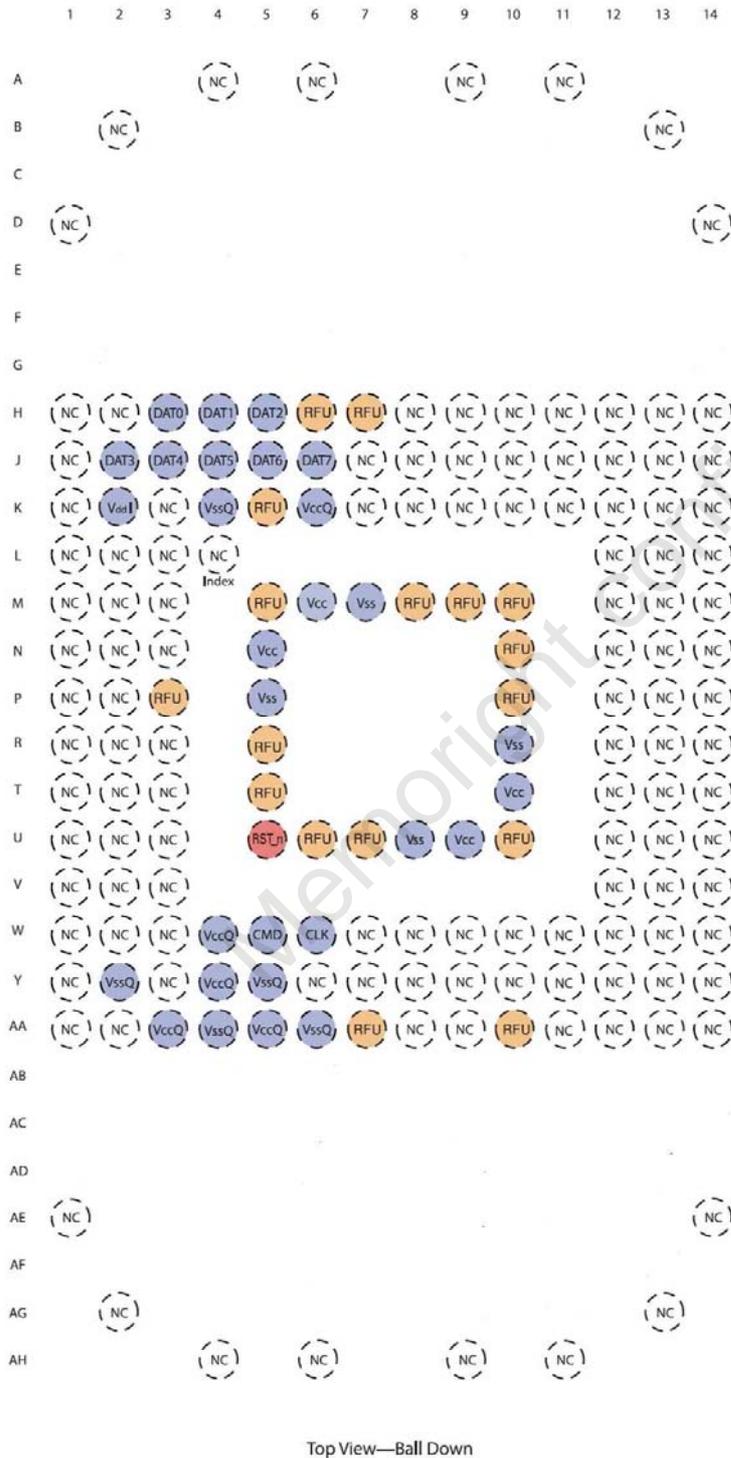
Top View—Ball Down

Figure 6 Memoright M1200 Series 169 pin Ball Array

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7.2   M1200 Ball Array (Top-View, Ball-Down)
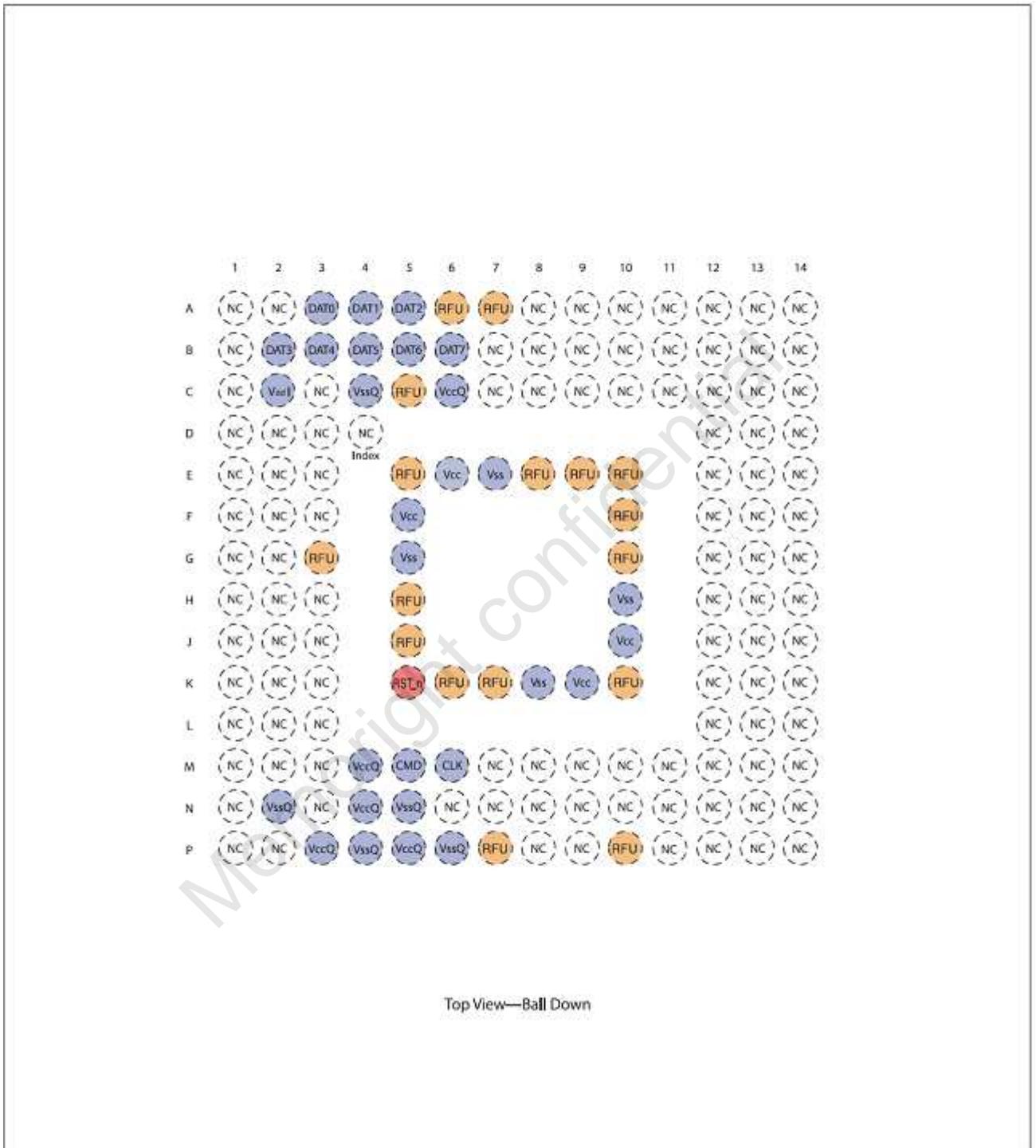
Figure 7   Memoright M1200 Series 153 pin Ball Array

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7.3 Pin and Signal Definition

169 Ball (AA Type)

Table 8 169 Ball Pin and Signal Definition

Pin Name	Signal Name	Input/Output	Description
W6	CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines.
W5	CMD	Input	Command: A bidirectional channel used for device initialization and command transfers. Command has two operating modes: 1) Open-drain for initialization. 2) Push-pull for fast command transfer.
H3	DAT0	I/O	Data I/O0: Bidirectional channel used for data transfer.
H4	DAT1	I/O	Data I/O1: Bidirectional channel used for data transfer.
H5	DAT2	I/O	Data I/O2: Bidirectional channel used for data transfer.
J2	DAT3	I/O	Data I/O3: Bidirectional channel used for data transfer.
J3	DAT4	I/O	Data I/O4: Bidirectional channel used for data transfer.
J4	DAT5	I/O	Data I/O5: Bidirectional channel used for data transfer.
J5	DAT6	I/O	Data I/O6: Bidirectional channel used for data transfer.
J6	DAT7	I/O	Data I/O7: Bidirectional channel used for data transfer.
U5	RST_n	Input	Reset signal pin
M6, N5, T10, U9	VCC	Supply	VCC: Flash memory I/F and Flash memory power supply.
K6, W4, Y4, AA3, AA5	VCCQ	Supply	VCCQ: Memory controller core and MMC interface I/O power supply.
M7, P5, R10, U8	VSS	Supply	VSS: Flash memory I/F and Flash

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			memory ground connection.
K4, Y2, Y5, AA4, AA6	VSSQ	Supply	VSSQ: Memory controller core and MMC I/F ground connection.
K2	VDDi		VDDi: Connect 0.1µF capacitor from VDDi to ground.
L4	NC Index	—	Index: Can be connected to ground or left floating.
A4, A6, A9, A11, B2, B13, D1, D14, H1, H2, H8, H9, H10, H11, H12, H13, H14, J1, J7, J8, J9, J10, J11, J12, J13, J14, K1, K3, K7, K8, K9, K10, K11, K12, K13, K14, L1, L2, L3, L12, L13, L14, M1, M2, M3, M12, M13, M14, N1, N2, N3, N12, N13, N14, P1, P2, P12, P13, P14, R1, R2, R3, R12, R13, R14, T1, T2, T3, T12, T13, T14, U1, U2, U3, U12, U13, U14, V1, V2, V3, V12, V13, V14, W1, W2, W3, W7, W8, W9, W10, W11, W12, W13, W14, Y1, Y3, Y6, Y7, Y8, Y9, Y10, Y11, Y12, Y13, Y14, AA1, AA2, AA8, AA9, AA11, AA12, AA13, AA14, AE1, AE14, AG2, AG13, AH4, AH6, AH9, AH11	NC	—	No connect: Can be connected to ground or left floating.

H6, H7, K5, M5, M8, M9, M10, N10, P3, P10, R5, T5, U6, U7, U10, AA7, AA10	RFU	—	Reserved for future use. Left it floating for future use.

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153 Ball (BA Type)

Table 9 153 Ball Pin and Signal Definition

Pin Name	Signal Name	Input/Output	Description
M6	CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines.
M5	CMD	Input	Command: A bidirectional channel used for device initialization and command transfers. Command has two operating modes: 1) Open-drain for initialization. 2) Push-pull for fast command transfer.
A3	DAT0	I/O	Data I/O0: Bidirectional channel used for data transfer.
A4	DAT1	I/O	Data I/O1: Bidirectional channel used for data transfer.
A5	DAT2	I/O	Data I/O2: Bidirectional channel used for data transfer.
B2	DAT3	I/O	Data I/O3: Bidirectional channel used for data transfer.
B3	DAT4	I/O	Data I/O4: Bidirectional channel used for data transfer.
B4	DAT5	I/O	Data I/O5: Bidirectional channel used for data transfer.
B5	DAT6	I/O	Data I/O6: Bidirectional channel used for data transfer.
B6	DAT7	I/O	Data I/O7: Bidirectional channel used for data transfer.
K5	RST_n	Input	Reset signal pin
E6,F5,J10,K9	VCC	Supply	VCC: Flash memory I/F and Flash memory power supply.
C6,M4,N4,P3,P5	VCCQ	Supply	VCCQ: Memory controller core and MMC interface I/O power supply.
E7,G5,H10,K8	VSS	Supply	VSS: Flash memory I/F and Flash memory ground connection.

C4,N2,N5,P4,P6	VSSQ	Supply	VSSQ: Memory controller core and MMC I/F ground connection.
C2	VDDi		VDDi: Connect 0.1µF capacitor from VDDi to ground.
D4	NC Index	—	Index: Can be connected to ground or left floating.
A1,A2,A8,A9,A10, A11,A12,A13,A14, B1,B7,B8,B9,B10, B11,B12,B13,B14 C1,C3,C7,C8,C9, C10,C11,C12,C13 C14,D1,D2,D3,D12, D13,D14,E1,E2,E3, E12,E13,E14,F1,F2, F3,F12,F13,F14,G1, G2,G12,G13,G14,H1, H2,H3,H12,H13,H14, J1,J2,J3,J12,J13,J14, K1,K2,K3,K12,K13,K14, L1,L2,L3, L12,L13,L14, M1, M2, M3, M7, M8, M9, M10, M11, M12,M13,M14,N1,N3, N6,N7,N8,N9,N10,N11, N12,N13,N14,P1,P2,P8 ,P9, P11,P12,P13,P14	NC	—	No connect: Can be connected to ground or left floating.
A6,A7,C5,E5,E8 E9,E10,F10,G3 G10,H5,J5,K6,K7 K10,P7,P10	RFU	—	Reserved for future use. Left it floating for future use.

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8. Product Features

The Memoright M1200 contain with a high-speed MultiMediaCard (MMC) controller and Multi-Level Cell (MLC) NAND Flash package in to a low profile BGA package. With functions performance by the controller like error correction code (ECC), wear leveling, and bad block management, the M1200 controller simply transform a program/erase/read device with bad blocks and bad bits (NAND) into a simple write/read memory.

8.1　MMC bus and Power Lines

Memoright M1200 with MMC interface supports the MMC protocol. For more details regarding these buses refer to JEDEC Standard No. 84-A441. The Memoright M1200 has the following command line show as Table 1.

Table 10 M1200 Command Line List

Command	Description
CMD	This signal is a bidirectional command channel used for device initialization and command transfers. The CMD signal has two operating modes: open-drain for initialization, and push-pull for command transfer. Commands are sent from the MMC bus master to the device, and responses are sent from the device to the host.
DAT [7:0]	These are bidirectional data signals. The DAT signals operate in push-pull mode. By default, after power-up or RESET, only DAT0 is used for data transfer. The memory controller can configure a wider data bus for data transfer using either DAT[3:0] (4-bit mode) or DAT[7:0] (8-bit mode).
CLK	Each cycle of the clock directs a transfer on the command line and on the data line(s).The frequency can vary between the minimum and the maximum clock frequency.
RST_n	Reset signal is used for host resetting device, moving the device to pre-idle state. By default, the RST_n signal is temporary disabled in device. Host need to set bit[0:1] in the extended CSD register [162] to 0x1 to enable this functionality before the host uses.
VCCQ	VCCQ is the supply voltage for host interface
VCC	Flash memory I/F and Flash memory power supply.
VDDi	Connect 0.1µF capacitor to stabilize regulator output to controller core logics
VSS/VSSQ	ground lines

8.2 Bus Operating Condition

Table 11 M1200 Command Line List

Parameter	Symbol	Min	Max.	Unit
Peak voltage on all lines		-0.5	VCCQ + 0.5	V
All Inputs				
Input Leakage Current (before initialization sequence and/or the internal pull up resistors connected)		-100	100	µA
Input Leakage Current (after initialization sequence and the internal pull up resistors disconnected)		-2	2	µA
All Outputs				
Output Leakage Current (before initialization sequence)		-100	100	µA
Output Leakage Current (after initialization sequence)		-2	2	µA

Table 12 Dual Voltage Power Supply

Parameter	Symbol	Min	Max.	Unit	Remarks
Supply voltage (low voltage range)	VDDL	1.70	1.95	V	1.95V~2.7 V range is not supported
Supply voltage (high voltage range)	VDDH	2.7	3.6	V	
Supply voltage differentials (VSS1, VSS2)		-0.5	0.5	V	
Supply power-up (low voltage range)	tPRUL	-	25	ms	
Supply power-up (high voltage range)	tPRUH	-	35	ms	

The M1200 supports one or more combinations of VCC and VCCQ as shown in Table 4. The VCCQ must be defined at equal to or less than VCC. The available voltage configuration is shown in Table 5

Table 13 M1200 power supply voltage

Parameter	Symbol	Min	Max.	Unit	Remarks
Supply voltage (NAND)	VCC	2.7	3.6	V	
Supply voltage (I/O)	VCCQ	2.7	3.6	V	
		1.65	1.95	V	
Supply power-up for 3.3V	tPRUH		35	ms	
Supply power-up for 1.8V			25	ms	
Supply power-up for 1.2V			20	ms	

8.3   Endurance

The endurance of the SSD is > 5 years sequential write (for a full drive's capacity write per day).

8.4   ECC

The SSD provides Enhanced ECC algorithm which reduces error rate and enforces write endurance at the same time. The ECC rate is BCH: 70bit/1KB correction ECC.

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9. M1200 e-MMC 4.41 Supported Features

9.1 Bootable

Memoright M1200 supports boot operation modes accordingly to eMMC 4.41 interface definition as specified by JEDEC.

9.1.1 Timing for Boot Operation

The following diagram show Multimedia Card state and timing diagram for normal boot mode. The operation detail for the boot operation is described as following.

If the CMD line is held LOW for 74 clock cycles and more after power-up or reset (no matter through CMD0 with the argument of 0xF0F0F0F0 or assertion of hardware reset for e-MMC, If it is enabled in Extended CSD register byte [162], bits [1:0]) before the first command is issued, the boot data will be prepared internally by the slave once it recognizes that the boot mode is being initiated. The partition from which the master will read the boot data can be selected in advance by using EXT_CSD byte [179], bits [5:3]. The data size 128KB xBOOT_SIZE_MULT (EXT_CSD byte [226]). After the CMD line goes low and within 1 second, the slave starts to send the first boot data to the master on the DAT line (s). The CMD line must be kept LOW by the master to read all of the boot data. The push-pull mode must be used by the master until boot operation is terminated. The master can choose to use single data rate mode with backward-compatible interface timing, single data rate with high-speed interface timing or dual data rate timing (if it supported). The master can choose to receive boot acknowledge from the slave by setting "1" in EXIT_CSD register, byte [179], bit6. And then the master recognizes that the slave is operating in boot mode. The slave has to send acknowledge pattern "010" to the master within 50ms after the CMD goes low if boot acknowledge is enabled. The acknowledge pattern "0-1-0" will not be sent out by the slave if boot acknowledge is disabled. The boot mode can be terminated by the master with the CMD line is High. If the CMD line is pulled High by the master in the middle of data transfer, the slave has to terminate the data transfer or acknowledge pattern within NST clock cycles (one data cycle and end bit cycle). If the boot mode is terminated by the master between consecutive blocks, the slave must release the data line(s) within NST clock cycles.

When all contents of the enabled boot data are sent to the master, boot operation will be terminated. After boot operation is executed, the slave shall be ready for CMD1 operation and the master needs to start a normal MMC initialization sequence by sending CMD1. From CMD signal high to next MMC command, it needs minimum 8 clocks + 48 clocks = 56 clocks. Before CMD1 is issued, if the CMD line is held LOW for less than 74 clock cycles after power-up or the master sends any normal MMC command other than CMD0 with argument 0xFFFFFFFA before initiating boot mode, the slave shall not respond and shall be locked out of boot mode until the next power cycle or hardware reset, and shall enter Idle State. Slave must enter Card Identification Mode and respond to the command when BOOT_PARTITION_ENABLE bits are set and master send CMD1

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(SEND_OP_COND). If the boot operation mode is not supported by the slave that is compliant with v4.2 or before or BOOT_PARTITION_ENABLE bit is cleared, slave automatically enter Idle State after power-on.
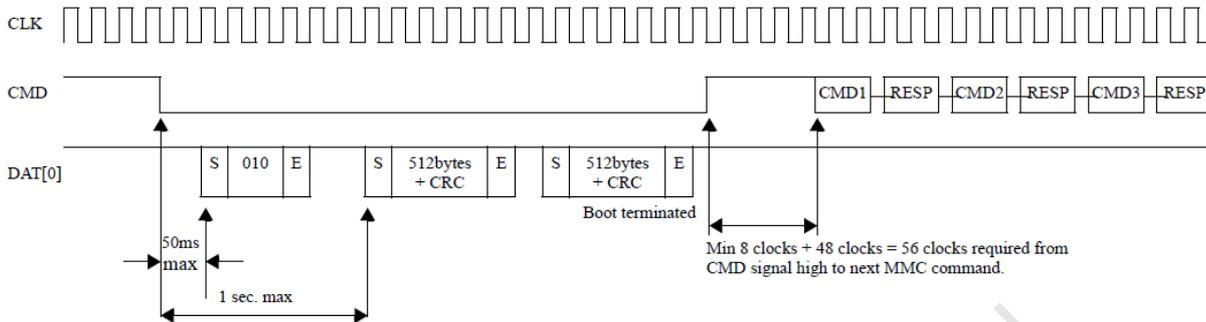

Figure 8 Multimedia Card State & Timing Diagram (Boot Mode)

9.1.2 Alternative Boot Operation

This boot function is compulsory for v4.4 or newer standard. Device that is compliant with v4.4 standard will show "1" bit 0 in the Extended CSD byte [228]. The slave will recognize that boot mode is being initiated and starts preparing boot data internally, if the host issues CMD0 with the argument of 0xFFFFFFFA after 74 clock cycles before CMD1 is issued or the CMD line goes low when the device is powered-up or reset (either assertion of CMD0 with the argument of 0xF0F0F0F0 or H/W reset if it is enabled). The partition from which the master will read the boot data can be selected in advance using EXT_CSD byte [179], bits [5:3]. 128KB xBOOT_SIZE_MULT (EXT_CSD byte [226] is the data size that the master can read during boot operation. The slave starts to send the first boot data to the master on the DAT line(s) within 1 second after CMD with the argument of 0xFFFFFFFA is issued within 1 second. The master must use push-pull mode until boot operation is terminated. The master can choose to use single data rate with high-speed interface timing or dual rate timing (if it is supported), single data rate mode with backward-compatible interface timing. The master can choose to receive boot acknowledge from the slave by setting "1" in EXT_CSD register, byte [179], bit 6 that the master can recognize that the slave is operating in boot mode.

The acknowledge pattern "010" must be sent to the master within 50ms by the slave after the CMD0 with the argument of 0xFFFFFFFA is received for the condition if boot acknowledge is enabled. If boot acknowledge is disabled, the acknowledge pattern "010" will not be sent out by the slave. When all contents of the enabled boot data are sent to the master, boot operation will be terminated.
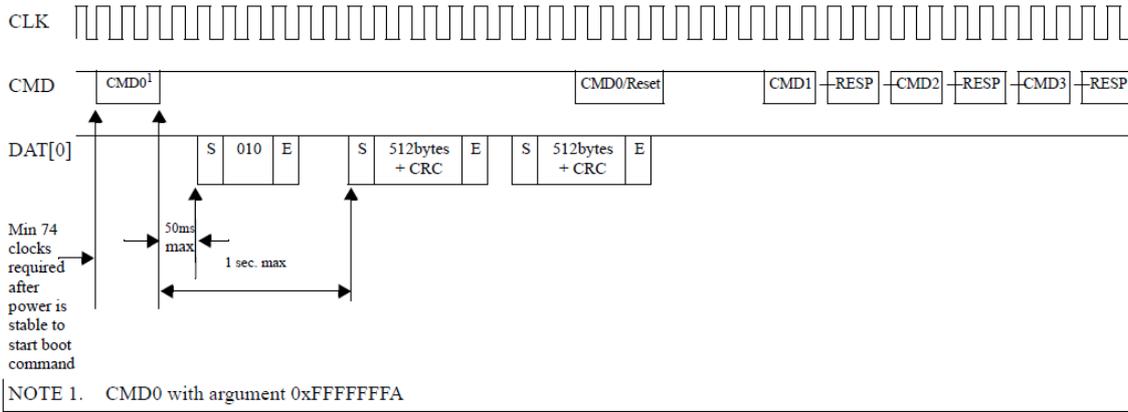
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Figure 9 Multimedia Card State & Timing Diagram (Alternative Boot Mode)

9.2 Partition

Memoright M1200 let the host split local memory into partitions with independent addressable space from logical address 0x00000000 for different use. Memory blocks are segmented as hereafter:

● Default factory setting defines two 1 MB boot partitions, as enhanced storage media. Host can set one segment in User Data Area as enhanced storage media (starting location and Write Protect Group size). This is one-time programmable and can NOT be changed once set. Up to 4 General Purpose Area can be set as user data or sensitive data or other usage. Partition size must be a multiple of the write protect group. This is one-time programmable and can NOT be changed once set.

There are four default area existed in the memory device including a User Data Area, two possible boot area partitions for booting and the Replay Protected Area Partition to verify and replay-protect data. Before any partitioning operation, the memory initially consists of the User Data Area and Boot Area Partitions. The embedded device offers the possibility of configuring by using host additional split local memory partition with independent addressable space. The addressable space starts from logical address 0x00000000 for different usage models. For two Boot Area Partitions, the size is multiple of 128KB and let the booting from e-MMC can be performed. Four General Purpose Area Partitions is used for sensitive data storage and the size is multiple of a Write Protect Group. Memory manufacturer defines Boot Partitions' size and attributes (read-only). For General Purpose Area Partitions' sizes and attributes, they can be programmed by the host only once in the device life cycle (one-time programmable). Moreover, one segment of the User Data Area can be configured to be implemented as enhanced storage media and to specify its starting location and size in terms of Write Protect Groups. The attributes of the Enhanced User Data Area can be programmed only once during device life cycle. The memory block area can be divided and example of partitions and user data area configuration are shown as following.
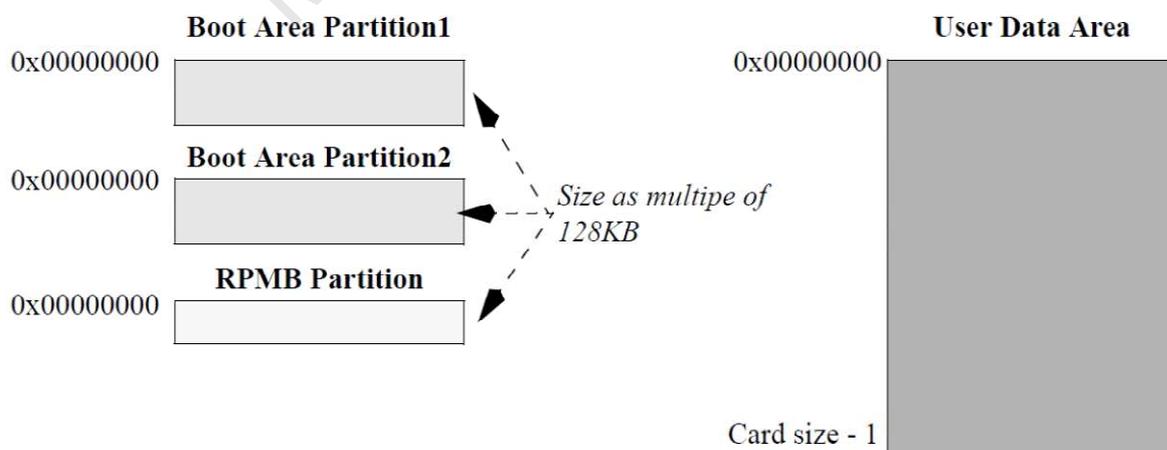

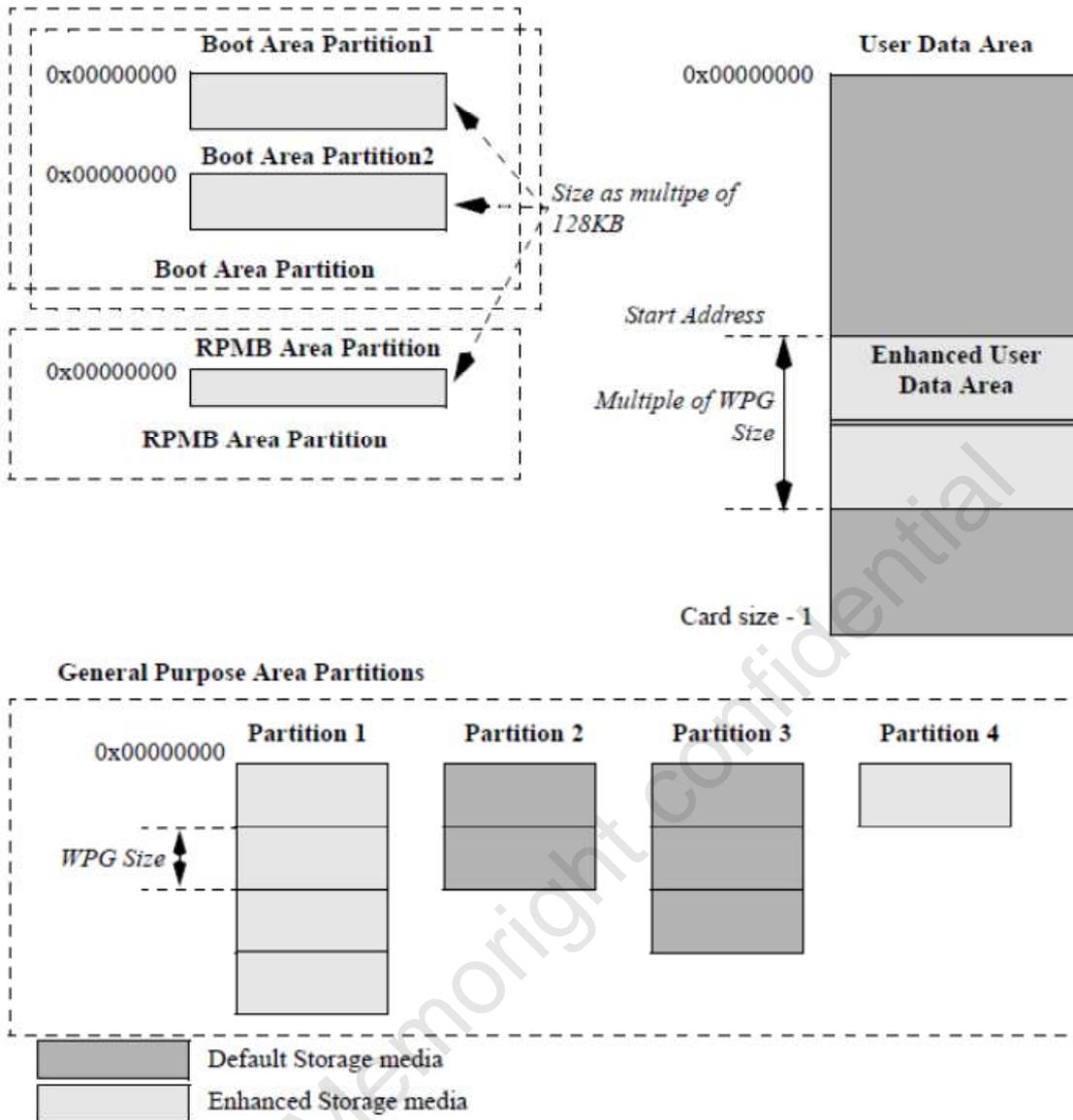
Figure 10 e-MMC Memory Organization

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Figure 11 Example of partitions and user data area configuration

9.3 Sleep Mode

Memoright M1200 automatically switches to sleep mode to save power if no further commands are received. Typical sleep transition last 200ns (highest duration before sleep is 850ms, for housekeeping operation). It does not involve any action from host, however, for maximum power saving (lowest current), host clock to the memory device needs to be shut down. For most embedded systems, beside while host is accessing data, devices are always in sleep mode, for greater power saving efficiency. Whenever host is going to access storage device in sleep mode, any issued command will cause device to exit sleep and operation execution.

9.4 Sleep (CMD5)

Memoright M1200 can switch between Sleep and Standby on SLEEP/AWAKE (CMD5) command. In Sleep state, device's power consumption is minimized and reacts only to RESET (CMD0) and SLEEP/AWAKE (CMD5) commands. Any other command will be completely ignored.

The Vcc power supply may even be switched off in Sleep mode to allow further power saving.

For additional information please refer JESD84-A441 section number 7.6.15

9.5 Enhanced Write

In Memoright M1200 reliable write (defined in eMMC 4.41 spec 4) mode, original data pointed by a logical address will stay the same until the new data has been successfully overwritten. This ensures that the each write transaction will always be reliable and never leaves undefined data in given address. When using enhanced write, data will remain valid even in the case of power drop during programming.

9.6 Secure Erase

Memoright M1200 supports Security Mode Erase command. Once triggered, no command is allowed until Secure Erase is completed.

Memoright M1200 will sanitize the erase area with predefined pattern. The purge will overwrite addressable content with a given character and then erase the NAND flash.

This command meets specific defense or governmental requirements and guarantees Flash memory content can no longer be restored.

9.7 Secure Trim

Memoright M1200 Secure Trim is similar to the Secure Erase but performs a purge on write blocks (512 bytes) .

9.8 Trim

Trim function acts like an Erase but operate at block (512 B) level. For additional information, refer to JEDEC JESD84-A441.

.

9.9 Write Protection

To prevent accidental data loss or overwrite, Memoright M1200 provides two levels of write protection:

• Write-protect the whole device (including the Boot Area Partitions, General Purpose Area Partition, and User/Enhanced User Data Area Partition) by setting the permanent or temporary write protect bits in the CSD.

• Write-protect specific segments permanently or temporarily write protected. Segment size can be defined in the EXT_CSD register. For additional information, refer to JEDEC JESD84-A441.

9.10 Hardware Reset

Host may reset the device to pre-idle state and disable temporary write protection on related blocks. For additional information, refer to JEDEC JESD84-A441.

9.11 Background Operations

In order to reduce latency for time critical operations, housekeeping operations (garbage collection, erase and compaction) are executed in the background.

Operations are classified into two types:

Foreground – such as read or write commands and

Background –executed when the device is not busy with host commands.

For additional information on Background Operations, refer to JESD84-A441 standard section 7.6.19

9.12 High Priority Interrupt (HPI)

If OS use on demand-paging to run user process, the host needs to fetch pages in the midst of other operation, so the query might be delayed until the completion of the command.

High priority interrupt (HPI) allows low read latency operation, by holding lower priority process before completion. This mechanism reduces latency, typically to less than 10 ms.

For additional information on the HPI function, refer to JESD84-A441 standard section 7.6.2

9.13 DDR Interface

Memoright M1200 support DDR signaling to double bus performance. For additional information please refer to JESD84-A441 standard.

10. Memoright e-MMC Marking Information

10.1 Top View

16mm

12mm

M1200
MREMK3B016GOBBAB00
3-YYWWD-S1-C
Taiwan

Industrial Drive

10.1.1 Label Content
- First Row: Memoright Logo
- Second Row: Product Name
- Third Row: Part Number
- Fourth Row: Internal Code-X-YYWWD-S1-C
  - ◆ X: MR Internal use only
  - ◆ YY: Last two digit of year
  - ◆ WW: Work week
  - ◆ D: A day within the week
  - ◆ S1-C: For internal use only

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11. eMMC Signals Connection and Layout Guideline

The paragraph provides you the connection and layout guideline for Memoright e-MMC embedded storage solutions. Please follow following layout guidelines to achieve highest reliability and performance for your e-MMC storage solutions

1. For signal integrity, it is recommended that all of e-MMC signals route on PCB component layer and reference to GND layer.
2. The following table capture from e-MMC spec shows the pull high resistor value for e-MMC interface. It is recommended to put 51KΩ for DAT signals, 10 KΩ for CMD signal and a 22 Ω serial resistor for CLK between host and e-MMC device.

Table 14 Recommended component value for layout

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7		100(1)	KΩ	To prevent bus floating
Pull-up resistance for DAT0-7	R_{DAT}	10		100(1)	KΩ	To prevent bus floating

3. The e-MMC support one or more combinations of Vcc and V_{CCQ} as shown below. The V_{CCQ} must be defined at equal to or less than Vcc.

Table 15 V_{CC} & V_{CCQ} combination supported by e-MMC

		V_{CCQ}		
		1.1V~1.3V	**1.65V~1.95V**	**2.7V~3.6V**
V_{CC}	**2.7V~3.6V**	Valid	Valid	Valid
	1.7V~1.95V	Valid	Valid	NOT VALID

4. It's recommended to put one 0.1uF and 1uF Capacitor for both Vcc and V_{CCQ}. For Vddi, it needs only one 0.1uF capacitor.

It needs to keep the PWR/GND trace as wide as short as possible. It's recommended to put the capacitors on bottom layer under the power ball.
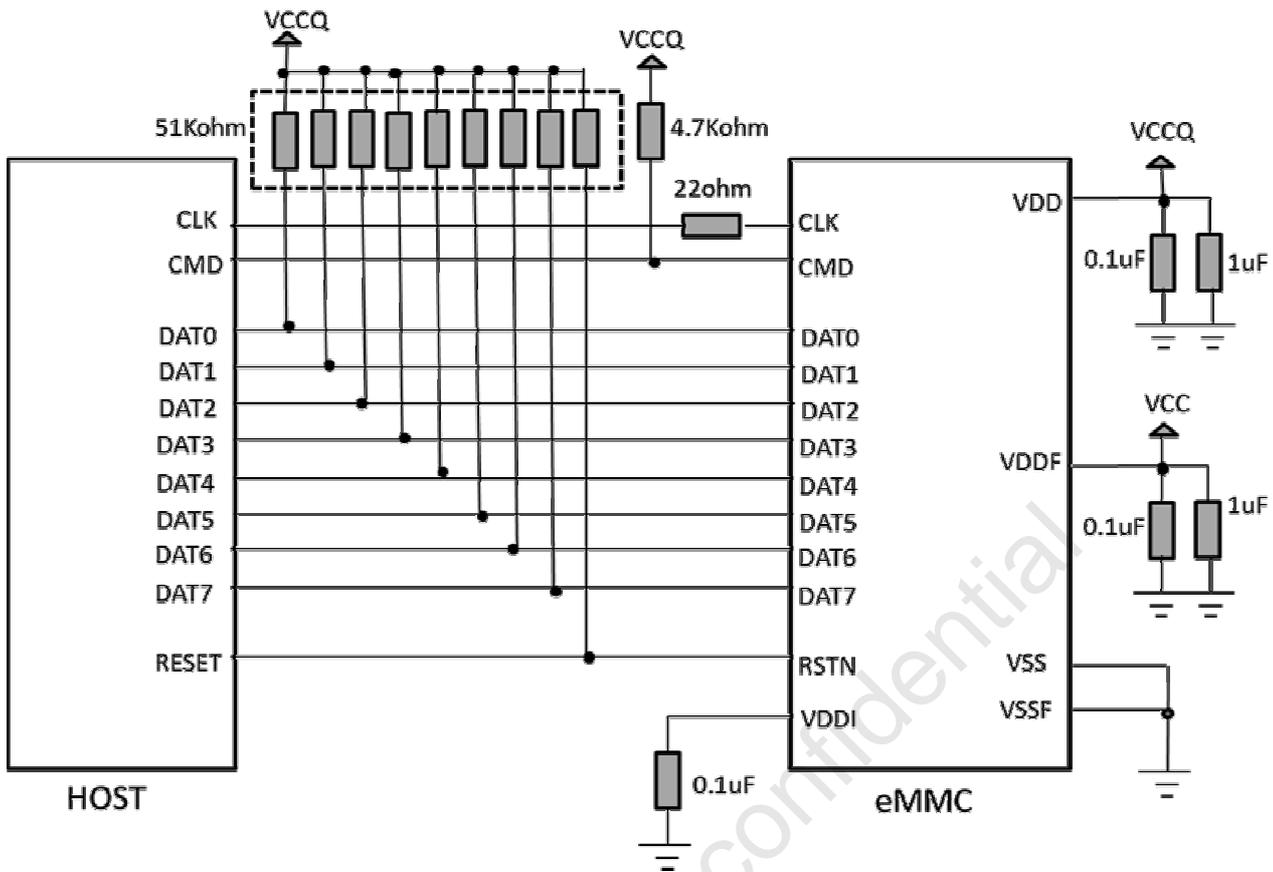
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Figure 12 Supported x8 connection guide

12. Contact Information

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