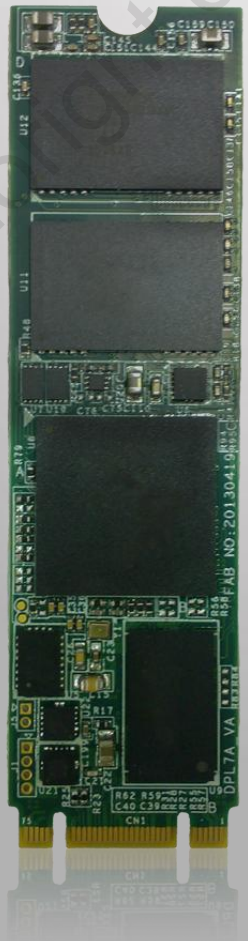
Memoright

Product Data Sheet

NF8-830

PCI-e Gen2x2

Commercial Temperature Grade



Revision: V06

Date: January 2015

Commercial Temp M.2 Solid State Drive – NF8-830 Series

128 GB~512 GB

1. Features

- Form Factor
  - M.2(NGFF) 22*80mm (Next Generation Form Factor) Solid State Drive (SSD)
- Available Capacities
  - 128 GB~512 GB (MLC NAND Flash)
- Highly integrated controller for NAND Flash memory
  - MLC NAND Flash
- High Performance
  - Up to 1000 MB/s burst transfer rate in PCIe Gen2x2, 10 Gb/s
  - Read Performance: up to 750 MB/s
  - Write Performance: up to 550 MB/s
- Low Power Consumption
  - Supply Voltage 3.3V±5%
- ECC
  - Built-in Strong BCH-ECC engine
- High Reliability
  - MTBF > 1,200,000 hours
  - Dynamic, static and active balanced wear-leveling strategy
  - Bad-Block Management
- Certificate
  - Fully Compliant with RoHS directive
  - CE and FCC compliant
- Temperature Ranges
  - Commercial Temperature Range: 0℃ ~+70℃

2. Contents

3. Ordering Information

The following Tables list the part No. for Memoright NF8-830 series SSDs.

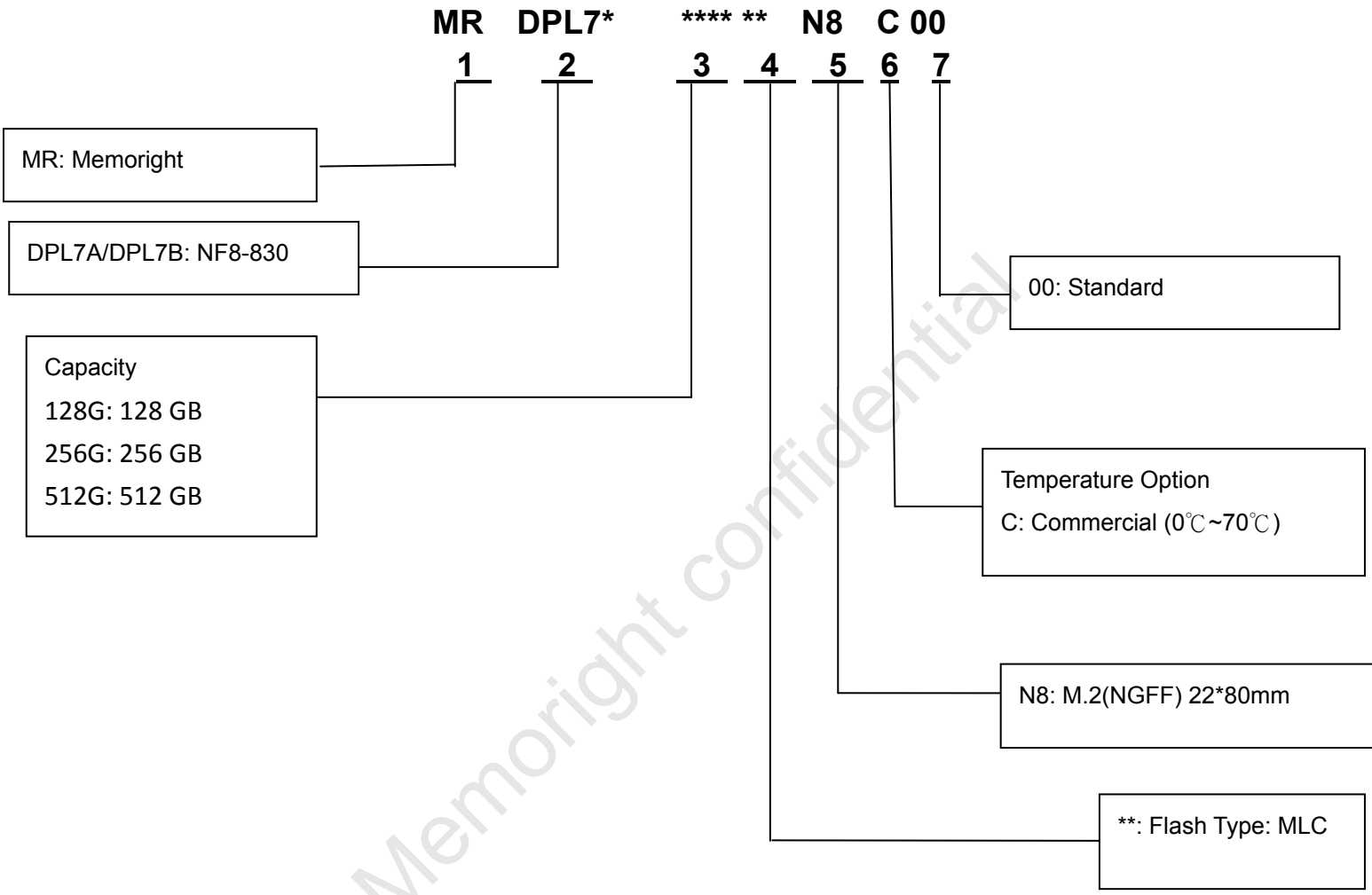
Table 1: Commercial temperature product list

Part Number	Capacity	Flash Type	Form Factor
MRDPL7A128GTSN8C00	128 GB*	MLC	M.2 22*80mm
MRDPL7B128GTRN8C00	128 GB*	MLC	M.2 22*80mm
MRDPL7B256GTSN8C00	256 GB*	MLC	M.2 22*80mm
MRDPL7B512GTUN8C00	512 GB*	MLC	M.2 22*80mm

* 1 GB=1,000,000,000 Bytes

For latest ordering information, please consult Memoright's sales representatives or check on our website: http://www.memoright.com

3.1 Part Number Decoder



4. General Description

The Memoright NF8-830 series SSD with state-of-the-art M.2(NGFF) form factor provides you ultimate performance and ultra-high reliability over traditional hard disk drive by achieving up to 750 MB/s/550 MB/s sequential read/write rate and integrated protection technologies such as bad block management and wear-leveling. The above-mentioned features made Memoright NF8-830 series SSD the best solution for various industrial applications.

For reliability, Memeoright NF8-830 series SSD integrates **dynamic, static and active (inactive) balanced wear leveling technology** to ensure an equal usage of the Flash memory cells to extend the SSD life time. Moreover, it provides features such as Enhanced **ECC algorithm**, **bad block management algorithm and MTBF>1,200,000** hours to assure overall reliability.

Memoright NF8-830 series SSD consists solely of semiconductor devices, which means it doesn't have any mechanical part such as platter (disk), motor and suspension as traditional hard disk drive. Its characteristics such as high performance, capacity, reliability, ruggedness, low power consumption and small form factor make it the best storage solution for industrial application with extreme environment and increased MTBF requirements.

4.1 Physical Description

The important component of Memoright NF8-830 SSD includes a Flash controller and NAND Flash memory modules. The controller works with a host system to allow data to be written to and read from the Flash memory modules through a (PCIe) interface. The SSD is offered in a NF8-830 form factor with a M.2 connector.

4.2 Endurance and Warranty Policy

Endurance	In normal operation, guarantees for 3 years product lifetime for half the SSD capacity sequential write per day based on JEDEC 218 standard test pattern*.
Warranty Policy	Please refer to Memoright official website http://www.memoright.com for latest warranty policy.

*Endurance is variable depends on different platform/OS and test pattern.

4.3 System Performance

Table 2: System Performance Table

System Performance		Max.	Unit
Data transfer Rate (PCIe Gen2x2 burst (10 Gb/s)		1000	MB/s
Sequential Read Rate	128 GB	750	MB/s
Sequential Write Rate	128 GB	300	MB/s
4KB Random Read IOPS	128 GB	80000	IOPS
4KB Random Write IOPS	128 GB	60000	IOPS
Sequential Read Rate	256 GB	750	MB/s
Sequential Write Rate	256 GB	550	MB/s
4KB Random Read IOPS	256 GB	95000	IOPS
4KB Random Write IOPS	256 GB	70000	IOPS
Sequential Read Rate	512 GB	750	MB/s
Sequential Write Rate	512 GB	550	MB/s
4KB Random Read IOPS	512 GB	95000	IOPS
4KB Random Write IOPS	512 GB	70000	IOPS

4.4 Environmental Specifications

4.4.1 Recommended Operating Conditions

Table 3: Recommended Operating Conditions

Parameter	Value
Commercial Operating Temperature	0℃ to 70℃
Power Supply Voltage Range	3.3V DC ± 5%

4.4.2 Power Consumption (*)

Table 4: Power Consumption

Current/Power Consumption	3.3V	Unit
Continue Read Power (Average)	＜4.38	W
Continue Write Power (Average)	＜9.20	W
Idle Mode Power (Average)	＜1.02	W

* All values are tested under room temperature 25℃ @ 3.3V. The power consumption may vary depends on different platform, OS, BIOS & test tools.

4.4.3 Recommended Storage Conditions

Table 5: Recommended Storage Conditions

Parameter	Value
Commercial Storage Temperature	-55℃ to 95℃
Maximum Temperature Gradient	25℃ per hour

4.4.4 Shock, Vibration and Humidity

Table 6: Shock, Vibration and Humidity

Parameter	Value
Humidity (non-condensing)	5%~95% (Operating)
Relative Humidity Gradient	30% per hour max
Vibration	10G(Peak,10~2000Hz)
Shock (Operating)	50G, (11ms duration, half sine wave)
Shock (Non-Operating)	1500G, (0.5ms duration, half sine wave)

4.5 Reliability

Table 7: Reliability

Parameter	Value
Mean Time Between Failures (MTBF)	＞ 1,200,000hours (Calculation mode: Telcordia SR-332 Issue 1 Method 1, Case 1)

4.6 Physical Dimensions

Table 8 Physical Dimension

Physical Dimensions		Unit
Length	80	mm
Width	22	mm
Thickness	3.2	mm

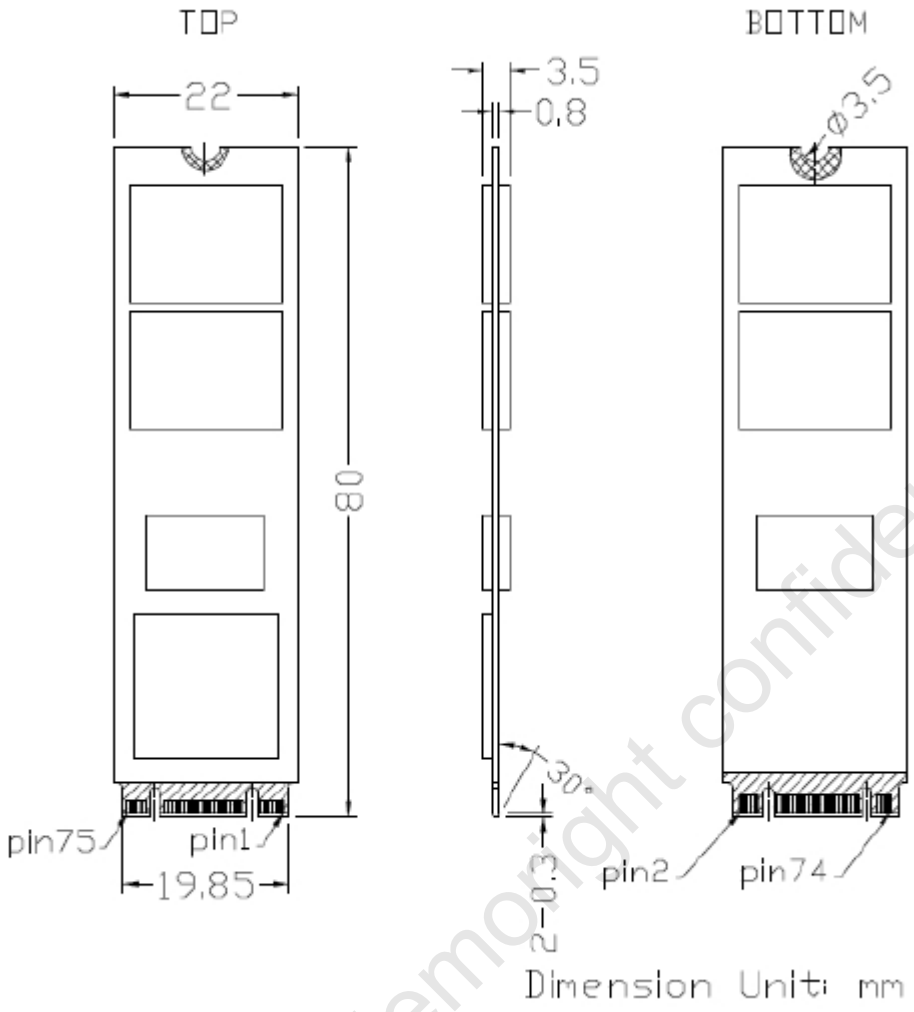
4.7 Drive Geometry

Unformatted Capacity	Guaranteed Sectors	Bytes per Sector
128 GB*	250,069,680	512
256 GB*	500,118,192	512
512 GB*	1,000,215,216	512

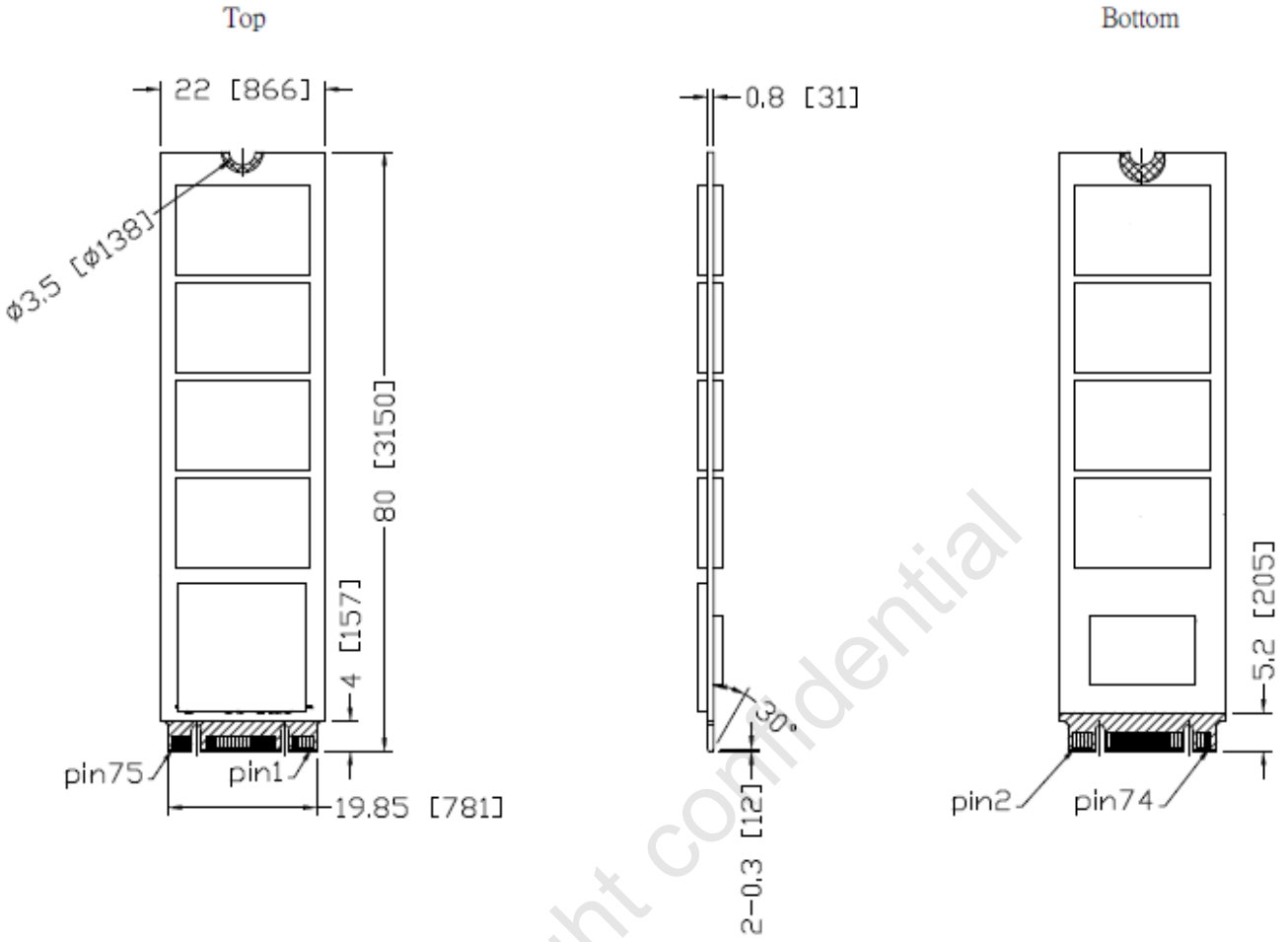
*1GB=1,000,000,000 Bytes

5. Physical Dimension Diagram

Table 9: Physical Dimension Diagram



Physical Dimensions		Unit
Length	80	mm
Width	22	mm
Thickness	3.5	mm



Physical Dimensions		Unit
Length	80	mm
Width	22	mm
Thickness	3.2	mm

6. Mean Time Between Failure (MTBF)

The MTBF prediction results for various NF8-830 configurations. The analysis was performed using a RAM Commander™ failure rate prediction.

- Failure Rate: The total number of failures within an item population, divided by the total number of life units expended by that population during a particular measurement interval under stated condition.

- Mean Time between Failures (MTBF): A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

Product	Condition	MTBF (Hours)
NF8-830	25°C	> 1,200,000

7. Pin Assignment

Table 10 Pin Assignment

74	3.3V	CONFIG_2=GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz)(I)(0/3.3V)	CONFIG_1=NC	69
	Module Key	NC	67
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
58	Reserved for MFG_CLOCK	GND	57
56	Reserved for MFG_DATA	REFCLKP	55
54	PEWAKE#(I/O)(0/3.3V)	REFCLKN	53
52	CLKREQ#(I/O)(0/3.3V)	GND	51
50	PERST#(I/O)(0/3.3V)	PERp0	49
48	N/C	PERn0	47
46	N/C	GND	45
44	N/C	PETp0	43
42	N/C	PETn0	41
40	N/C	GND	39
38	N/C	PERp1	37
36	N/C	PERn1	35
34	N/C	GND	33
32	N/C	PETp1	31
30	N/C	PETn1	29
28	N/C	GND	27
26	N/C	N/C	25
24	N/C	N/C	23
22	N/C	CONFIG_0=GND	21
20	N/C	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	N/C	11
10	LED1#	N/C	9
8	N/C	N/C	7
6	N/C	N/C	5
4	3.3V	GND	3
2	3.3V	CONFIG_3=GND	1

8. Supported ATA Commands

Table 11 Supported ATA Command

Command Name	Code (Hex)	Command Name	Code (Hex)
NOP	00h	WRITE MULTIPLE	C5h
DATA SET MANAGEMENT	06h	SET MULTIPLE MODE	C6h
READ SECTOR(S)	20h	READ DMA	C8h
READ SECTOR(S) EXT	24h	WRITE DMA	CAh
READ DMA EXT	25h	WRITE MULTIPLE FUA EXT	CEh
READ NATIVE MAX ADDRESS EXT	27h	STANDBY IMMEDIATE	E0h
READ MULTIPLE EXT	29h	IDLE IMMEDIATE	E1h
READ LOG EXT	2Fh	STANDBY	E2h
WRITE SECTOR(S)	30h	IDLE	E3h
WRITE SECTOR(s) EXT	34h	READ BUFFER	E4h
WRITE DMA EXT	35h	CHECK POWER MODE	E5h
SET MAX ADDRESS EXT	37h	SLEEP	E6h
WRITE MULTIPLE EXT	39h	FLUSH CACHE	E7h
WRITE DMA FUA EXT*	3Dh	WRITE BUFFER	E8h
WRITE LOG EXT	3Fh	READ BUFFER DMA	E9h
READ VERIFY SECTOR(S)	40h	FLUSH CACHE EXT	EAh
READ VERIFY SECTOR(S) EXT	42h	WRITE BUFFER DMA	EBh
WRITE UNCORRECTABLE EXT*	45h	IDENTIFY DEVICE	ECh
READ LOG DMA EXT*	47h	SET FEATURES	EFh
WRITE LOG DMA EXT*	57h	SECURITY SET PASSWORD	F1h
READ FPDMA QUEUED	60h	SECURITY UNLOCK	F2h
WRITE FPDMA QUEUED	61h	SECURITY ERASE PREPARE	F3h
EXECUTE DEVICE DIAGNOSTIC	90h	SECURITY ERASE UNIT	F4h
DOWNLOAD MICROCODE*	92h	SECURITY FREEZE LOCK	F5h
SMART	B0h	SECURITY DISABLE PASSWORD	F6h
Device Configuration Overlay	B1h	READ NATIVE MAX ADDRESS	F8h
Sanitize Device*	B4h	SET MAX ADDRESS	F9h
READ MULTIPLE	C4h		

*: Commands with * are not supported yet.

8.1 SECURITY FEATURE Set

The security mode features is used to prevent the SSD from unauthorized access by implementing a security password system to the host.

SECURITY Mode Default Setting

The SSD is shipped with the master password set to 20h value (ASCII blanks) and the lock function is disabled.

The new master password can bet set by system manufacturer or dealer by using the SECURITY SET PASSWORD command without enabling the lock function.

Initial Setting of the User Password

When a user password is set, the SSD enters lock mode automatically by the next power-on.

SECURITY Mode Operation from Power-On

In locked mode, the media access commands will be rejected until the SECURITY UNLOCK command is completed successfully.

Password Lost

User is not allowed to access any data if the user password is lost and high level security is set. However, the user can unlock the drive by using the master password.

It is impossible to access data if the user password is lost and maximum security level is set. However, user can unlock the drive by using the ERASE UNIT command with the master password and the drive will erase all user data and unlock the drive.

8.2 SMART FEATURE Set (B0h)

The SMART Feature Set command is used for providing access for Attribute Values, the Attribute Thresholds and other low level subcommands that can be used for logging and purpose reporting. Besides, it can also accommodate special needs for users. When the SMART Feature Set command is issued by the host, there are several subcommands of the SMART Feature Set that can be selected by the device's Features Register. In order to select a subcommand, the host must write the subcommand code to the device's Feature Register before issuing the SMART Feature Set command.

Sub Command

The host must write the subcommand code to the device's Feature Register before issuing the S.M.A.R.T Function Set command in order to select a subcommand. Please see following table for subcommands and respective subcommand codes.

Table 12 S.M.A.R.T Sub Command Set

Subcommand	Code
SMART READ DATA	D0h
SMART READ ATTRIBUTE THRESHOLDS	D1h
SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE	D2h
SMART SAVE ATTRIBUTE VALUES	D3h
SMART EXECUTE OFF-LINE IMMEDIATE	D4h
SMART READ LOG	D5h
SMART WRITE LOG	D6h
SMART ENABLE OPERATIONS	D8h
SMART DISABLE OPERATIONS	D9h
SMART RETURN STATUS	DAh
SMART ENABLE/DISABLE AUTOMATIC OFF-LINE	DBh

- **S.M.A.R.T. Read Data (subcommand D0h)**

This subcommand returns the device's Attribute Values to the host. After receiving the S.M.A.R.T. Read Attribute Values subcommand from the host, the device asserts BSY, and then saves any updated Attribute Values to the Attribute Data sectors. After that, the device asserts DRQ, clears BSY, asserts INTRO, and then the device will wait for the host to transfer the 512 bytes of Attribute Value information from the device via the Data Register.

- **S.M.A.R.T. Read Attribute Thresholds (subcommand D1h)**

  The subcommand returns the device's Attribute Threshold to the host. The device reads the Attribute Thresholds from the Attribute Threshold sectors and then waits for the host to transfer the 512 bytes of Attribute Thresholds information from the device after receiving the S.M.A.R.T. Read Attribute Thresholds subcommand from the host.

- **S.M.A.R.T. Enable/Disable Attribute Autosave (subcommand D2h)**
  The subcommand enables and disables the attribute auto save feature of the device. At the timing of the first transition to Active idle mode and after 15 minutes after the last saving of Attribute Values, the S.M.A.R.T. Enable/Disable Attribute Autosave subcommand allows the device to automatically save its updated Attribute Values to the Attribute Data Sector. This subcommand will disable the auto-save feature. No matter the state of the Attribute Autosave feature is enabled or disabled, it will be preserved by the device across the power cycle.
  By writing a value of 00h from the host into the device's Sector Count Register before issuing the S.M.A.R.T. Enable/Disable Attribute Autosave subcommand will cause this feature to be disabled. During some other normal operation such as a power-up or a power-down, it will not prevent the device from saving Attribute Values to the Attribute Data sectors by disabling this feature.
  By writing a value of F1h from the host into the device's Sector Count Register before issuing the S.M.A.R.T. Enable/Disable Attribute Autosave subcommand will cause this feature to be enabled. Before issuing the S.M.A.R.T. Enable/Disable Attribute Autosave subcommand, any other nonzero value written from the host into this register will not change the current Autosave status. The device will respond with the S.M.A.R.T error code.
  The S.M.A.R.T. Disable Operations subcommand disables the auto save feature along with the device's S.M.A.R.T. operations. The device asserts BSY and then enables or disables the Autosave feature, clears BSY, and then asserts INTRQ after receiving the subcommand from the host.

- **S.M.A.R.T Save Attribute Values (subcommand D3h)**
  By using this subcommand, the device saves any updated Attribute Values to the device's Attribute Data Sector regardless of the Attribute Autosave feature status. The device asserts BSY, writes any updated Attribute Values to the Attribute Data Sector and then clears BSY and finally asserts INTRQ after receiving the S.M.A.R.T. Save Attribute Values subcommand from the host.

- **S.M.A.R.T. Execute Off-line Immediate (subcommand D4h)**
  By using this subcommand, the device immediately initiates the set of activities that collect Attribute data in an offline mode (off-line routine) or execute a self-test routine in either captive or off-line mode. The operation to be executed must be specified by setting the LBA Low register.

Table 13 Execute S.M.A.R.T Sub Command Set

LBA Low	Subcommand
00h	Execute S.M.A.R.T off-line data collection routine immediately
01h	Execute S.M.A.R.T. Short self-test routine immediately in off-line mode
02h	Execute S.M.A.R.T Extended self-test routine immediately in off-line mode
03h	Reserved
04h	Execute S.M.A.R.T. Selective self-test routine immediately in off-line mode
40h	Reserved
7Fh	Abort off-line mode self-test routine
81h	Execute S.M.A.R.T. short self-test routine immediately in captive mode
82h	Execute S.M.A.R.T Extended self-test routine immediately in captive mode
84h	Execute S.M.A.R.T. selective self-test routine immediately in captive mode
C0h	Reserved

Off-line mode: The device executes command completion before executing the specified routine. During execution of the routine, the device will not set BSY nor clear DRDY. If the device is interrupted by a new command from the host when performing its routine, the device will abort or suspend its routine and serve the host within 2 seconds after receiving the new command. The routine will be resumed or not started automatically after the interrupting command is served depending on the interrupting command.

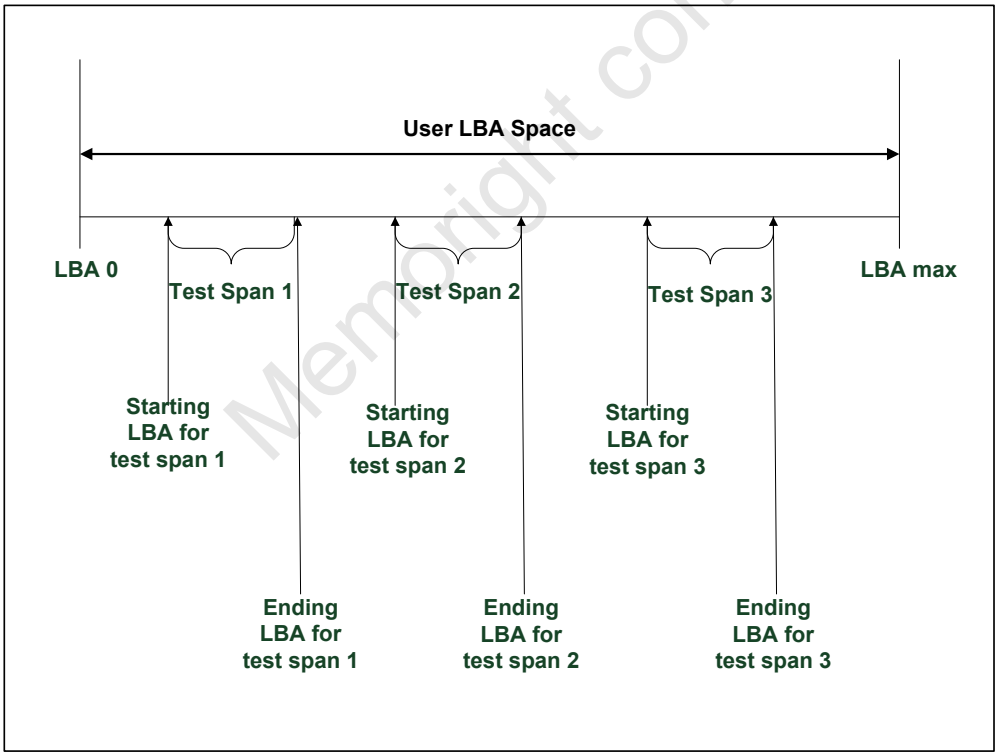
Captive mode: When executing self-test in captive mode, after receiving the command, the device sets BSY to one and executes the specified self-test routine. At the end of the routine, the device sets the execution result in the Self-test execution status byte and ATA registers and then executes the command completion. Please see following definition.

Status	Set ERR to one when the self-test has failed
Error	Set ABRT to one when the self-test has failed
LBA Low	Set to F4h when the self-test has failed
LBA High	Set to 2Ch when the self-test has failed

8.3 S.M.A.R.T. Selective Self-test Routine

The selective self-test routine shall be performed when the value in the LBA Low register is 4 or 132. The initial tests performed by the extended self-test routine plus a selectable read scan shall be included in the self-test routine. When the execution of a Selective self-test command is in progress, the Selective self-test log shall not be written by the host. The read scan can be done by user only on specific areas of the media. To do this, user shall set the test spans desired in the Selective self-test log and set the flags in the Feature flags field of the Selective self-test log to indicate do not perform off-line scan. In this case, the test spans defined shall be read scanned in their entirety. The Selective self-test log is updated as the self-test proceeds indicating test progress. The test is terminated when all specified test spans have been completed and the appropriate self-test execution status is reported in the SMART READ DATA response depending on the occurrence of errors. Please see following figures for an example of a Selective self-test definition with three defined test spans. In this eample, the test will be terminated when all three test spans have been scanned.

Table 14 S.M.A.R.T Self Test Example



The scan of the selected spans is shown as above figure. For a user that wishes to have the rest of media read scanned as an off-line scan, the flag must be set to enable off-line scan in addition to other settings. If there is an error during the scanning of the test spans, the self-test execution status in the SMART READ DATA response will report that error and the off-line scan will not be

executed.

When the test spans defined have been scanned, the device will set the offline scan pending, and then the active flags in the Selective self-test log will be set to one, the span under test will be set to a value greater than five, the self-test execution status in the SMART READ DATA response to 00h, set a value of 03h in the off-line data collection status in the SMART READ DATA response and shall proceed to do an off-line read scan through all areas not included in the test spans. This off-line read scan must be completed as rapidly as possible, with no pauses between block reads. Besides, any encountered errors shall not be reported to the host. However, the error locations must be logged for future reallocation. The off-line scan must be resumed when the device is power-up again once the device is power-down before the off-line scan is completed. The scan resumption time must be delayed for the time indicated in the Selective self-test pending time field in the Selective self-test log. During this delay time, the pending flag shall be set to one and active flag shall be set to zero in the Selective self-test log. The active flag must be set to one and the off-line scan must be resumed once the time expires. The off-line scan must be terminated when the entire media has been scanned and both the pending and active flags shall be cleared to zero. For indicating completion, the off-line data collection status in the SMART READ DATA response must be set to 02h.

The self-test executions time byte in the Device SMART Data Structure may be updated. However, the accuracy may be not exact due to the nature of the test span segments. Due to this reason, the time to complete off-line testing and the self-test polling times are not valid. Progress through the test span is indicated in the selective self-test log.

The Selective self-test shall be aborted except when the pending bit is set to one in the Selective self-test log. By receiving a SMART EXECUTE OFF-LINE IMMEDIATE command with 0Fh, Abort off-line test routine in the LBA Low register shall abort Selective self-test regardless of where the device is in the execution of the command. If a selective self-test is in progress and a second self-test is issued, the selective self-test is aborted and the newly requested self-test is executed.

S.M.A.R.T Read Log Sector (subcommand D5h)

The command is used to return the indicated log sector contents to the host and the sector count determines the sector numbers to be read from the specified log. The log transferred by the drive shall start at the first sector in the specified log regardless of the sector count requested. For sector number, it indicates the log sector to be returned. Please see following table for detail.

Table 15 Log Sector

Log Sector Address	Content
00h	Log Directory
01h	SMART Error Log
02h	Comprehensive SMART Error Log
04h-05h	Reserved
06h	SMART self-test log
08h	Reserved
09h	Selective self-test log
0Ah-7Fh	Reserved
80h-9Fh	Host Vendor Specific
A0h-FFh	Reserved

RO	Log is read only by the host
R/W	Log is read or written by the host
VS	Log is vendor specific thus read/write ability is vendor specific

- **S.M.A.R.T. Write Log Sector (subcommand D6h)**
  This command writes 512 bytes of data to the specified log sector. The 512 bytes of data must be transferred at a command and the LBA Low value shall be set to one. The LBA Low shall be set to specify the log sector address. The device will return ABRT error if a Read only log sector is specified.

- S.M.A.R.T. Enable Operations (subcommand D8h)
  This subcommand is used for all S.M.A.R.T. capabilities access in the device. Before receiving a S.M.A.R.T. Enable Operation subcommand, Attribute Values are not monitored or saved by the device. The S.M.A.R.T state will be preserved by the device across power cycle no matter the S.M.A.R.T. is enabled or disabled. Once the S.M.A.R.T is enabled, the Attribute Values won't be affected by subsequent S.M.A.R.T Enable Operations subcommand receiving. After the S.M.A.R.T. Enable Operations subcommand from the host, the device asserts BSY, enables S.M.A.R.T capabilities and functions, clears BSY and asserts INTRQ.

- **S.M.A.R.T. Disable Operations (subcommand D9h)**
  This subcommand is used to disable all S.M.A.R.T capabilities within the device including its attribute autosave feature. The device disables all S.M.A.R.T. operations after receiving this subcommand. Non self-preserved Attribute Values will no longer be monitored. The state of S.M.A.R.T. will be preserved by the device across power cycle no matter it is

enabled or disabled. Please note that this subcommand does not preclude the device's power mode attribute auto saving. After receiving the S.M.A.R.T Disable Operation subcommand from the host, the device asserts BSY, disables S.M.A.R.T. capabilities and functions, clears BSY and asserts INTRQ.

After the S.M.A.R.T Disable Operations subcommand is received from the host to the device, all other S.M.A.R.T. subcommands except S.M.A.R.T Enable Operation will be disabled, invalid and will be aborted by the device including the S.M.A.R.T. Disable Operations subcommand returning the S.M.A.R.T. error code.

Any Attribute Values accumulated and saved to volatile memory prior to the receiving of the S.M.A.R.T Disable Operations command will be preserved in the device's Attribute Data Sectors. If the device is re-enabled, these Attribute Values will be updated as needed after the receiving of S.M.A.R.T Read Attribute Values or S.M.A.R.T. Save Attribute Values command.

- **S.M.A.R.T Return Status (subcommand DAh)**

  This command is used to device reliability status to the host's request. After receiving the S.M.A.R.T. Return Status subcommand, the device asserts BSY, saves any updated Attribute Values to the reserved sector and compares the updated Attribute Values to the Attribute Thresholds.

  The device loads 4Fh into the LBA Mid register, C2h into the LBA High register, clears BSY and asserts INTRQ if the device does not detect a Threshold Exceed Condition or detects a Threshold Exceed Condition but involving attributes are advisory.

  The device loads F4h into the LBA Mid register, 2Ch into the LBA High register, clears BSY, and asserts INTRQ if the device detects a Threshold Exceed Condition for pre-failure attributes. Advisory attributes never result in a negative reliability condition.

- **S.M.A.R.T. Enable/Disable Automatic Off-line (subcommand DBh)**

  The subcommand enables and disables the optional feature that cause the device to perform the set of off-line data collection activities that automatically collect attribute data in an off-line mode and then save this data to the device's nonvolatile memory. This subcommand may either cause the device to automatically initiate or resume performance of its off-line data collection activities or cause the automatic off-line data collection feature to be disabled. This subcommand also enables and disables the off-line read scanning feature that causes the device to perform the entire read scanning with defect reallocation as the part of the off-line data collection activities.

Please set the Sector Count register to specify the feature to be enabled or disabled.

Sector Count	Feature Description
00h	Disable Automatic Off-line
F8h	Enable Automatic Off-line

The off-line data collection feature will be disabled if a value of zero is written by the host into the device's Sector Count register before issuing this subcommand. Disabling this feature does not preclude the device from saving attribute values to nonvolatile memory during some other normal operation such as during a power-on, a power-off, or an error recovery sequence.
The automatic Off-line data collection feature will be enabled if a value of F8h is written by the host into the device's Sector Count register before issuing this subcommand.
Any other non-zero value written by the host into the register before issuing this subcommand is vendor specific and will not change the current Automatic Off-Line Data Collection and Off-line Read Scanning status. However, the device may respond with the S.M.A.R.T. error codes.

8.4 Device Attribute Data Structure

Following table defines the 512 bytes that make up the Attribute Value information. The data structure is accessed by the host in its entirety by using the S.M.A.R.T. Read Attribute Values subcommand.

Table 16 Device Attribute Data Structure

Byte	Description
0~1	Data structure revision number
2~361	1st-30th Individual attribute data
362	Off-line data status
363	Self-test execution status
364~365	Total time in seconds to complete off-line data collection activity
366	Vendor Specific
367	Off-line data collection capability
368~369	SMART capability
370	Error logging capability 7-1 Reserved 0 1=Device error logging supported
371	Self-test failure check point
372	Short self-test routine recommended polling time (in minutes)
373	Extended self-test routine recommended polling time (in minutes)
374-510	Reserved
511	Data structure checksum

Data Structure Revision Number

The Data Structure Revision Number identifies which version of this data structure is implemented by the device. This revision number will be set to 0005h. This revision number identifies both the Attribute Value and Attribute Threshold Data Structure.

Individual Attribute Data Structure

The following defines the 12 bytes that make up the information for each Attribute entry in the Device Attribute Data Structure.

Table 17 Attribute Data Structure

Byte	Descriptions
0	Attribute ID number 01-FFh
1-2	Status flag Bit 0 (pre-failure/advisory bit) Bit 0=0 If attribute value is less than the threshold, the drive is in advisory condition. Product life period may expire. Bit0=1: If attribute value is less than the threshold, the drive is in pre-failure condition. The drive may have failure Bit 1 (on-line data collection bit) Bit 1=0: Attribute value will be changed during off-line data collection operation Bit 1=1: Attribute value will be changed during normal operation Bit 2(Performance Attribute Bit) Bit 3 (Error rate Attribute bit) Bit4 (Event Count Attribute Bit) Bit 5 (Self-Preserving Attribute Bit) Bit 6-15 Reserved
3	Attribute value 01h-FDh*1 00h,FEh,FFh= Not in use 01h=Minimum value 64h=Initial value Fdh=Maximum value
4	Worst Ever normalized Attribute Value (valid values from 01h-FEh)
5~10	Raw Attribute Value Attribute specific raw data (FFFFFFh-reserved as saturated value)
11	Reserved (00h)
*1 For ID= 199 CRC Error Count	

Attribute ID Numbers: Any nonzero value in the Attribute ID Number indicates an active attribute. The device supports following Attribute ID Numbers.

ID	Attribute Name
09h	Power-on Hours
0Ch	Power Cycle CountB1h
B1h	Wear Leveling Count
B2h	Used Reserved Block Count (Chip)
B3h	Used Reserved Block Count (Total)
B4h	Unused Reserved Block Count (Total)
B7h	Runtime Bad Count (Total)

Off-Line Data Collection Status

The current status of the off-line activities is defined by the value of this byte. Bit 7 indicates an Automatic Off-line Data Collection Status.

Bit 7	Automatic Off-line Data Status
0	Automatic Off-line Data Collection is disabled.
1	Automatic Off-line Data Collection is enabled.

Bit 0-6 represents a hexadecimal status value reported by the device.

Value	Definition
0	Off-line data collection never started.
2	All segments completed without errors. In this case the current segment pointer is equal to the total segments required.
3	Off-line activity in progress
4	Off-line data collection is suspended by the interrupting command
5	Off-line data collecting is aborted by the interrupting command
6	Off-line data collection is aborted with a fatal error.

Self-Test Execution Status

Bit	Definition
0-3	Percent self-test remaining. An approximation of the self-test routine remaining until completion given in ten percent increments. Valid Values are 0 through 9
4-7	Current Self-test execution status
0	The self-test routine completed without error or has never been run
1	The self-test routine was aborted by the host
2	The self-test routine was interrupted by the host with a hard or soft reset
3	The device was unable to complete the self-test routine due to a fatal error or unknown test error.
4	The self-test routine was completed with an unknown element failure
5	The self-test routine was completed with an electrical element failure
6	The self-test routine was completed with a servo element failure
7	The self-test routine was completed with a read element failure
15	The self-test routine is in progress

Total time in seconds to complete off-line data collection activity

This field tells the host how many seconds the device requires to complete the off-line data collection activity.

Current Segment Pointer

This byte is a counter indicating the next segment to execute as an off-line data collection activity. Because the number of segments is 1,01h is always returned in this field.

- Off-line Data Collection Capability

Bit	Definition
0	Execute Off-line Immediate implemented bit
	0: S.M.A.R.T Execute Off-line Immediate subcommand is not implemented
	1: S.M.A.R.T. Execute Off-line Immediate subcommand is implemented
1	Enable/Disable Automatic Off-line implemented bit
	0: S.M.A.R.T Enable/disable Automatic Off-line subcommand is not implemented
	1: S.M.A.R.T Enable/disable Automatic Off-line subcommand is implemented
2	Abort/restart off-line by host bit
	0: The device will suspend off-line data collection activity after an interrupting command and resume it after a vendor specific event
	1: The device will abort off-line data collection activity after receiving a new command Bit Definition
3	Off-line Read Scanning implemented bit
	0: The device does not support Off-line Read Scanning
	1: The device supports Off-line Read Scanning
4	Self-test implemented bit
	0: Self-test routing is not implemented
	1: Self-test routine is implemented
5	Reserved (0)
6	Selective self-test routine is not implemented
	0: Selective self-test routine is not implemented
	1: Selective self-test routine is implemented
7	Reserved (0)

8.4.1 S.M.A.R.T Capability

The word of bit flag describes the S.M.A.R.T. capabilities of the device. The device will return 03h indicating that the device will save its Attribute Values prior to going into a power saving mode and supports the S.M.A.R.T ENABLE/DISABLE ATTRIBUTE AUTOSAVE command.

Bit	Definition
0	Pre-power mode attribute saving capability. If bit=1, the device will save its Attribute Values prior to going into a power saving mode (Standby or Sleep mode)
1	Attribute auto save capability. If bit=1, the device supports the S.M.A.R.T. ENABLE/DISABLE ATTRIBUTE AUTOSAVE command
2-15	Reserved (0)

8.4.2 Error Logging Capability

Bit	Definition
7-1	Reserved (0)
0	The Error Logging support bit. If bit=1, the device supports the Error Logging.

8.4.3 Self-test failure check point

This byte shows the self-test section where the device detects a failure

8.4.4 Self-test Completion Time

These bytes are the minimum time in minutes to complete the self-test

8.4.5 Data Structure Checksum

The Data Structure Checksum is the 2's compliment of the result of a simple 8-bit addition of the first 511 bytes in the data structure.

8.5 Device Attribute Thresholds Data Structure

Please see following table for the 512 bytes that make up the Attribute Threshold information. This data structure is accessed by the host in its entirety using the S.M.A.R.T. Read Attribute Thresholds. All multi-byte fields in those data structures comply with the ATA/ATAPI-6 specification for byte ordering. So, the least significant byte occupies the lowest numbered byte address location in the field.

The active Attribute Thresholds sequence will appear in the same order as their corresponding Attribute Values.

Table 18 Attribute Thresholds Data Structure

Byte	Descriptions
0-1	Data structure revision number
2-361	1^{st}-30^{th} Individual attribute data
362-379	Reserved
380-510	Vendor Specific
511	Data structure checksum

8.5.1 Data Structure Revision Number

This value is the same as the value used in the Device Attributes Value Data Structure.

8.5.2 Individual Thresholds Data Structure

The 12 bytes that make up the information for each Threshold entry in the Device Attribute Thresholds Data Structure is defined in following table. Attribute entries in the Individual Threshold Data Structure are in the same order and correspond to the entries in the Individual Attribute Data Structure.

Table 19 Threshold Data Structure

Byte	Descriptions
0	Attribute ID Number (01h to FFh)
1	Attribute Threshold (for comparison with Attribute Values from 00h to FFh) 00h- “always passing” threshold value to be used for code test purposes 01h- minimum value for normal operation FDh-maximum value for normal operation FEh-invalid for threshold value FFh-“always failing” threshold value to be used for code test purposes
2-11	Reserved (00h)

8.5.3 Attribute ID Numbers

Attribute ID Numbers supported by the device are the same as Attribute Values Data Structures.

8.5.4 Attribute Threshold

These values are predetermined at the factory and can not be changed. However, the “S.M.A.R.T. Write Attribute Threshold” subcommand can be used by the host to override the preset values in the Threshold sectors.

8.5.5 Data Structure Checksum

The Data Structure Checksum is the 2’s compliment of the result of a simple 8-bit addition of the first 511 bytes in the data structure.

8.6 S.M.A.R.T. Log Directory

The 512 bytes that make up the S.M.A.R.T. Log Directory are defined as following table.

Table 20 S.M.A.R.T Log Directory

Byte	Descriptions
0-1	S.M.A.R.T Logging Version
2	Number of sectors in the log at log address 1
3	Reserved
4	Number of sectors in the log at log address 2
5	Reserved

510	Number of sectors in the log at log address 255
511	Reserved

The S.M.A.R.T. Logging Version word value shall be 01h. The logs at log addresses 80-9Fh are defined as 16 sectors long.

S.M.A.R.T. Error Log Sector

The 512 bytes that make up the S.M.A.R.T. error log sector is defined as following table. All multi-byte fields in these data structures comply with the ATA/ATAPI-6 specifications for byte ordering.

Table 21 S.M.A.R.T Error Log Sector

Byte	Descriptions
0	S.M.A.R.T error log version
1	Error log pointer
2-91	1st error log data structure
92-181	2nd error log data structure
182-271	3rd error log data structure
272-361	4th error log data structure
362-451	5th error log data structure
452-453	Device error count
454-510	Reserved
511	Data structure checksum

8.6.1 S.M.A.R.T. Error Log Version

This value is set to 01h

8.6.2 S.M.A.R.T. Error Log Pointer

This error log pointer points to the most recent error log data structure. Only values 1 through 5 are valid.

8.6.3 Device Error Count

The field contains the total number of errors. The value will not roll over.

8.6.4 Error Log Data Structure

The data format of each error log structure is shown in the table as following.

Table 22 Error Data Structure

Byte	Descriptions
n~n+11	1st command data structure
n+12~n+23	2nd command data structure
n+24~n+35	3rd command data structure
n+36~n+47	4th command data structure
n+48~n+59	5th command data structure
n+60~n+89	Error data structure

8.6.5 Command Data Structure

Data format of each command data structure is shown below

Table 23 Command Data Structure

Bytes	Descriptions
n	Content of the Device Control register when the Command register was written
n+1	Content of the Features Control register when the Command register was written
n+2	Content of the Sector Count Control register when the Command register was written
n+3	Content of the LBA Low register when the Command register was written
n+4	Content of the LBA Mild register when the Command register was written
n+5	Content of the LBA High register when the Command register was written
n+6	Content of the Device/Head register when the Command register was written
n+7	Content written to the Command register
n+8	Timestamp
n+9	Timestamp
n+10	Timestamp
n+11	Timestamp

Timestamp shall be the time since power-on in milliseconds when command acceptance occurred. This timestamp may wrap around.

8.6.6 Error Data Structure

Table 24 Error Data Structure

Bytes	Descriptions
n	Reserved
n+1	Content written to the Error register after command completion occurred
n+2	Content written to the Sector Count register after command completion occurred.
n+3	Content written to the LBA Low register after command completion occurred.
n+4	Content written to the LBA Mild register after command completion occurred.
n+5	Content written to the LBA High register after command completion occurred.
n+6	Content written to the Device/Head register after command completion occurred.
n+7	Content written to the Status register after command completion occurred.
n+8- n+26	Extended error information
n+27	State
n+28	Life Timestamp (least significant byte)
n+29	Life Timestamp (most significant byte)

Extended error information will be vendor specific.

State field contains a value indicating the device state when command was issued to the device.

Value	State
X0h	Unknown
X1h	Sleep
X2h	Standby
X3h	Active/Idle with BSY cleared to zero
X4h	Executing SMART off-line or self-test
X5h-xAh	Reserved
xBh-xFh	Vendor unique

The value of x is vendor specific and it is possible to be different for each state.

8.7 Self-test Log Structure

Table 25 Self-test Log Structure

Byte	Description
0~1	Data structure revision
n*24+2	Self-test number
n*24+3	Self-test execution status
n*24+4~ n*24+5	Life timestamp
n*24+6	Self-test failure check point
n*24+7~ n*24+10	LBA of first failure
n*24+11~ n*24+25	Vendor specific
---	---
506-507	Vendor specific
508	Self-test log pointer
509~510	Reserved
511	Data structure checksum

Note: N is 0 through 20

The data structure contains the descriptor of the Self-test that the device has performed. Each descriptor is 24 bytes long and the self-test data structure is capable to contain up to 21 descriptors. After 21 descriptors are recorded, the oldest descriptor will be overwritten with the new descriptor. The self-test log pointer points to the most recent descriptor. When there is no descriptor, the value is 0. When there are descriptor(s), the value is 1 through 21.

8.7.1 Selective Self-test Log Data Structure

The selective self-test log is a log that may be read and written by the host. The log allows the host to select the parameters for self-test and to monitor the progress of the self-test. The Selective self-test log which is 512 bytes is shown in following table. All multi-byte fields shown in these data structures follow the specification for byte ordering.

Table 26 Self-test Log Data Structure

Byte	Description	Read/Write
0-1	Data Structure Revision	R/W
2-9	Starting LBA for test span 1	R/W
10-17	Ending LBA for test span 1	R/W
18-25	Starting LBA for test span 2	R/W
26-33	Ending LBA for test span 2	R/W
34-41	Starting LBA for test span 3	R/W
42-49	Ending LBA for test span 3	R/W
50-57	Starting LBA for test span 4	R/W
58-65	Ending LBA for test span 4+	R/W
66-73	Starting LBA for test span 5	R/W
74-81	Ending LBA for test span 5	R/W
82-337	Reserved	Reserved
338-491	Vendor Specific	Vendor specific
492-499	Current LBA under test	Read
500-501	Current Span under test	Read
502-503	Feature flags	R/W
504-507	Vendor Specific	Vendor Specific
508-509	Selective self-test pending time	R/W
510	Reserved	Reserved
511	Data structure checksum	R/W

8.8 Error Reporting

The values returned in the Status and Error Registers when specific error conditions are encountered by a device are shown in following table

Table 27 S.M.A.R.T. Error Codes

Error Correction	Status Register	Error Register
A S.M.A.R.T. Function Set Command was received by the device without the required key being loaded into the LBA High and LBA Mid registers.	51h	04h
A S.M.A.R.T. Function Set Command was received by the device with a subcommand value in the Features Register that is either invalid or not supported by this device. .	51h	04h
A S.M.A.R.T FUNCTION SET command subcommand other than S.M.A.R.T. ENABLE OPERATIONS was received by the device while the device was in a “S.M.A.R.T. Disabled” state	51h	04h
The device is unable to read its Attribute Values or Attribute Thresholds data structure	51h	10h or 04h
The device is unable to write to its Attribute Values data structure	51h	10h or 40h

9. Regulatory and Certification Compliance for Product

Category	Certifications
EMC and EMI	CE (EU)
	BSMI (Taiwan)
	C-Tick (Australia)
	FCC (USA)

10. Feature Descriptions

10.1 Wear Leveling

For extending SSD's life time, a sophisticated wear leveling technology is important. Memoright NF8-830 series provides dynamic, static (initiative) balanced wear leveling strategy. The dynamic wear leveling algorithm ensures that erase/write cycles can be evenly distributed across all flash memory block locations to prevent excessive writes to the same physical flash memory location.

10.2 Bad Block Management

Memorigt NF8-830 series M.2 form factor SSD provides bad block management function with a certain number of reserved blocks. When a user data block fails, a reserved block will replace the failed block. The replacement of bad block is transparent to user.

10.3 ECC

The SSD provides Built-in Strong BCH-ECC engine

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10.4 Standards Compliance

Memoright NF8-830 SSD complies with following standards.

FCC

CE

RoHS

11. Contact Information

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