Memoright

Product Data Sheet

M1600

BGA 153 Balls
up to 400 MB/sec Bus Transfer Rate
Business Temperature Grade

Revision: V02
Date: January 2014

e-MMC 5.0 Embedded Flash Memory – M1600 Series

4GB ~ 32GB

1. Features

- **General Features**
  - **Embedded with e-MMC Flash Controller and NAND flash**
  - **Field Firmware Update Supported**
  - **Support Sleep Notification in Power Off Notification**
  - **Device Health Report Supported**
  - **Secure Removal Type Supported**
  - **Complies with e-MMC Specification version 5.0**
  - **Mechanical design complies with JEDEC® Standard**
  - **Support data bus widths of 1bit, 4bit, 8bit**
- **Support clock frequency**
  - **MMC I/F Clock Frequency: 0~400 MHz**
- **Form Factor**
  - **e-MMC 5.0 Embedded Flash Memory**
  - **BA type:11.5 mm x 13 mm 1.0 mm**
  - **BGA 153 Ball**
  - **Complies with JEDEC® MO-276D Specification**
- **Available Capacities**
  - **4 GB to 32 GB (MLC NAND Flash)**
- **Voltages**
  - **Memory Power (VCC) 3.3V**
  - **Supported Interface Power (VCCQ) voltage: 1.2V and 1.8 V (ranges are 1.1V~1.3V & 1.7V~1.95V)**
- **ECC**
  - **Internal Strong Error Correction supported**
- **High Performance**
  - **Up to 400 MB/s bus transfer rate**
- **High Reliability**
  - **MTBF > 2,100,000 hours**
  - **Endurance: In normal operation condition, guarantees for 3 years product lifetime for half the e-MMC capacity sequential write per day**
- **Temperature Ranges**
  - **Business Temperature Range: -25℃ ~+85℃**
  - **Storage Temperature Range: - 40℃ ~+85℃**

2. Contents

3. Ordering Information

The following Table 1 lists the part No. for Memoright M1600 series e-MMC.

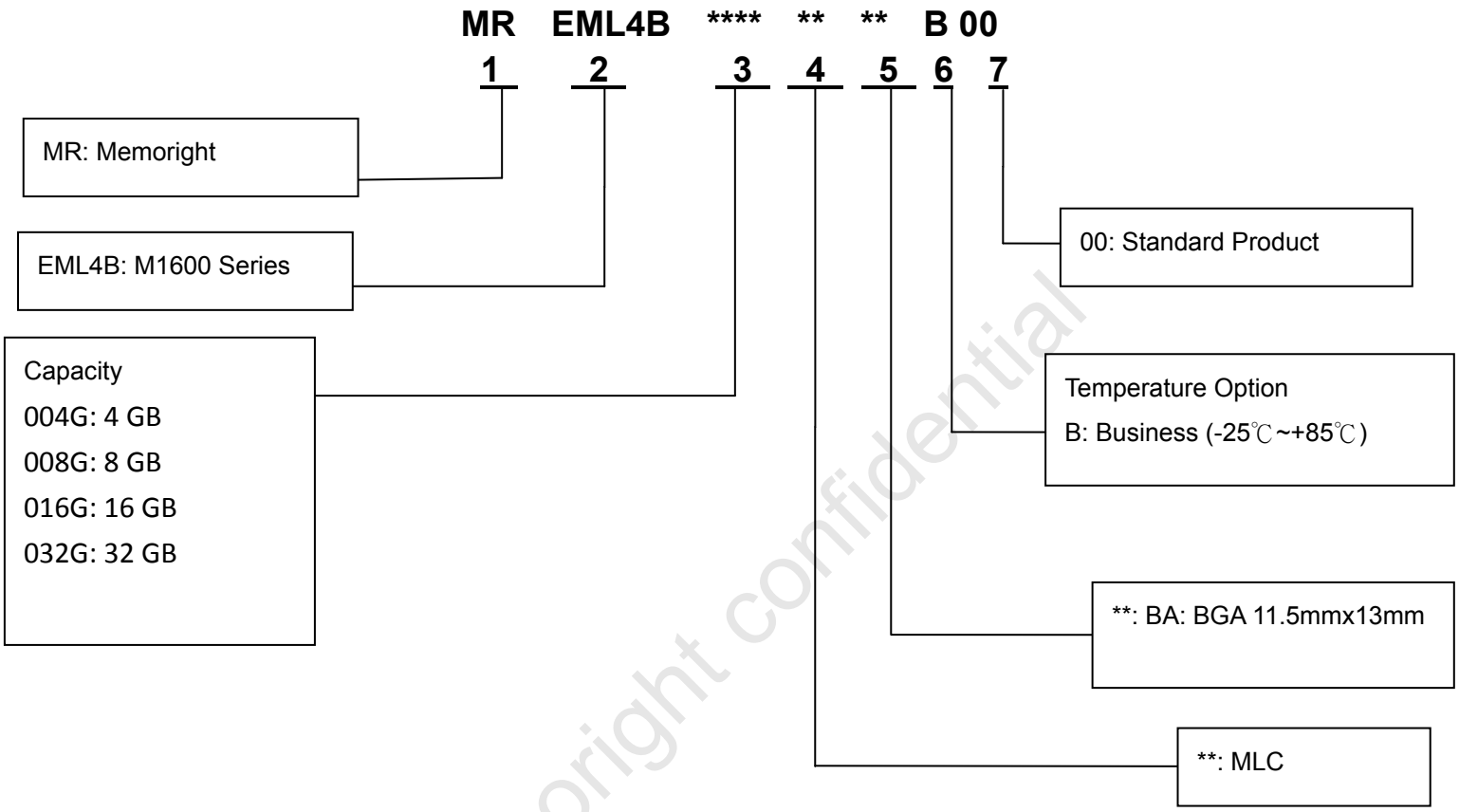
Table 1: Business temperature product list

BGA 153 Ball, 11.5mm x 13mm			
Part Number	**Capacity**	**Flash Type**	**Form Factor**
MREML4B004GOPBAB00	4 GB*	MLC	BGA 153 ball
MREML4B008GOPBAB00	8 GB*	MLC	BGA 153 ball
MREML4B008GGDBAB00	8 GB*	MLC	BGA 153 ball
MREML4B016GGDBAB00	16 GB*	MLC	BGA 153 ball
MREML4B032GGDBAB00	32 GB*	MLC	BGA 153 ball

* 1 GB=1,000,000,000 Bytes

For latest ordering information, please consult Memoright's sales representatives or check on our website: http://www.memoright.com

3.1 Part Number Decoder



4. General Description

Memoright M1600 series is an eMMC 5.0 compliance embedded flash memory module that **integrates a slim controller** and MLC NAND flash into a **BGA package** for various consumer electronics applications such as smart phones, Tablet PC, GPS, etc.
Memoright M1600 series provides low power mode to greatly **extend battery lifetime** and to **achieve high performance** for up to 32GB storage capacity that makes it an ideal solution for multimedia handsets. M1600 integrates advanced MLC flash management technology to achieve balance between cost and performance. It supports three clock frequency of **0-400MHz** and also supports for data bus width modes **of 1bit, 4bit and 8bit**. Besides, it **integrates several patented method such as dynamic & static wear-leveling and advance block management** to **achieve highest data reliability and maximized flash life expectancy**.
Memoright M1600's various advantages such as high performance, capacity and reliability make it the best eMMC storage solution for several consumer electronics devices such as mobile PC and personal handheld devices.

4.1 Physical Description

The important component of Memoright M1600 embedded Flash Memory integrates a Flash controller and NAND Flash memory modules. The Memoright M1600 e-MMC embedded Flash memory solution is provided in BGA 153 ball package.

4.2 System Performance

Table 2: System Performance Table

System Performance		Max.	Unit
Data transfer Rate (e-MMC 5.0)		400	MB/s
Sustained Sequential Read Rate	4 GB	60	MB/s
	8 GB	120	MB/s
	16 GB	150	MB/s
	32 GB	150	MB/s
Sustained Sequential Write Rate	4 GB	10	MB/s
	8 GB	20	MB/s
	16 GB	40	MB/s
	32 GB	40	MB/s
4KB Random Read IOPS	4 GB	3000	IOPS
4KB Random Read IOPS	8 GB	4000	IOPS
4KB Random Read IOPS	16 GB	4000	IOPS
4KB Random Read IOPS	32 GB	4000	IOPS
4KB Random Write IOPS	4 GB	800	IOPS
4KB Random Write IOPS	8 GB	1500	IOPS
4KB Random Write IOPS	16 GB	2000	IOPS
4KB Random Write IOPS	32 GB	2000	IOPS

*1 GB=1024 Mega Bytes

4.3 Environmental Specifications

4.3.1 Recommended Operating Conditions

Table 3: Recommended Operating Conditions

Parameter	Value
Business Operating Temperature	-25℃ to +85℃
Temperature Gradient (℃ per hour max, non-condensing)	20℃ (operating)
Temperature Gradient (℃ per hour max, non-condensing)	30℃ (non-operating)
Power Supply Voltage Range (VCC)	3.3V
Power Supply Voltage Range (VCCQ)	1.7V to 1.95V
	1.1V to 1.3V

4.3.2 Power Consumption (*)

Table 4: Power Consumption

Current/Power Consumption	Max. Current High Voltage Range	Max. Current Low Voltage Range	Unit
Standby Mode Current (Typ.)	250	240	μA
Read Power (Typ.)	200	200	mA
Write Power (Typ.)	200	200	mA

* All value are tested under room temperature 25℃ @ 3.3V

4.3.3 Recommended Storage Conditions

Table 5: Recommended Storage Conditions

Parameter	Value
Business Storage Temperature	-40℃ to +85℃

4.3.4 Shock, Vibration and Humidity

Table 6: Shock, Vibration and Humidity

Parameter	Value
Humidity, Moisture Sensitivity Level	3
Relative Humidity Gradient	30% per hour max
Vibration	10G (Peak, 10~2000Hz)
Shock (Operating)	1000G, (0.5ms duration, half sine wave)
Shock (Non-Operating)	1500G, (0.5ms duration, half sine wave)

4.4 Reliability

Table 7: Reliability

Parameter	Value
Mean Time Between Failures (MTBF)	＞ 2,100,000 hours (Calculation mode: Telcordia SR-332 Issue 1 Method 1, Case 1)

4.5 Physical Dimensions

Physical Dimensions	BA Type	Unit
Length	11.5	mm
Width	13	mm
Thickness (Max.)	1.0	mm

5. Functional Block Diagram

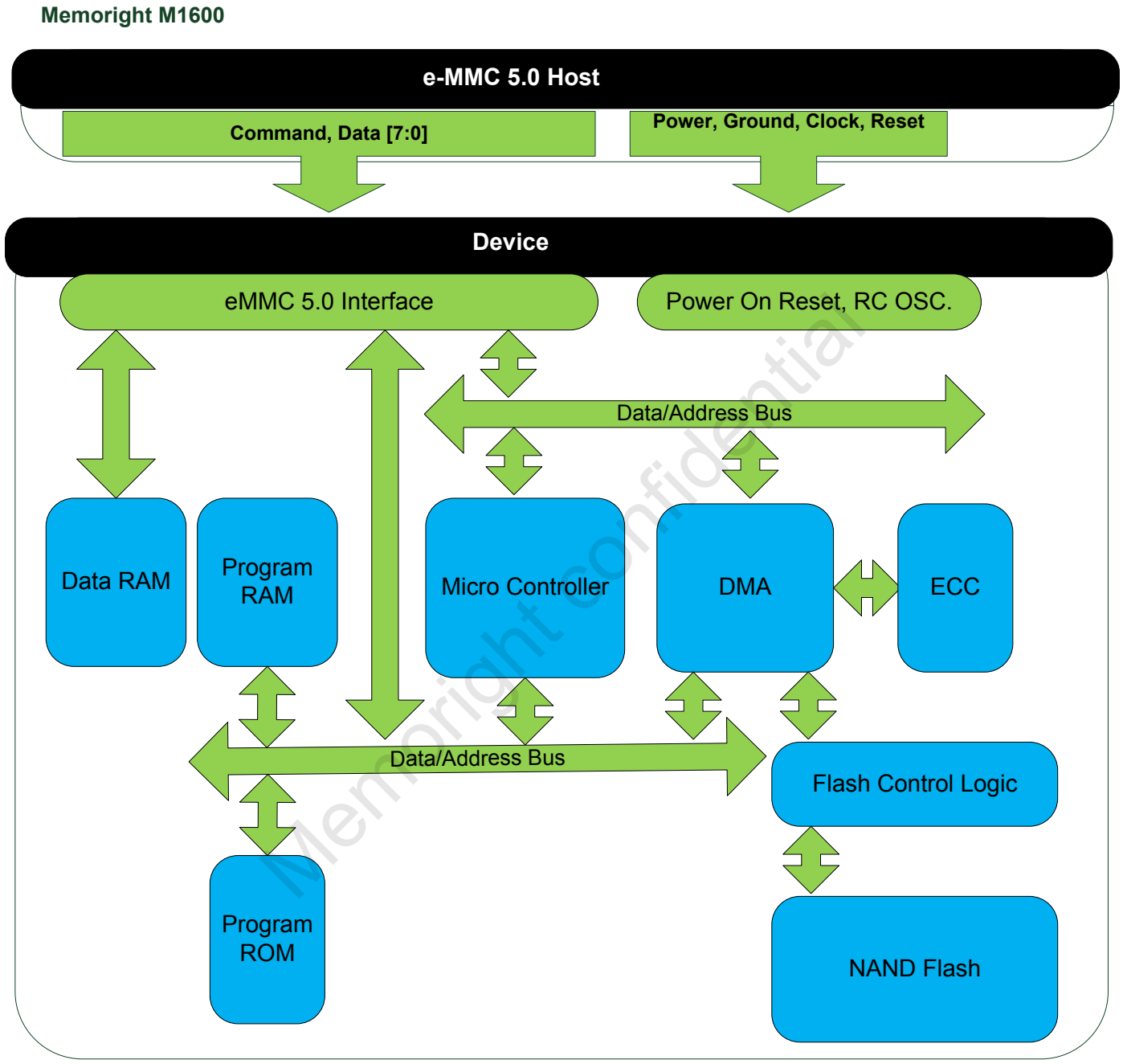
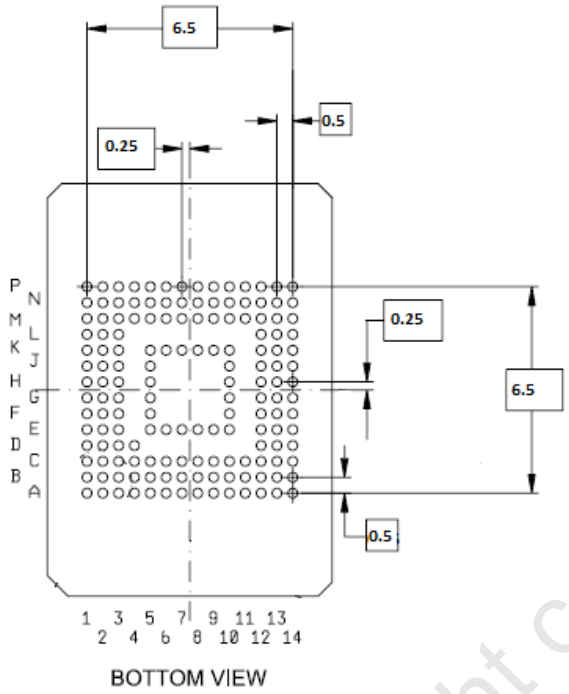


Figure 1: Functional Block Diagram

6. Physical Dimension Diagram

6.1 Bottom View: BA format



Note: Dimensions are in millimeters

Figure 2: Bottom View: BA format

6.2 Side/Top View: BA format

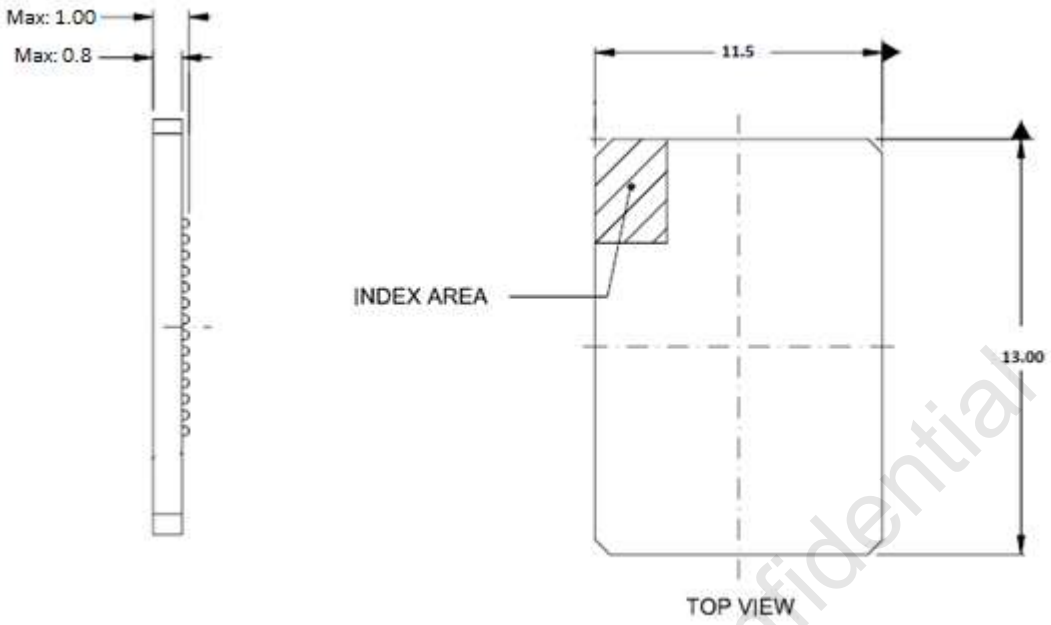


Figure 3 Side/Top View: BA format

Physical Dimensions		Unit
Length	11.5	mm
Width	13	mm
Thickness	1.0	mm

7. Electrical Interface

7.1 M1600 Ball Array (Top-View, Ball-Down)

7.2 Pin and Signal Definition

153 Ball (BA Type)

Table 8 153 Ball Pin and Signal Definition

Pin Name	Signal Name	Input/Output	Description
M6	CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines.
M5	CMD	Input	Command: A bidirectional channel used for device initialization and command transfers. Command has two operating modes: 1) Open-drain for initialization. 2) Push-pull for fast command transfer.
A3	DAT0	I/O	Data I/O0: Bidirectional channel used for data transfer.
A4	DAT1	I/O	Data I/O1: Bidirectional channel used for data transfer.
A5	DAT2	I/O	Data I/O2: Bidirectional channel used for data transfer.
B2	DAT3	I/O	Data I/O3: Bidirectional channel used for data transfer.
B3	DAT4	I/O	Data I/O4: Bidirectional channel used for data transfer.
B4	DAT5	I/O	Data I/O5: Bidirectional channel used for data transfer.
B5	DAT6	I/O	Data I/O6: Bidirectional channel used for data transfer.
B6	DAT7	I/O	Data I/O7: Bidirectional channel

			used for data transfer.
K5	RST_n	Input	Reset signal pin
E6,F5,J10,K9	VCC	Supply	VCC: Flash memory I/F and Flash memory power supply.
C6,M4,N4,P3,P5	VCCQ	Supply	VCCQ: Memory controller core and MMC interface I/O power supply.
E7,G5,H10,K8	VSS	Supply	VSS: Flash memory I/F and Flash memory ground connection.
C4,N2,N5,P4,P6	VSSQ	Supply	VSSQ: Memory controller core and MMC I/F ground connection.
C2	VDDi		VDDi: Connect 0.2μF capacitor from VDDi to ground.
D4	NC Index	—	Index: Can be connected to ground or left floating.
A1,A2,A8,A9,A10, A11,A12,A13,A14, B1,B7,B8,B9,B10, B11,B12,B13,B14 C1,C3,C7,C8,C9, C10,C11,C12,C13 C14,D1,D2,D3,D12, D13,D14,E1,E2,E3, E12,E13,E14,F1,F2, F3,F12,F13,F14,G1, G2,G12,G13,G14,H1, H2,H3,H12,H13,H14, J1,J2,J3,J12,J13,J14, K1,K2,K3,K12,K13,K14, L1,L2,L3, L12,L13,L14, M1, M2, M3, M7, M8, M9, M10, M11, M12,M13,M14,N1,N3, N6,N7,N8,N9,N10,N11, N12,N13,N14,P1,P2,P8 ,P9, P11,P12,P13,P14	NC	—	No connect: Can be connected to ground or left floating.

A6,A7,C5,E5,E8 E9,E10,F10,G3 G10,H5,J5,K6,K7 K10,P7,P10	RFU	—	Reserved for future use. Left it floating for future use.

8. Product Features

The Memoright M1600 contain with a high-speed MultiMediaCard (MMC) controller and Multi-Level Cell (MLC) NAND Flash package in to a low profile BGA package. With functions performance by the controller like error correction code (ECC), wear leveling, and bad block management, the M1600 controller simply transform a program/erase/read device with bad blocks and bad bits (NAND) into a simple write/read memory.

8.1 MMC bus and Power Lines

Memoright M1600 with MMC interface supports the MMC protocol. For more details regarding these buses refer to JEDEC® Standard No. 84-B50. The Memoright M1600 has the following command line as shown in Table 9.

Table 9 M1600 Command Line List

Command	Description
CMD	This signal is a bidirectional command channel used for device initialization and command transfers. The CMD signal has two operating modes: open-drain for initialization, and push-pull for command transfer. Commands are sent from the MMC bus master to the device, and responses are sent from the device to the host.
DAT [7:0]	These are bidirectional data signals. The DAT signals operate in push-pull mode. By default, after power-up or RESET, only DAT0 is used for data transfer. The memory controller can configure a wider data bus for data transfer using either DAT[3:0] (4-bit mode) or DAT[7:0] (8-bit mode).
CLK	Each cycle of the clock directs a transfer on the command line and on the data line(s).The frequency can vary between the minimum and the maximum clock frequency.
RST_n	Reset signal is used for host resetting device, moving the device to pre-idle state. By default, the RST_n signal is temporary disabled in device. Host need to set bit[0:1] in the extended CSD register [162] to 0x1 to enable this functionality before the host uses.
VCCQ	VCCQ is the supply voltage for host interface
VCC	Flash memory I/F and Flash memory power supply.
VDDi	Connect 0.2μF capacitor to stabilize regulator output to controller core logics
VSS/VSSQ	ground lines

8.2 Bus Operating Condition

Table 10 M1600 Command Line List

Parameter	Symbol	Min	Max.	Unit
Peak voltage on all lines		-0.5	VCCQ + 0.5	V
All Inputs				
Input Leakage Current (before initialization sequence and/or the internal pull up resistors connected)		-100	100	µA
Input Leakage Current (after initialization sequence and the internal pull up resistors disconnected)		-2	2	µA
All Outputs				
Output Leakage Current (before initialization sequence)		-100	100	µA
Output Leakage Current (after initialization sequence)		-2	2	µA

Table 11 Dual Voltage Power Supply

Parameter	Symbol	Min	Max.	Unit	Remarks
Supply voltage (low voltage range)	VCCQ	1.70	1.95	V	
		1.1	1.3	V	
	VCC	3.135	3.465	V	
Supply voltage differentials (VSS1, VSS2)		-0.5	0.5	V	
Supply power-up (low voltage range)	tPRUL	-	25	ms	
Supply power-up (high voltage range)	tPRUH	-	35	ms	

The M1600 supports one or more combinations of VCC and VCCQ as shown in Table 12. The VCCQ must be defined at equal to or less than VCC. The available voltage configuration is shown in Table 13

Table 12 M1600 power supply voltage

Parameter	Symbol	Min	Max.	Unit	Remarks
Supply voltage (NAND)	VCC	3.135	3.465	V	
Supply voltage (I/O)	VCCQ	1.1	1.3	V	
		1.7	1.95	V	

8.3 Endurance

In normal operation condition, guarantees for 3 years product lifetime for half the e-MMC capacity sequential write per day

8.4 ECC

The e-MMC provides strong ECC algorithm which reduces error rate and enforces write endurance at the same time.

9. M1600 e-MMC 5.0 Supported Features

9.1 Bootable

Memoright M1600 supports boot operation modes accordingly to eMMC 5.0 interface definition as specified by JEDEC®.

9.1.1 Timing for Boot Operation

The following diagram show Multimedia Card state and timing diagram for normal boot mode. The operation detail for the boot operation is described as following.

If the CMD line is held LOW for 74 clock cycles and more after power-up or reset (no matter through CMD0 with the argument of 0xF0F0F0F0 or assertion of hardware reset for e-MMC, If it is enabled in Extended CSD register byte [162], bits [1:0]) before the first command is issued, the boot data will be prepared internally by the slave once it recognizes that the boot mode is being initiated. The partition from which the master will read the boot data can be selected in advance by using EXT_CSD byte [179], bits [5:3]. The data size 128KB xBOOT_SIZE_MULT (EXT_CSD byte [226]). After the CMD line goes low and within 1 second, the slave starts to send the first boot data to the master on the DAT line (s). The CMD line must be kept LOW by the master to read all of the boot data. The push-pull mode must be used by the master until boot operation is terminated. The master can choose to use single data rate mode with backward-compatible interface timing, single data rate with high-speed interface timing or dual data rate timing (if it supported). The master can choose to receive boot acknowledge from the slave by setting “1” in EXIT_CSD register, byte [179], bit6. And then the master recognizes that the slave is operating in boot mode. The slave has to send acknowledge pattern “010” to the master within 50ms after the CMD goes low if boot acknowledge is enabled. The acknowledge pattern “0-1-0” will not be sent out by the slave if boot acknowledge is disabled. The boot mode can be terminated by the master with the CMD line is High. If the CMD line is pulled High by the master in the middle of data transfer, the slave has to terminate the data transfer or acknowledge pattern within NST clock cycles (one data cycle and end bit cycle). If the boot mode is terminated by the master between consecutive blocks, the slave must release the data line(s) within NST clock cycles.

When all contents of the enabled boot data are sent to the master, boot operation will be terminated. After boot operation is executed, the slave shall be ready for CMD1 operation and the master needs to start a normal MMC initialization sequence by sending CMD1. From CMD signal high to next MMC command, it needs minimum 8 clocks + 48 clocks = 56 clocks. Before CMD1 is issued, if the CMD line is held LOW for less than 74 clock cycles after power-up or the master sends any normal MMC command other than CMD0 with argument 0xFFFFFFFA before initiating boot mode, the slave shall not respond and shall be locked out of boot mode until the next power cycle or hardware reset, and shall enter Idle State. Slave must enter Card Identification Mode and respond to the command when BOOT_PARTITION_ENABLE bits are set and master send CMD1

(SEND_OP_COND). If the boot operation mode is not supported by the slave that is compliant with v4.2 or before or BOOT_PARTITION_ENABLE bit is cleared, slave automatically enter Idle State after power-on.

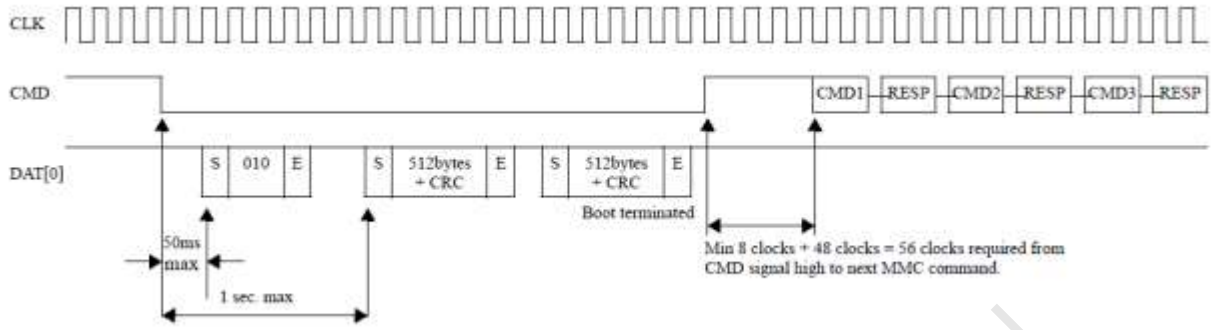


Figure 4 Multimedia Card State & Timing Diagram (Boot Mode)

9.1.2 Alternative Boot Operation

This boot function is compulsory for v4.4 or newer standard. Device that is compliant with v4.4 standard will show “1” bit 0 in the Extended CSD byte [228]. The slave will recognize that boot mode is being initiated and starts preparing boot data internally, if the host issues CMD0 with the argument of 0xFFFFFFFA after 74 clock cycles before CMD1 is issued or the CMD line goes low when the device is powered-up or reset (either assertion of CMD0 with the argument of 0xF0F0F0F0 or H/W reset if it is enabled). The partition from which the master will read the boot data can be selected in advance using EXT_CSD byte [179], bits [5:3]. 128KB xBOOT_SIZE_MULT (EXT_CSD byte [226] is the data size that the master can read during boot operation. The slave starts to send the first boot data to the master on the DAT line(s) within 1 second after CMD with the argument of 0xFFFFFFFA is issued within 1 second. The master must use push-pull mode until boot operation is terminated. The master can choose to use single data rate with high-speed interface timing or dual rate timing (if it is supported), single data rate mode with backward-compatible interface timing. The master can choose to receive boot acknowledge from the slave by setting “1” in EXT_CSD register, byte [179], bit 6 that the master can recognize that the slave is operating in boot mode.

The acknowledge pattern “010” must be sent to the master within 50ms by the slave after the CMD0 with the argument of 0xFFFFFFFA is received for the condition if boot acknowledge is enabled. If boot acknowledge is disabled, the acknowledge pattern “010” will not be sent out by the slave. When all contents of the enabled boot data are sent to the master, boot operation will be terminated.

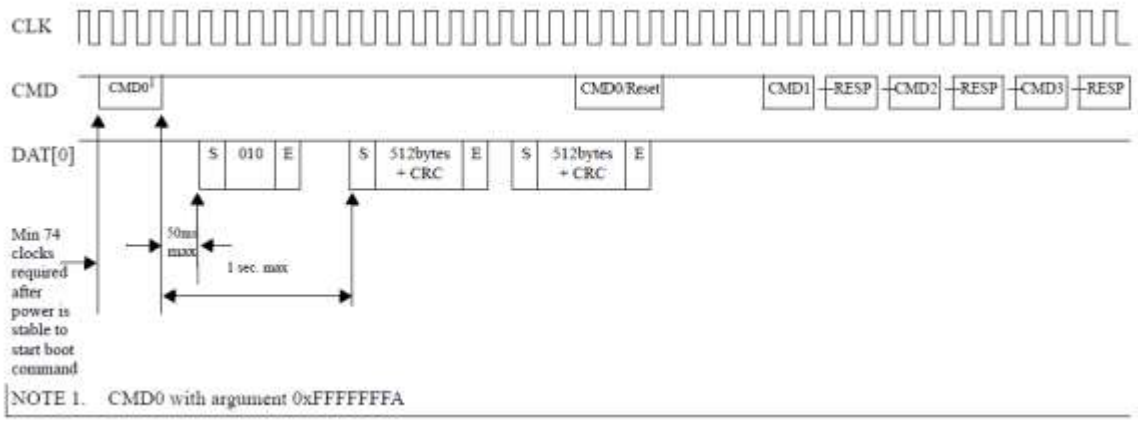


Figure 5 Multimedia Card State & Timing Diagram (Alternative Boot Mode)

9.2 Partition

Memoright M1600 let the host split local memory into partitions with independent addressable space from logical address 0x00000000 for different use. Memory blocks are segmented as hereafter:

- Default factory setting defines two 1 MB boot partitions, as enhanced storage media.

Host can set one segment in User Data Area as enhanced storage media (starting location and Write Protect Group size). This is one-time programmable and can NOT be changed once set.
Up to 4 General Purpose Area can be set as user data or sensitive data or other usage. Partition size must be a multiple of the write protect group. This is one-time programmable and can NOT be changed once set.
There are four default area existed in the memory device including a User Data Area, two possible boot area partitions for booting and the Replay Protected Area Partition to verify and replay-protect data. Before any partitioning operation, the memory initially consists of the User Data Area and Boot Area Partitions. The embedded device offers the possibility of configuring by using host additional split local memory partition with independent addressable space. The addressable space starts from logical address 0x00000000 for different usage models. For two Boot Area Partitions, the size is multiple of 128KB and let the booting from e-MMC can be performed. Four General Purpose Area Partitions is used for sensitive data storage and the size is multiple of a Write Protect Group. Memory manufacturer defines Boot Partitions' size and attributes (read-only). For General Purpose Area Partitions' sizes and attributes, they can be programmed by the host only once in the device life cycle (one-time programmable). Moreover, one segment of the User Data Area can be configured to be implemented as enhanced storage media and to specify its starting location and size in terms of Write Protect Groups. The attributes of the Enhanced User Data Area can be programmed only once during device life cycle. The memory block area can be divided and example of partitions and user data area configuration are shown as following.

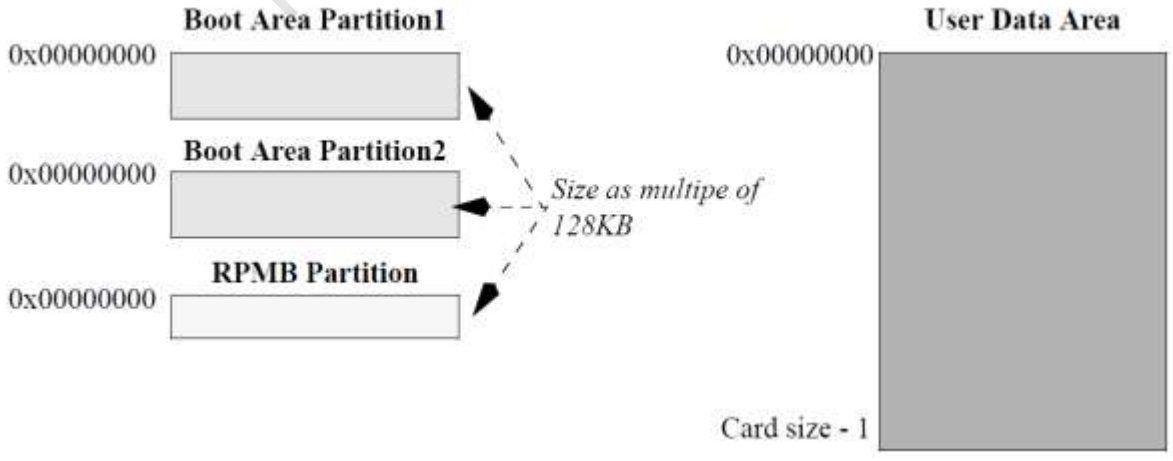


Figure 6 e-MMC Memory Organization

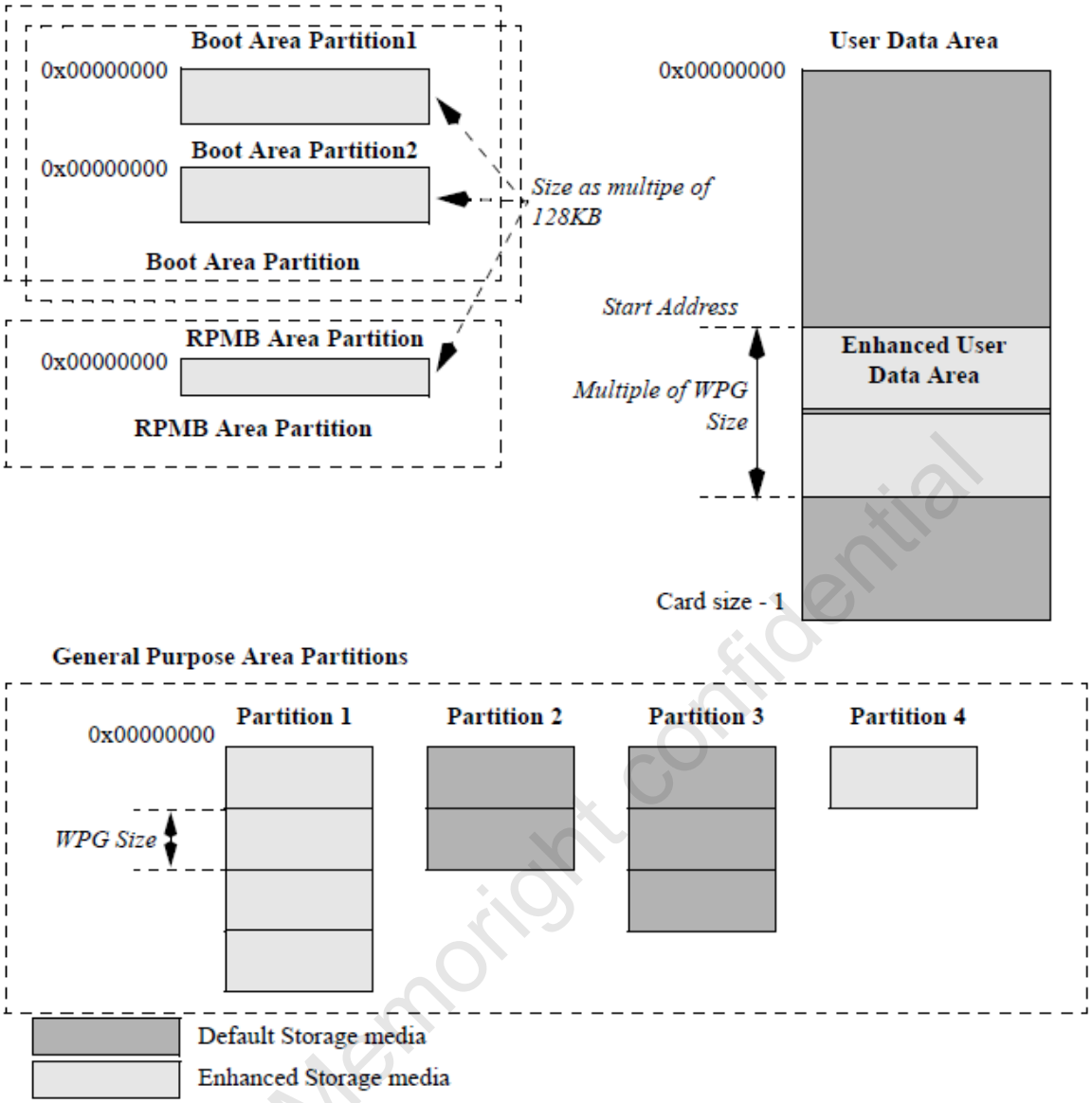


Figure 7 Example of partitions and user data area configuration

9.3 Sleep Mode

Memoright M1600 automatically switches to sleep mode to save power if no further commands are received. Typical sleep transition last 200ns (highest duration before sleep is 850ms, for housekeeping operation). It does not involve any action from host, however, for maximum power saving (lowest current), host clock to the memory device needs to be shut down. For most embedded systems, beside while host is accessing data, devices are always in sleep mode, for greater power saving efficiency. Whenever host is going to access storage device in sleep mode, any issued command will cause device to exit sleep and operation execution.

9.4 Sleep (CMD5)

Memoright M1600 can switch between Sleep and Standby on SLEEP/AWAKE (CMD5) command. In Sleep state, device's power consumption is minimized and reacts only to RESET (CMD0) and SLEEP/AWAKE (CMD5) commands. Any other command will be completely ignored.
The Vcc power supply may even be switched off in Sleep mode to allow further power saving.
For additional information please refer JESD84-B50 6.6.24.

9.5 Enhanced Write

In Memoright M1600 reliable write mode, original data pointed by a logical address will stay the same until the new data has been successfully overwritten. This ensures that the each write transaction will always be reliable and never leaves undefined data in given address. When using enhanced write, data will remain valid even in the case of power drop during programming.

9.6 Secure Erase

Memoright M1600 supports Security Mode Erase command. Once triggered, no command is allowed until Secure Erase is completed.
Memoright M1600 will sanitize the erase area with predefined pattern. The purge will overwrite addressable content with a given character and then erase the NAND flash.
This command meets specific defense or governmental requirements and guarantees Flash memory content can no longer be restored.

9.7 Secure Trim

Memoright M1600 Secure Trim is similar to the Secure Erase but performs a purge on write blocks (512 bytes) .

9.8 Trim

Trim function acts like an Erase but operate at block (512 B) level. For additional information, refer to JEDEC® JESD84-B50.

9.9 Write Protection

To prevent accidental data loss or overwrite, Memoright M1600 provides two levels of write protection:

- Write-protect the whole device (including the Boot Area Partitions, General Purpose Area Partition, and User/Enhanced User Data Area Partition) by setting the permanent or temporary write protect bits in the CSD.
- Write-protect specific segments permanently or temporarily write protected. Segment size can be defined in the EXT_CSD register.

For additional information, refer to JEDEC® JESD84-B50.

9.10 Hardware Reset

Host may reset the device to pre-idle state and disable temporary write protection on related blocks. For additional information, refer to JEDEC® JESD84-B50.

9.11 Background Operations

In order to reduce latency for time critical operations, housekeeping operations (garbage collection, erase and compaction) are executed in the background.
Operations are classified into two types:
Foreground – such as read or write commands and
Background –executed when the device is not busy with host commands.
For additional information on Background Operations, refer to JESD84-B50 standard 6.6.28.

9.12 High Priority Interrupt (HPI)

If OS use on demand-paging to run user process, the host needs to fetch pages in the midst of other operation, so the query might be delayed until the completion of the command.
High priority interrupt (HPI) allows low read latency operation, by holding lower priority process before completion. This mechanism reduces latency, typically to less than 10 ms.
For additional information on the HPI function, refer to JESD84-B50 standard 6.6.29.

9.13 HS400

Memoright M1600 e-MMC supports the HS 400 mode operation which can enhance the transfer speed up to 400 MB/s with up to 400 MHz frequency by 1.8V or 1.2V supply voltages.
After the M1600 is triggered by the host, the host will read the DEVICE_TYPE field in the Extended CSD register to see whether M1600 is HS400 mode supported or not.. For more information on the HS400 mode, refer to JESD84-B50 standard 5.3.6. Please see following diagram for HS400 mode operation flow.

HS400 Mode Selection Sequence

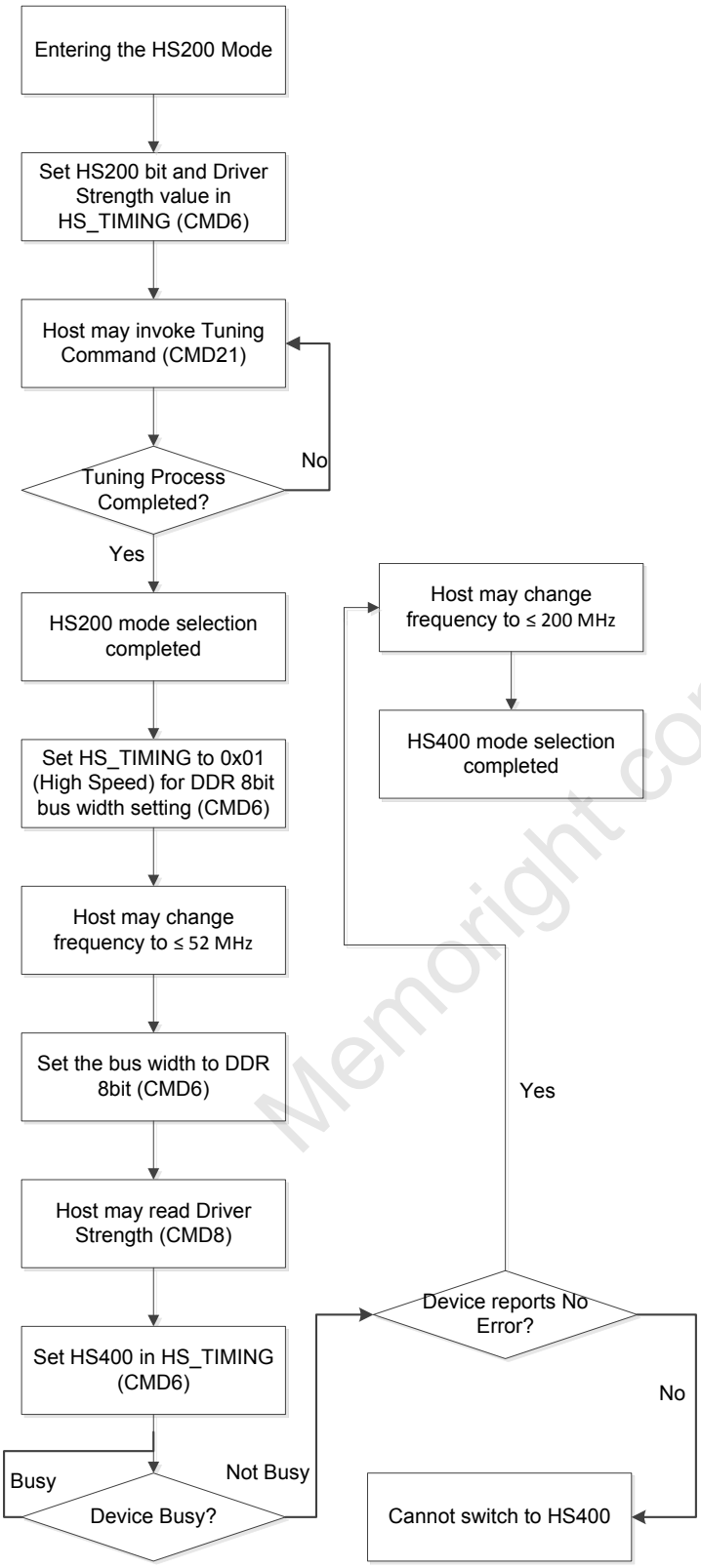


Figure 8 M1600 HS400 operation flow

9.14 Discard Command

The Discard function allows the host to identify the data that is no longer needed and then the data can be erased if necessary during background erase events. The Discard operation is similar to TRIM. After discard operation, the data will be partially or fully remained according to different device. The contents of discarded write block will be decided by the device.

For Discard, if the data is marked for erase, it is no need for the device to guarantee that the host would not retrieve the original data from those “marked” logical block address when a Read operation is directed. However, for TRIM operation, it must response with ‘0’ or ‘1’ depends on different memory technology.

For additional information on the Discard, please refer to JESD84-B50 standard 6.6.15

9.15 Sanitize

The Sanitize operation is a feature that is used to remove data from the device in addition to TRIM and Erase. The Sanitize operation is to physically remove the data from the unmapped user address space in the device. For initializing a Sanitize operation, it is needed to write a value to the extended CSD [165] SANITIZE_START. While the device is performing the sanitize operation, the busy line is asserted, the busy line is asserted. The Sanitize operation will be continued with busy asserted until one of the following events occurs:

- Sanitize operation is complete.
- An HPI is used to abort the operation
- A power failure.
- A hardware reset. For additional information on the Sanitize, refer to JESD84-B50 standard 6.6.14.

9.16 Extended partition types

Each General Purpose partition has a different extended partition attribute. The list of attribute types includes as following:

- Default: no extended attribute is set
- System code: a partition that is rarely updated and contains important system files (e.g. containing the executable files of the host operating system)
- Non-Persistent – a partition that is used for temporary information (e.g. swap file to extend the host virtual memory space)

The device can be optimized for the mixture of storage media characteristics for users per partition. The enhanced and extended attribute set can not be existed in a single partition. For additional information on the extended partition, refer to JESD84-B50 standard

9.17 Context ID Management

Contents can be associated with groups of read and write commands for improving multitasking support and distinguishing large sequential and small random operations. By combining a group of commands with a single context can optimize the performance of data handling for the device.
The context-ID defines one or more concurrent contexts that can be supported by the device. Context ID #0 always exists for backward compatibility and for context-less data. For each context ID (besides #0), there is a configuration field in EXT_CSD to control its behavior. For additional information on the Context ID Management, refer to JESD84-B50 standard 6.6.30.

9.18 Data Tag

The device can receive the specific data types (for instance file system metadata, time-stamps, configuration parameters, etc.) from the host by the Data Tag mechanism. The address will be well defined and the information will be transferred before a write multiple blocks writing operation. During the read and update operations, the device improves the access rate by receiving the Data Tag information. Besides, the Data Tag also helps for more reliable and robust storage solution. For additional information on the Data Tag function, refer to JESD84-B50 standard 6.6.31

9.19 Packed Commands

For reducing overheads, packed commands can be applied to pack read and write commands in one group and transfer it at one time on the bus. For additional information on the Packed Commands, refer to JESD84-B50 standard 6.6.32.

9.20 Real Time Clock

For the host, it provides UTC based absolute time or relative time if available for the host to update real time clock and relative time updates (see CMD49). The main function of the real time clock is to provide real time clock information to the device for internal maintenance use. For additional information on the Real Time Clock, refer to JESD84-B50 standard 6.6.38.

9.21 Dynamic Device Capacity

Dynamic Device Capacity is a function to reduce the bad blocks capacity due to extensive memory usage or aging of Flash to extend the lifespan of the device.
The dynamic device capacity commands and statuses are based on high capacity write protection group size and support only for high capacity devices.
For additional information on the Dynamic Device Capacity, refer to JESD84-B50 standard.

9.22 Power Off Notification

The Power Off Notification is transferred from the host to the device to notify the device to be well prepared before power off occurs.

For additional information on the Power Off Notification, refer to JESD84-B50 standard 6.6.39

9.23 Large Sector Size

The Large sector size can be the smallest unit for the device for internal management. There are two options for the large sector size of high capacity devices as follows.

- Small 512B sectors (supported by devices up to and including 256GB)
- Large 4KB sectors (supported by all devices)

The device reports its native sector size in NATIVE_SECTOR_SIZE field of EXT_CSD [63].

For additional information on the Large Sector Size, refer to JESD84-B50 standard 6.6.37

9.24 Cache

For an e-MMC device, cache is the temporary storage space used for reducing read/write access time (compared to an access to the main non-volatile storage). The cache can be used also for some special operations such as to be the execution memory for memory controller or to be the address mapping table storage space. For additional information on the Large Sector Size, refer to JESD84-B50 standard 6.6.34.

10. Memoright e-MMC Marking Information

10.1 Top View

Industrial Drive

10.1.1 Label Content

- First Row: Memoright Logo
- Second Row: Product Name
- Third Row: Part Number
- Fourth Row: Internal Code-X-YYWWD-S1-C
  - Internal Code: MR internal use only
  - YY: Last two digit of year
  - WW: Work week
  - D: A day within the week
  - S1-C: For internal use only

11. eMMC Signals Connection and Layout Guideline

The paragraph provides you the connection and layout guideline for Memoright e-MMC embedded storage solutions. Please follow following layout guidelines to achieve highest reliability and performance for your e-MMC storage solutions

1. For signal integrity, it is recommended that all of e-MMC signals route on PCB component layer and reference to GND layer.
2. The following table capture from e-MMC spec shows the pull high resistor value for e-MMC interface. It is recommended to put 47KΩ for DAT signals, 10 KΩ for CMD signal and a 22 Ω serial resistor for CLK between host and e-MMC device.

Table 13 Recommended component value for layout

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7		100	KΩ	To prevent bus floating
Pull-up resistance for DAT0-7	R_{DAT}	10		100	KΩ	To prevent bus floating

3. The e-MMC support one or more combinations of Vcc and Vccq as shown below. The Vccq must be defined at equal to or less than Vcc.

For eMMC 5.0, it needs Vccq 1.8V for 400MHz high speed, so it is recommended to supply 3.3V and 1.8V for Vcc and Vccq respectively.

		VCCQ	
		1.1V~1.3V	**1.7V~1.95V**
V_{CC}	**2.7V~3.6V**	Valid	Valid

4. For VCC, It's recommended to put one 0.2uF and one 4.7uF capacitors. For VCCQ, it is recommended to put one 0.2uF and one 2.0uF capacitors

It needs to keep the PWR/GND trace as wide as short as possible. It's recommended to put the capacitors on bottom layer under the power ball.

M1600 Host/e-MMC Connection Guide for x8 Support

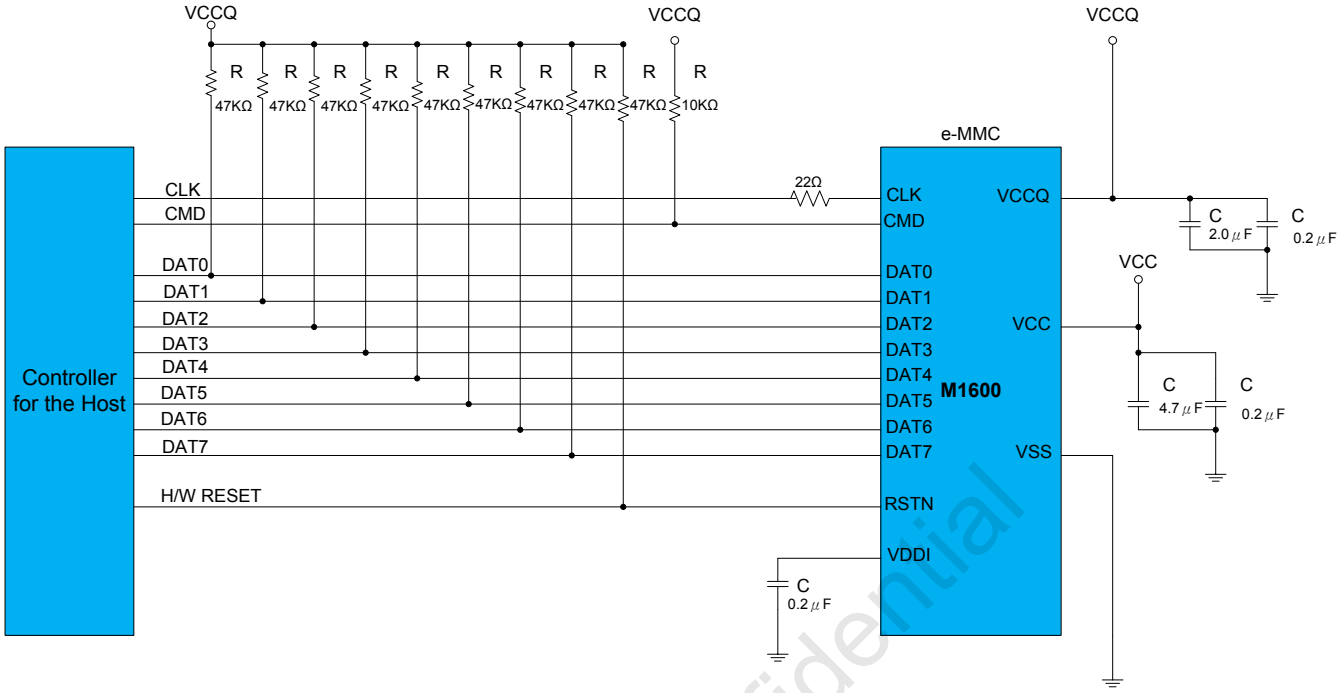


Figure 9 Supported x8 connection guide

M1600 Host/e-MMC Connection Guide for x4 Support

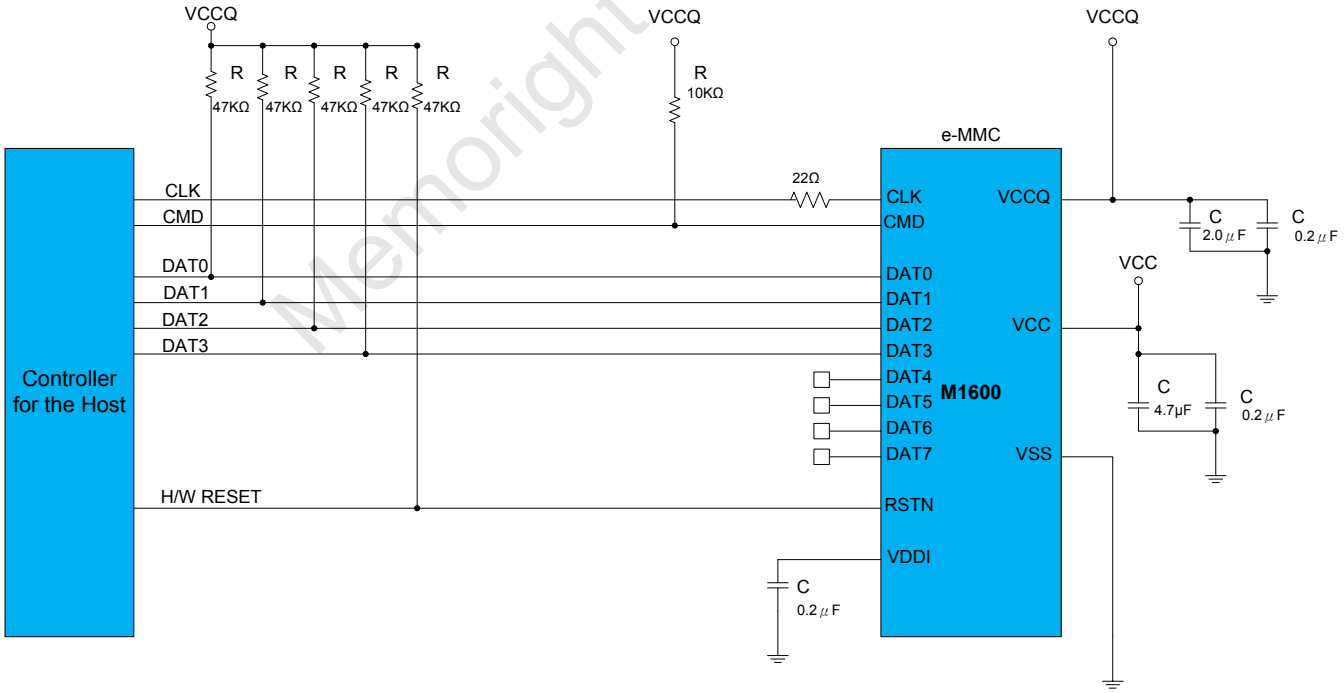


Figure 10 Supported x4 connection guide

12. Register

12.1 Main Register

Register	Offset	Value
OCR Register		C0 ff 80 80
CID Register		00 01 00 65 4d 4d 43 35 30 00 00 00 00 00 00 69
CSD Register		d0 27 01 32 1f 59 03 ff ff ff ff ff 9e 40 40 a9
ExtCSD Register	0x000	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
	0x010	01 03 00 c0 0d 00 00 00 00 00 00 00 00 00 00 00
	0x020	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
	0x030	00 00 00 00 00 00 00 00 01 00 00 00 00 00 00 00
	0x040	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
	0x050	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
	0x060	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
	0x070	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
	0x080	00 00 01 00 00 00 00 00 00 00 00 00 00 00 00 00
	0x090	00 00 00 00 00 00 00 00 00 00 00 00 00 70 00 00
	0x0A0	07 00 00 00 00 00 05 1f 01 00 00 00 00 00 00 00
	0x0B0	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
	0x0C0	07 00 02 00 57 01 02 04 00 00 00 00 00 08 08 08
	0x0D0	08 08 08 00 00 80 e1 00 00 11 00 00 00 04 01 30
	0x0E0	20 0f 10 00 07 00 00 55 02 00 08 08 00 00 00 00
	0x0F0	00 00 00 00 00 00 00 ff 10 80 00 00 00 00 80 04
	0x100	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
	0x110	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
	0x120	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
	0x130	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
	0x140	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
	0x150	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
	0x160	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
	0x170	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
	0x180	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
	0x190	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
	0x1A0	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
	0x1B0	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

	0x1C0	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
	0x1D0	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
	0x1E0	00 00 00 00 00 00 00 00 00 00 00 00 00 00 03 00
	0x1F0	05 00 08 01 3f 3f 01 01 01 00 00 00 00 00 00 00

12.2 OCR Register

Offset	Field	Value
[6:0]	Reserved	00 0000b
[7:7]	1.70 V to 1.95V	1b
[14:8]	2.0 V to 2.6V	000 0000b
[23:15]	2.7 V to 3.6V	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access mode	10b (sector mode)
[31:31]	Card power up status bit	1b (Ready)

12.3 CID Register

Offset	Field	Value
[127:120]	MID	0x0
[119:114]	Reserved	Reserved
[113:112]	CBX	0x40
[111:104]	OID	0x0
[103:56]	PNM	0x654D4D433530 (eMMC50)
[55:48]	PRV	0x00 (0.0)
[47:16]	PSN	0x00000000
[15:8]	MDT	0x00 (Month:0, Year:1997)
[7:1]	CRC	0x34
[0:0]	Always1	0x1

12.4 CSD Register

Offset	Field	Value
[127:126]	CSD_STRUCTURE	0x3 (Version is coded in the CSD_STRUCTURE byte in the EXT_CSD register)
[125:122]	SPEC_VERS	0x4 (Version 4.1, 4.2, 4.3)
[121:120]	Reserved	0x0
[119:112]	TAAC	0x27 (0ms)
[111:104]	NSAC	0x1
[103:96]	TRAN_SPEED	0x32 (26MHz)
[95:84]	CCC	0x1F5 (Card supports class 0 2 4 5 6 7 8)
[83:80]	READ_BL_LEN	0x9 (512 Bytes)
[79:79]	READ_BL_PARTIAL	0x0
[78:78]	WRITE_BLK_MISALIGN	0x0
[77:77]	READ_BLK_MISALIGN	0x0
[76:76]	DSR_IMP	0x0
[75:74]	Reserved	0x0
[73:62]	C_SIZE	0xFFF (device density is greater than 2GB)
[61:59]	VDD_R_CURR_MIN	0x7 (100mA)
[58:56]	VDD_R_CURR_MAX	0x7 (200mA)
[55:53]	VDD_W_CURR_MIN	0x7 (100mA)
[52:50]	VDD_W_CURR_MAX	0x7 (200mA)
[49:47]	C_SIZE_MULT	0x7 (512)
[46:42]	ERASE_GRP_SIZE	0x1F (31)
[41:37]	ERASE_GRP_MULT	0x1F (31)
[36:32]	WP_GRP_SIZE	0x1F
[31:31]	WP_GRP_ENABLE	0x1
[30:29]	DEFAULT_ECC	0x0
[28:26]	R2W_FACTOR	0x7 (128)
[25:22]	WRITE_BL_LEN	0x9 (512 Bytes)
[21:21]	WRITE_BL_PARTIAL	0x0
[20:17]	Reserved	0x0
[16:16]	CONTENT_PROT_APP	0x0
[15:15]	FILE_FORMAT_GRP	0x0(Hard disk-like file system with partition table)
[14:14]	COPY	0x1
[13:13]	PERM_WRITE_PROTECT	0x0
[12:12]	TMP_WRITE_PROTECT	0x0
[11:10]	FILE_FORMAT	0x0

[9:8]	ECC code	0x0(none)
[7:1]	CRC	0x54
[0:0]	Always1	0x1

12.5 Extended CSD Register

Offset	Field	Value
Properties Segment		
[511:506]	Reserved	00 00 00 00 00 00
[505]	EXT_SECURITY_ERR	0x0
[504]	S_CMD_SET	0x1
[503]	HPI_FEATURES	0x1
		(HPI_SUPPORT, HPI mechanism implementation based on CMD13)
[502]	BKOPS_SUPPORT	0x1
[501]	MAX_PACKED_READS	0x3F
[500]	MAX_PACKED_WRITES	0x3F
[499]	DATA_TAG_SUPPORT	0x1
[498]	TAG_UNIT_SIZE	0x8
[497]	TAG_RES_SIZE	0x0
[496]	CONTEXT_CAPABILITIES	0x5
[495]	LARGE_UNIT_SIZE_M1	0x0
[494]	EXT_SUPPORT	0x3
[493]	SUPPORTED_MODES	0x0
		bit[0]=0x0 (FFU(Field Firmware Update) is not supported.),
		bit[1]=0x0 (VSM(Vendor Specific Mode) is not supported.)
[492]	FFU_FEATURES	0x0
		bit[0]=0x0 (Device don't support FFU_FEATURES.)
[491]	OPERATION_CODE_TIMEOUT	0x0
		(Not Defined)
[490:487]	FFU_ARG	00 00 00 00
[486:306]	Reserved	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
		00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
		00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
		00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
		00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
		00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
		00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
		00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
		00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

		00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
		00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
		00 00 00 00 00
[305:302]	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	0x00000000
[301:270]	VENDOR_PROPRIETARY_HEALTH_REPORT	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
		00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
[269]	DEVICE_LIFE_TIME_EST_TYP_B	0x0
		(Not Defined)
[268]	DEVICE_LIFE_TIME_EST_TYP_A	0x0
		(Not Defined)
[267]	PRE_EOL_INFO	0x0
		(Not Defined)
[266]	OPTIMAL_READ_SIZE	0x0
		(Not Defined)
[265]	OPTIMAL_WRITE_SIZE	0x0
		(Not Defined)
[264]	OPTIMAL_TRIM_UNIT_SIZE	0x0
		(Not Defined)
[263:262]	DEVICE_VERSION	0x0000
[261:254]	FIRMWARE_VERSION	00 00 00 00 00 00 04 80
[253]	PWR_CL_DDR_200_360	0x0
[252:249]	CACHE_SIZE	0x00000080 (Size of the Cache = 128 Kbytes)
[248]	GENERIC_CMD6_TIME	0x10 (160 ms)
[247]	POWER_OFF_LONG_TIME	0xFF (2550 ms)
[246]	BKOPS_STATUS	0x0
[245:242]	CORRECTLY_PRG_SECTORS_NUM	0x00000000
[241]	INI_TIMEOUT_AP	0x0 (0 ms)
[240]	Reserved	0x0
[239]	PWR_CL_DDR_52_360	0x0
[238]	PWR_CL_DDR_52_195	0x0
[237]	PWR_CL_200_195	0x0

[236]	PWR_CL_200_130	0x0
[235]	MIN_PERF_DDR_W_8_52	0x8
[234]	MIN_PERF_DDR_R_8_52	0x8
[233]	Reserved	0x0
[232]	TRIM_MULT	0x2 (TRIM Timeout = 600 ms)
[231]	SEC_FEATURE_SUPPORT	0x55
		bit[0]=0x1(SECURE_ER_EN),
		bit[2]=0x1(SEC_BD_BLK_EN),
		bit[4]=0x1(SEC_GB_CL_EN),
		bit[6]=0x1(SEC_SANITIZE)
[230]	SEC_ERASE_MULT	0x0 (Secure Erase Timeout = 0 ms)
[229]	SEC_TRIM_MULT	0x0 (Secure TRIM Timeout = 0 ms)
[228]	BOOT_INFO	0x7
		bit[0]=0x1(Support ALT_BOOT_MODE),
		bit[1]=0x1(Support DDR_BOOT_MODE),
		bit[2]=0x1(Support HS_BOOT_MODE)
[227]	Reserved	0x0
[226]	BOOT_SIZE_MULTI	0x10 (Boot Partition size = 2048 Kbytes)
[225]	ACC_SIZE	0xF (Super-page size = 8388608 Kbytes)
[224]	HC_ERASE_GRP_SIZE	0x20 (Erase Unit Size = 16384 Kbytes)
[223]	ERASE_TIMEOUT_MULT	0x30 (1200 ms)
[222]	REL_WR_SEC_C	0x1
[221]	HC_WP_GRP_SIZE	0x4 (65536 Kbytes)
[220]	S_C_VCC	0x0(Not defined)
[219]	S_C_VCCQ	0x0(Not defined)
[218]	PRODUCTION_STATE_AWARENESS_TIMEOUT	0x0
[217]	S_A_TIMEOUT	0x11 (13107200 ns)
[216]	SLEEP_NOTIFICATION_TIME	0x0
[215:212]	SEC_COUNT	0x00E18000 (Device density = 7.047 Gb)

[211]	Reserved	0x0
[210]	MIN_PERF_W_8_52	0x8
[209]	MIN_PERF_R_8_52	0x8
[208]	MIN_PERF_W_8_26_4_52	0x8
[207]	MIN_PERF_R_8_26_4_52	0x8
[206]	MIN_PERF_W_4_26	0x8
[205]	MIN_PERF_R_4_26	0x8
[204]	Reserved	0x0
[203]	PWR_CL_26_360	0x0
[202]	PWR_CL_52_360	0x0
[201]	PWR_CL_26_195	0x0
[200]	PWR_CL_52_195	0x0
[199]	PARTITION_SWITCH_TIME	0x4 (40 ms)
[198]	OUT_OF_INTERRUPT_TIME	0x2 (20 ms)
[197]	DRIVER_STRENGTH	0x1
[196]	DEVICE_TYPE	0x57
		bit[0]=0x1(HS @ 26MHz - at rated device voltage(s)),
		bit[1]=0x1(HS @ 52MHz - at rated device voltage(s)),
		bit[2]=0x1(HS_DDR @ 52MHz - 1.8V or 3V I/O),
		bit[3]=0x0(HS_DDR @ 52MHz - 1.2V I/O),
		bit[4]=0x1(HS200_SDR @ 200 MHz - 1.8V I/O),
		bit[5]=0x0(HS200_SDR @ 200 MHz - 1.2V I/O),
		bit[6]=0x1(HS400_DDR @ 200MHz V 1.8V I/O),
		bit[7]=0x0(HS400_DDR @ 200MHz V 1.2V I/O)
[195]	Reserved	0x0
[194]	CSD_STRUCTURE	0x2 (CSD version No. 1.2)
[193]	Reserved	0x0
[192]	EXT_CSD_REV	0x7 (Revision 1.7, for MMC v5.0)

[191]	CMD_SET	0x0
[190]	Reserved	0x0
[189]	CMD_SET_REV	0x0 (v4.0)
[188]	Reserved	0x0
[187]	POWER_CLASS	0x0
[186]	Reserved	0x0
[185]	HS_TIMING	0x1 (High Speed)
[184]	Reserved	0x0
[183]	BUS_WIDTH	0x0
[182]	Reserved	0x0
[181]	ERASED_MEM_CONT	0x0
[180]	Reserved	0x0
[179]	PARTITION_CONFIG	0x0
		bit[2:0]=0x0(PARTITION_ACCESS: No access to boot partition (default))
		bit[5:3]=0x0(BOOT_PARTITION_ENABLE: Device not boot enabled (default))
		bit[6]=0x0(BOOT_ACK: No boot ACK sent (default))
[178]	BOOT_CONFIG_PROT	0x0
		bit[0]=0x0(PWR_BOOT_CONFIG_PROT: is not enabled (default))
		bit[4]=0x0(PERM_BOOT_CONFIG_PROT: is not enabled (default))
[177]	BOOT_BUS_CONDITIONS	0x0
		bit[1:0]=0x0(BOOT_BUS_WIDTH: x1(sdr) or x4(ddr) bus width in boot operation mode (default))
		bit[2]=0x0(RESET_BOOT_BUS_CONDITIONS: Reset (default))
		bit[4:3]=0x0(BOOT_MODE: SDR, backward compatible timings (default))
[176]	Reserved	0x0

[175]	ERASE_GROUP_DEF	0x0
[174]	BOOT_WP_STATUS	0x0
		bit[1:0]=0x0(B_AREA_1_WP: Boot Area 1 is not protected)
		bit[3:2]=0x0(B_AREA_2_WP: Boot Area 2 is not protected)
[173]	BOOT_WP	0x0
		bit[0]=0x0(B_PWR_WP_EN)
		bit[1]=0x0(B_PWR_WP_SEC_SEL)
		bit[2]=0x0(B_PERM_WP_EN)
		bit[3]=0x0(B_PERM_WP_SEC_SEL)
		bit[4]=0x0(B_PERM_WP_DIS)
		bit[6]=0x0(B_PWR_WP_DIS)
		bit[7]=0x0(B_SEC_WP_SEL)
[172]	Reserved	0x0
[171]	USER_WP	0x0
		bit[0]=0x0(US_PWR_WP_EN)
		bit[2]=0x0(US_PERM_WP_EN)
		bit[3]=0x0(US_PWR_WP_DIS)
		bit[4]=0x0(US_PERM_WP_DIS)
		bit[6]=0x0(CD_PERM_WP_DIS)
		bit[7]=0x0(PERM_PSWD_DIS)
[170]	Reserved	0x0
[169]	FW_CONFIG	0x0
[168]	RPMB_SIZE_MULT	0x1 (RPMB partition size = 128 Kbytes)
[167]	WR_REL_SET	0x1F
		bit[0]=0x1(WR_DATA_REL_USR)
		bit[1]=0x1(WR_DATA_REL_1)
		bit[2]=0x1(WR_DATA_REL_2)
		bit[3]=0x1(WR_DATA_REL_3)
		bit[4]=0x1(WR_DATA_REL_4)
[166]	WR_REL_PARAM	0x5
		bit[0]=0x1(HS_CTRL_REL)
		bit[1]=0x0(EN_REL_WR)
[165]	SANITIZE_START	0x0

[164]	BKOPS_START	0x0
[163]	BKOPS_EN	0x0
[162]	RST_n_FUNCTION	0x0
		bit[1:0]=0x0(RST_n_ENABLE: RST_n signal is temporarily disabled (default))
[161]	HPI_MGMT	0x0
[160]	PARTITIONING_SUPPORT	0x7
		bit[0]=0x1(PARTITIONING_EN)
		bit[1]=0x1(ENH_ATTRIBUTE_EN)
		bit[2]=0x1(WR_DATA_REL_2)
[159:157]	MAX_ENH_SIZE_MULT	0x000070 (Max Enhanced Area = 7340032 Kbytes)
[156]	PARTITIONS_ATTRIBUTE	0x0
		bit[0]=0x0(ENH_USR)
		bit[1]=0x0(ENH_GPP_1)
		bit[2]=0x0(ENH_GPP_2)
		bit[3]=0x0(ENH_GPP_3)
		bit[4]=0x0(ENH_GPP_4)
[155]	PARTITION_SETTING_COMPLETED	0x0
[154:143]	GP_SIZE_MULT	0x000000(GPP1)
		0x000000(GPP2)
		0x000000(GPP3)
		0x000000(GPP4)
[142:140]	ENH_SIZE_MULT	0x000000 (Enhanced User Area Size = 0 Kbytes)
[139:136]	ENH_START_ADDR	0x00000000
[135]	Reserved	0x0
[134]	SEC_BAD_BLK_MGMNT	0x0 (SEC_BAD_BLK)
[133]	PRODUCTION_STATE_AWARENESS	0x0
[132]	TCASE_SUPPORT	0x0
[131]	PERIODIC_WAKEUP	0x0 (WAKEUP_PERIOD: 0 infinity (no wakeups))
[130]	PROGRAM_CID_CSD_DDR_SUPPORT	0x1
[129:128]	Reserved	0x0000

[127:64]	VENDOR_SPECIFIC_FIELD	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
		00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
		00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
		00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
[63]	NATIVE_SECTOR_SIZE	0x0
[62]	USE_NATIVE_SECTOR	0x0
[61]	DATA_SECTOR_SIZE	0x0
[60]	INI_TIMEOUT_EMU	0x0 (0 ms)
[59]	CLASS_6_CTRL	0x0 (Write Protect (Default))
[58]	DYNCAP_NEEDED	0x0
[57:56]	EXCEPTION_EVENTS_CTRL	0x0001
		bit[1]=0x0(DYNCAP_EVENT_EN)
		bit[2]=0x0(SYSPOOL_EVENT_EN)
		bit[3]=0x0(PACKED_EVENT_EN)
		bit[4]=0x0(EXTENDED_SECURITY_EN)
[55:54]	EXCEPTION_EVENTS_STATUS	0x0000
		bit[0]=0x0(URGENT_BKOPS)
		bit[1]=0x0(DYNCAP_NEEDED)
		bit[2]=0x0(SYSPOOL_EXHAUSTED)
		bit[3]=0x0(PACKED_FAILURE)
		bit[4]=0x0(EXTENDED_SECURITY_FAILURE)
[53:52]	EXT_PARTITIONS_ATTRIBUTE	0x0000
		0x00(EXT_1)
		0x00(EXT_2)
		0x00(EXT_3)
		0x00(EXT_4)
[51:37]	CONTEXT_CONF	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
[36]	PACKED_COMMAND_STATUS	0x0
		bit[0]=0x0(Error)
		bit[1]=0x0(Indexed Error)
[35]	PACKED_FAILURE_INDEX	0x0
[34]	POWER_OFF_NOTIFICATION	0x0
		(NO_POWER_NOTIFICATION)

[33]	CACHE_CTRL	0x0
		(Cache is OFF)
[32]	FLUSH_CACHE	0x0
		(Reset value)
[31]	Reserved	0x0
[30]	MODE_CONFIG	0x0
		(Normal Mode: To keep the compatibility)
[29]	MODE_OPERATION_CODES	0x0
		(Reserved)
[28:27]	Reserved	00 00
[26]	FFU_STATUS	0x0
		(Success)
[25:22]	PRE_LOADING_DATA_SIZE	00 00 00 00
[21:18]	MAX_PRE_LOADING_DATA_SIZE	00 0D C0 00
[17]	PRODUCT_STATE_AWARENESS_ENABLEMENT	0x3
		bit[0]=0x1(Manual mode is supported)
		bit[1]=0x1(Auto mode is supported)
		bit[4]=0x0(Production State Awareness is enabled)
		bit[5]=0x0(Auto mode is enabled)
[16]	SECURE_REMOVAL_TYPE	0x1
		[Supported Secure Removal Type]
		bit[0]=0x1(info. removed by an erase of the physical memory)
		bit[1]=0x0
		bit[2]=0x0
		bit[3]=0x0
		[Configure Secure Removal Type]
		bit[5:4]=0x0(info. removed by an erase of the physical memory)
[15:0]	Reserved	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

13. Contact Information

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