

Memoright M1000 Series

e-MMC 4.41 Embedded Flash Memory

Part Number: MREMK1A****O*ACB00

Product Specification

Version 0.2

Summary

This document serves as reference basis for e-MMC M1000 Series Multimedia Card technical characteristics and helps you choose Memoright NAND Flash storage solution.

Revision History

Revision	Description	Date
0.1	Initial Draft	Nov. 15, 2010
0.2	Preliminary	Jan. 18, 2011

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1. Overview

1.1 Product Description

Memoright M1000 Series is an embedded flash memory module special design for applications like smart phones, mobile handheld device, Tablet PC, cameras, GPS, PDAs, digital recorders, MP3 players, etc. M1000 Series is a hybrid device combining that package a slim flash controller and standard MLC NAND flash in to standard BGA Form factor that fully compliance with industry standard e.MMC 4.41 interface.

With new e-MMC 4.41 standard features such as Enhance reliable write, HPI, Boot, RPMB partitions, Background Operations and HW Reset make M1000 the most reliable e-MMC device to storage system data and application code.

Memoright M1000 support low power mode that can extend the lift time for the battery embedded device such as personal multimedia player. M1000 is fully compatible with JEDEC e-MMC 4.41 standard form factor which high performance, up to 64GB storage capacity and low power consumption make it an ideal solution for multimedia handsets.

The M1000 controllers is furthering with advantage NAND flash management technology that can utilize advance Multi-Level Cell (MLC) NAND Flash provide a perfect balance between device cost and performance.

M1000 architecture and embedded firmware fully emulates a hard disk to the host processor, enabling read/write operations that are identical to a standard, sector-based hard drive. Memoright firmware employs patented methods include dynamic and static wear-leveling, garbage collection, virtual mapping, and advance block management to ensure high data reliability and maximize flash life expectancy.

Utilizing the MLC NAND Flash, Memoright M1000 offers up to 64GB data capacity which can meet the mess storage need on multimedia device and mobile PC storage need. M1000 also embedded with intelligent e-MMC controller that will monitoring the interface protocols and execute process like data storage and retrieval, clock control, Error correction code (ECC) and power management.

1.2 Block Diagram

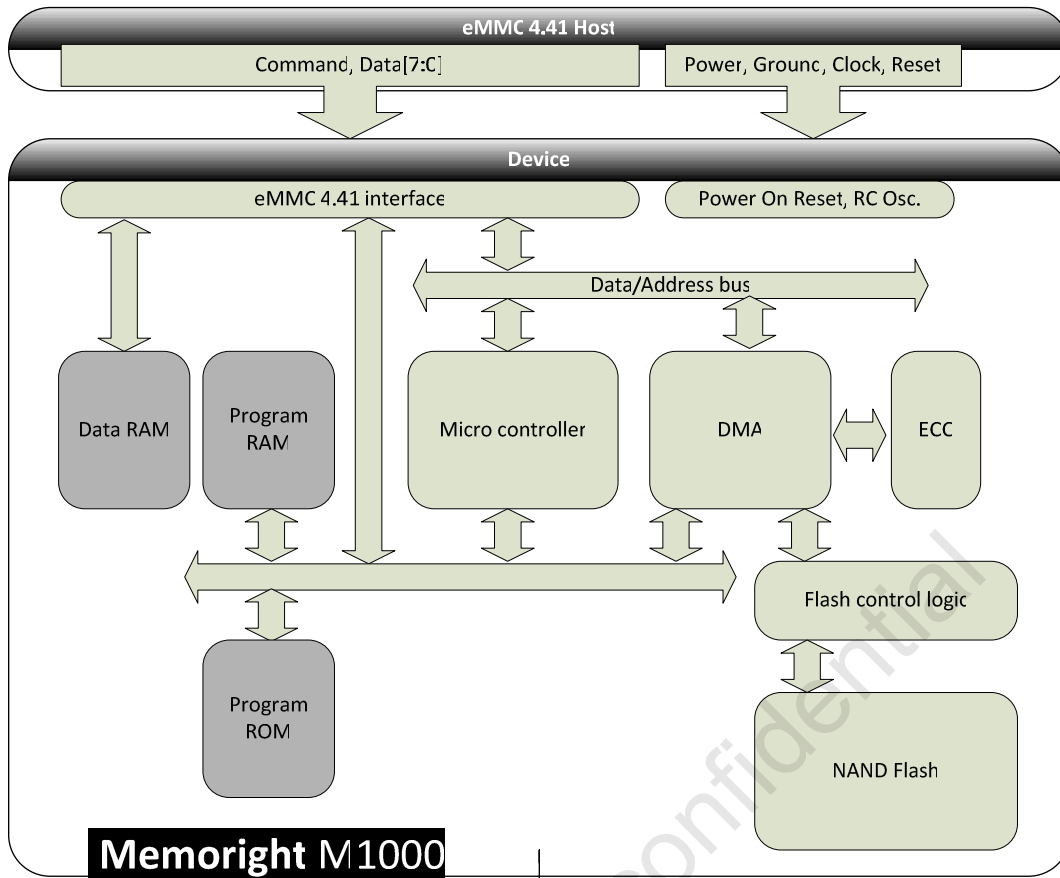


Fig. 1 Memoright M1000 Block Diagram

1.3 Product Overview

Memoright M1000 e-MMC 4.41 embedded flash memory devices is featuring with following specification:

- Embedded with e-MMC Flash Controller and NAND flash
- Complies with e.MMC Specification Ver. 4.41
- Write-Block-Length 512
- Support Command Class 0~7
- Mechanical design complies with JEDEC Standard No. JESD84-C44 Specification
- Packages
 - BGA 169 Ball
 - Complies with JEDEC MO-276C Specification
- AC type: 14 mm x 18 mm x 1.4 mm
- Densities: up to 64GB (MLC)
- Core Voltage (VCC) 2.7-3.6V
- I/O (VCCQ) voltage, either: 1.7-1.95v or 2.7-3.6v
- Temperature:
 - Operate: -20 C° ~ +85 C°
 - Storage: -40 C° ~ +85 C°
- Multiple Data Bus Widths support
 - 1bit
 - 4bit
 - 8bit
- Supported clock frequencies mode:
 - 0-20 MHz
 - 0-26 MHz
 - 0-52 MHz
- Up to 52 MB/sec bus transfer rate
- Internal Error Correction support: BCH: 70bit/1KB correction ECC
- Eases the design and validation process

2. Product Features

The Memoright M1000 contain with a high-speed MultiMediaCard (MMC) controller and Multi-Level Cell (MLC) NAND Flash package in to a low profile BGA package. With functions performance by the controller like error correction code (ECC), wear leveling, and bad block management, the M1000 controller simply transform a program/erase/read device with bad blocks and bad bits (NAND) into a simple write/read memory.

2.1 MMC bus and Power Lines

Memoright M1000 with MMC interface supports the MMC protocol. For more details regarding these buses refer to JEDEC Standard No. 84-A441. The Memoright M1000 has the following command line show as Table 1.

Table 1: M1000 Command Line List

CMD	This signal is a bidirectional command channel used for device initialization and command transfers. The CMD signal has two operating modes: open-drain for initialization, and push-pull for command transfer. Commands are sent from the MMC bus master to the device, and responses are sent from the device to the host.
DAT [7:0]	These are bidirectional data signals. The DAT signals operate in push-pull mode. By default, after power-up or RESET, only DAT0 is used for data transfer. The memory controller can configure a wider data bus for data transfer using either DAT[3:0] (4-bit mode) or DAT[7:0] (8-bit mode).
CLK	Each cycle of the clock directs a transfer on the command line and on the data line(s).The frequency can vary between the minimum and the maximum clock frequency.
RST_n	Reset signal is used for host resetting device, moving the device to pre-idle state. By default, the RST_n signal is temporary disabled in device. Host need to set bit[0:1] in the extended CSD register [162] to 0x1 to enable this functionality before the host uses.
VCCQ	VCCQ is the supply voltage for host interface
VCC	Flash memory I/F and Flash memory power supply.
VDDi	Connect 0.1μF capacitor to stabilize regulator output to controller core logics
VSS/VSSQ	ground lines

2.2 Bus operating conditions

Table 2: M1000 Command Line List

Parameter	Symbol	Min	Max.	Unit
Peak voltage on all lines		-0.5	VCCQ + 0.5	V
All Inputs				
Input Leakage Current (before initialization sequence and/or the internal pull up resistors connected)		-100	100	μA
Input Leakage Current (after initialization sequence and the internal pull up resistors disconnected)		-2	2	μA
All Outputs				
Output Leakage Current (before initialization sequence)		-100	100	μA
Output Leakage Current (after initialization sequence)		-2	2	μA

Table 3: Power supply: dual-voltage

Parameter	Symbol	Min	Max.	Unit	Remarks
Supply voltage (low voltage range)	VDDL	1.70	1.95	V	1.95V–2.7V range is not supported
Supply voltage (high voltage range)	VDDH	2.7	3.6	V	
Supply voltage differentials (VSS1, VSS2)		-0.5	0.5	V	
Supply power-up (low voltage range)	tPRUL	-	25	ms	
Supply power-up (high voltage range)	tPRUH	-	35	ms	

The M100 supports one or more combinations of VCC and VCCQ as shown in Table 4. The VCCQ must be defined at equal to or less than VCC. The available voltage configuration is shown in Table 5.

Table 4: M1000 Power supply voltage

Parameter	Symbol	Min	Max	Unit	Remarks
Supply voltage (NAND)	VCC	2.7	3.6	V	
		1.7	1.95	V	
Supply voltage (I/O)	VCCQ	2.7	3.6	V	
		1.65	1.95	V	
		1.1	1.3	V	
Supply power-up for 3.3V	tPRUH		35	ms	
Supply power-up for 1.8V			25	ms	
Supply power-up for 1.2V			20	ms	

Table 5: M1000 voltage combinations

		VCCQ		
		1.1V-1.3V	1.65V-1.95V	2.7V-3.6V
V CC	2.7V-3.6V	Valid	Valid	Valid
	1.7V-1.95V	Valid	Valid	NOT VALID

3. M1000 e-MMC 4.41 Support Features

3.1 Bootable

Memoright M1000 supports boot operation modes accordingly to eMMC 4.41 interface definition as specified by JEDEC.

3.2 Sleep Mode

Memoright M1000 automatically switch to sleep mode to save power if no further commands are received. Typical sleep transition last 200ns (highest duration before sleep is 850ms, for housekeeping operation). It does not involve any action from host, however, for maximum power saving (lowest current), host clock to the memory device needs to be shut down. For most embedded systems, beside while host is accessing data, devices are always in sleep mode, for greater power saving efficiency. Whenever host is going to access storage device in sleep mode, any issued command will cause device to exit sleep and operation execution.

3.3 Sleep (CMD 5)

Memoright M1000 can switch between Sleep and Standby on SLEEP/AWAKE (CMD5) command. In Sleep state, device's power consumption is minimized and reacts only to RESET (CMD0) and SLEEP/AWAKE (CMD5) commands. any other command will be completely ignored.

The Vcc power supply may even be switched off in Sleep mode to allow further power saving.

For additional information please refer JESD84-A441 section number 7.6.15

3.4 Enhanced Write

In Memoright M1000 reliable write (defined in eMMC 4.41 spec 4) mode, original data pointed by a logical address will stay the same until the new data has been successfully overwritten. This ensures that the each write transaction will always be reliable and never leaves undefined data in given address. When using enhanced write, data will remain valid even in the case of power drop during programming.

3.5 Secure Erase

Memoright M1000 supports Security Mode Erase command. Once triggered, no command is allowed until Secure Erase is completed.

Memoright M1000 will sanitize the erase area with predefined pattern. The purge will overwrite addressable content with a given character and then erase the NAND flash.

This command meets specific defense or governmental requirements and guarantees Flash memory content can no longer be restored.

3.6 Secure Trim

Memoright M1000 Secure Trim is similar to the Secure Erase but performs a purge on write blocks (512 bytes) .

3.7 Trim

Trim function acts like an Erase but operate at block (512 B) level.

For additional information, refer to JEDEC JESD84-A441.

3.8 Partition

Memoright M1000 let the host split local memory into partitions with independent addressable space from logical address 0x00000000 for different use. Memory blocks are segmented as hereafter:

- Default factory setting defines two 2MB boot partitions, as enhanced storage media and an extra 256KB RPMB.

Host can set one segment in User Data Area as enhanced storage media (starting location and Write Protect Group size). This is one-time programmable and can NOT be changed once set.

Up to 4 General Purpose Area can be set as user data or sensitive data or other usage. Partition size must be a multiple of the write protect group. This is one-time programmable and can NOT be changed once set.

For additional information, refer to JEDEC JESD84-A441.

3.9 Write Protection

To prevent accidental data loss or overwrite, Memoright M1000 provides two levels of write protection:

- Write-protect the whole device (including the Boot Area Partitions, General Purpose Area Partition, and User/Enhanced User Data Area Partition) by setting the permanent or temporary write protect bits in the CSD.
- Write-protect specific segments permanently or temporarily write protected. Segment size can be defined in the EXT_CSD register.

For additional information, refer to JEDEC JESD84-A441.

3.10 Hardware Reset

Host may reset the device to pre-idle state and disable temporary write protection on related blocks.

For additional information, refer to JEDEC JESD84-A441.

3.11 Background Operations

In order to reduce latency for time critical operations, housekeeping operations (garbage collection, erase and compaction) are executed in the background.

Operations are classified into two types:

Foreground – such as read or write commands and

Background –executed when the device is not busy with host commands.

For additional information on Background Operations, refer to JESD84-A441 standard section 7.6.19

3.12 High Priority Interrupt (HPI)

If OS use on demand-paging to run user process, the host needs to fetch pages in the midst of other operation, so the query might be delayed until the completion of the command.

High priority interrupt (HPI) allows low read latency operation, by holding lower priority process before completion. This mechanism reduces latency, typically to less than 10 ms.

For additional information on the HPI function, refer to JESD84-A441 standard section 7.6.20

3.13 DDR interface

Memoright M1000 support DDR signaling to double bus performance.

For additional information please refer to JESD84-A441 standard.

4. Product Specifications

4.1 Power Consumption

Operation	Max Current High Voltage Range 2.7V-3.6V	Max Current Low Voltage Range 1.65V-1.95V
Sleep Mode	150 μ A	140 μ A
Read	60 mA	50 mA
Write	60 mA	50 mA

4.2 Performance

Max. Sequential Read (MB/s)	35
Max. Sequential Write (MB/s)	20

4.3 Temperature

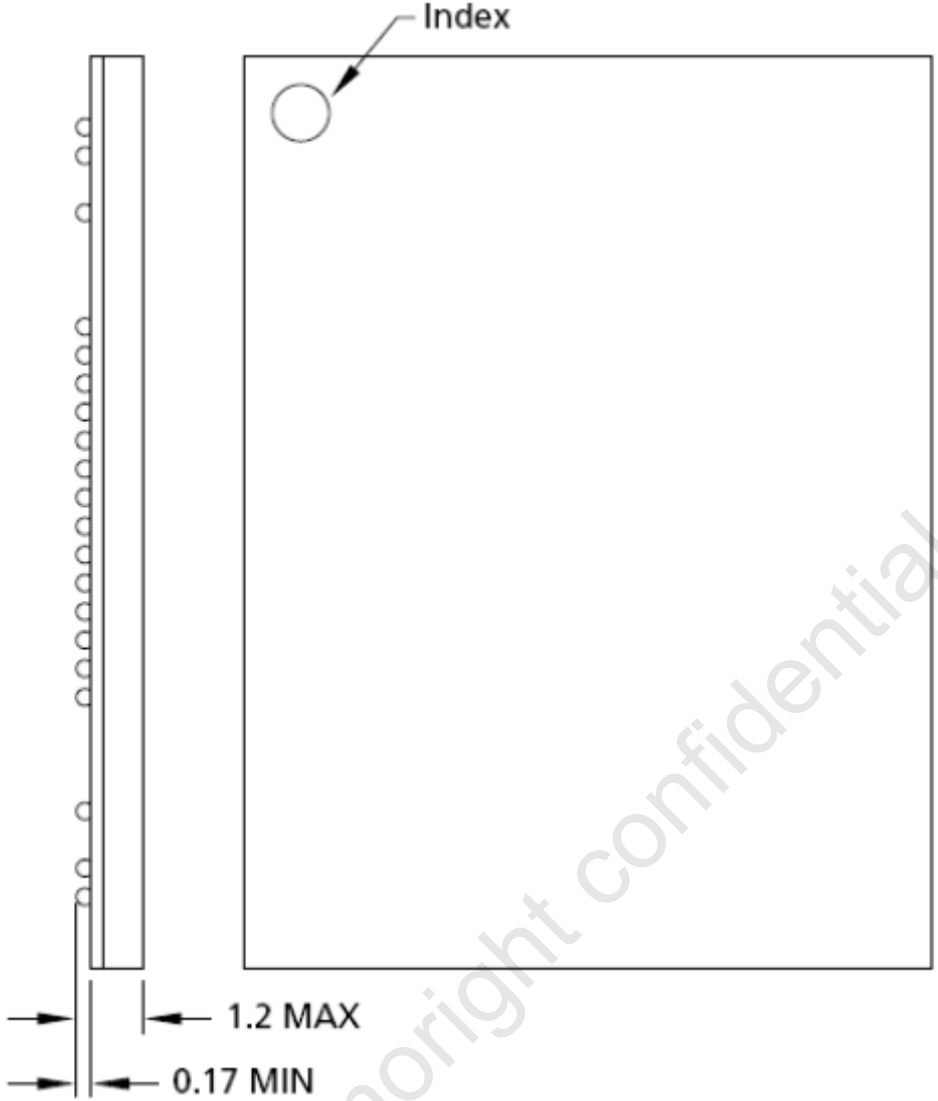
Operate: -20 C° ~ +85 C°

Storage: -40 C° ~ +85 C°

4.4 Humidity

The moisture sensitivity level for Memoright M1000 is MSL = 3.

5.2 Physical Dimension (Side/Front View)



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5.3 M1000 Ball Array

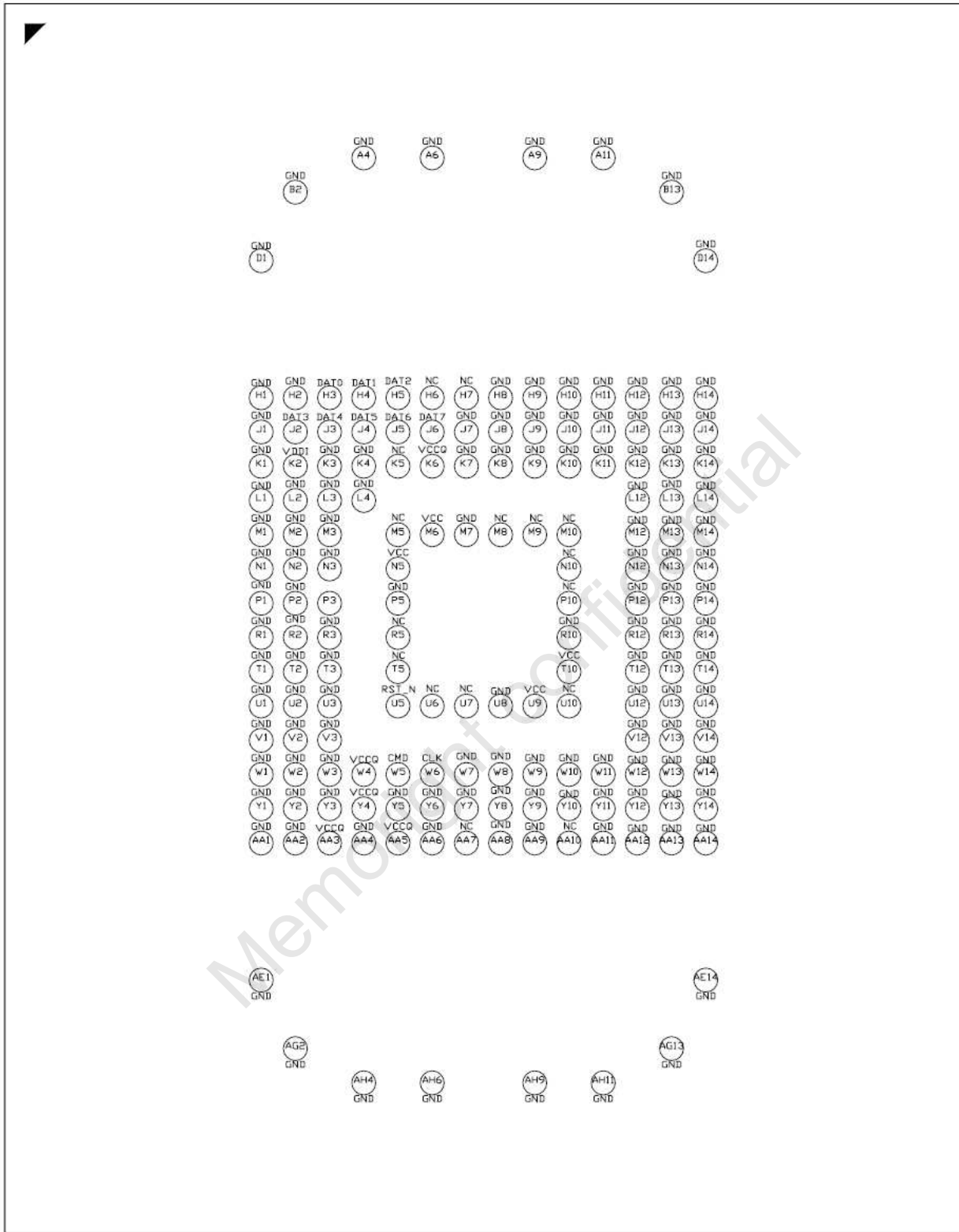


Fig 2. Memoright M1000 Series 169 pin Ball Array

5.4 Pin and Signal Definition

W6	CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines.
W5	CMD	Input	Command: A bidirectional channel used for device initialization and command transfers. Command has two operating modes: 1) Open-drain for initialization. 2) Push-pull for fast command transfer.
H3	DAT0	I/O	Data I/O0: Bidirectional channel used for data transfer.
H4	DAT1	I/O	Data I/O1: Bidirectional channel used for data transfer.
H5	DAT2	I/O	Data I/O2: Bidirectional channel used for data transfer.
J2	DAT3	I/O	Data I/O3: Bidirectional channel used for data transfer.
J3	DAT4	I/O	Data I/O4: Bidirectional channel used for data transfer.
J4	DAT5	I/O	Data I/O5: Bidirectional channel used for data transfer.
J5	DAT6	I/O	Data I/O6: Bidirectional channel used for data transfer.
J6	DAT7	I/O	Data I/O7: Bidirectional channel used for data transfer.
U5	RST_n	Input	Reset signal pin
M6, N5, T10, U9	VCC	Supply	Vcc: Flash memory I/F and Flash memory power supply.
K6, W4, Y4, AA3, AA5	VccQ	Supply	VccQ: Memory controller core and MMC interface I/O power supply.
M7, P5, R10, U8	VSS	Supply	Vss: Flash memory I/F and Flash memory ground connection.
K4, Y2, Y5, AA4, AA6	VssQ	Supply	VssQ: Memory controller core and MMC I/F ground connection.
K2	VDDi		VDDi: Connect 0.1μF capacitor from VDDi to ground.
L4	NC Index	—	Index: Can be connected to ground or left floating.
A4, A6, A9, A11, B2, B13, D1, D14, H1, H2, H8, H9, H10, H11, H12, H13, H14, J1, J7, J8, J9, J10, J11, J12, J13, J14, K1, K3, K7, K8, K9, K10, K11, K12, K13, K14, L1, L2, L3, L12, L13, L14, M1, M2, M3, M12,	NC	—	No connect: Can be connected to ground or left floating.

M13, M14, N1, N2, N3, N12, N13, N14, P1, P2, P12, P13, P14, R1, R2, R3, R12, R13, R14, T1, T2, T3, T12, T13, T14, U1, U2, U3, U12, U13, U14, V1, V2, V3, V12, V13, V14, W1, W2, W3, W7, W8, W9, W10, W11, W12, W13, W14, Y1, Y3, Y6, Y7, Y8, Y9, Y10, Y11, Y12, Y13, Y14, AA1, AA2, AA8, AA9, AA11, AA12, AA13, AA14, AE1, AE14, AG2, AG13, AH4, AH6, AH9, AH11			
H6, H7, K5, M5, M8,	RFU	—	Reserved for future use.
M9, M10, N10, P3,			Left it floating for future use.
P10, R5, T5, U6, U7,			
U10, AA7, AA10			

6. Marking

First Row: Memoright Logo

Second Row: Device Code Name

Third Row: Sales Item Part Number

Fourth Row: A-YYWWD-XX-X

A: Manufacture code

YY: Last two digit of year

WW: Work week

D: A day within the week

XX-X: Internal use only

Fifth Row: Country of origin i.e. "Taiwan"

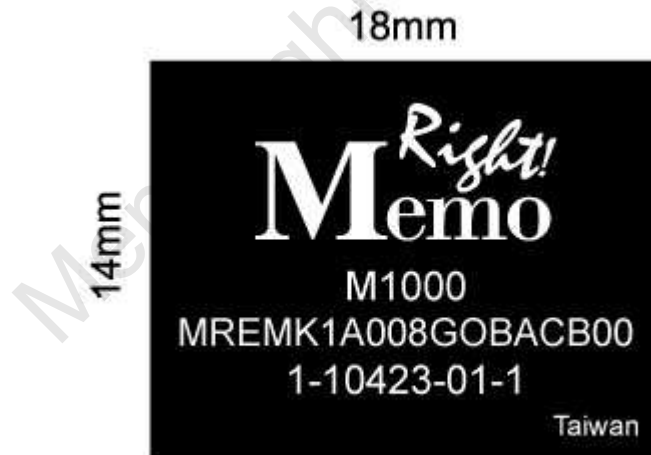


Fig 3. Example of M1000 32GB Marking

7. Ordering Information

Table 6. Ordering Information

Capacity	Part Number	Description
2GB	MREMK1A002GOCACB00	2 GB MLC ,M1000 e-MMC 4.41 embedded flash memory, 169 ball, BGA, 14mm x 18mm, B-temp solution.
4GB	MREMK1A004GOCACB00	4 GB MLC ,M1000 e-MMC 4.41 embedded flash memory, 169 ball, BGA, 14mm x 18mm, B-temp solution.
8GB	MREMK1A008GOBACB00	8 GB MLC ,M1000 e-MMC 4.41 embedded flash memory, 169 ball, BGA, 14mm x 18mm, B-temp solution.
16GB	MREMK1A016GOAACB00	16 GB MLC ,M1000 e-MMC 4.41 embedded flash memory, 169 ball, BGA, 14mm x 18mm, B-temp solution.
32GB	MREMK1A032GOAACB00	32 GB MLC ,M1000 e-MMC 4.41 embedded flash memory, 169 ball, BGA, 14mm x 18mm, B-temp solution.
64GB	MREMK1A064GOAACB00	64 GB MLC ,M1000 e-MMC 4.41 embedded flash memory, 169 ball, BGA, 14mm x 18mm, B-temp solution.

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