Memoright MSDR Series
Industrial Secure Digital Card

Model Code: MRSDE1A****B*S1*00

Product Specification

Version 1.02
May. 2012

Overview

This document serves as a reference basis for MSDR Series Industrial Secure Digital Card technical characteristics to help you to choose Memoright industrial operating temperature range SLC NAND Flash storage solution.

Ordering information

Decoder

| MR | SDE1A | **** | B* | S1 | * | 00 |

Memoright

Project code

Standard

Environmental Grade

I: Industrial Temperature (-40°C~+85 °C)
C: Commercial Temperature (0°C~+70 °C)

Capacity

128M: 128 MBytes

256M: 256 MBytes

512M: 512 Mbytes

001G: 1 GBytes

002G: 2 GBytes

Flash type

Samsung SLC

Form Factor

S1:   SD Card

                             May 2012
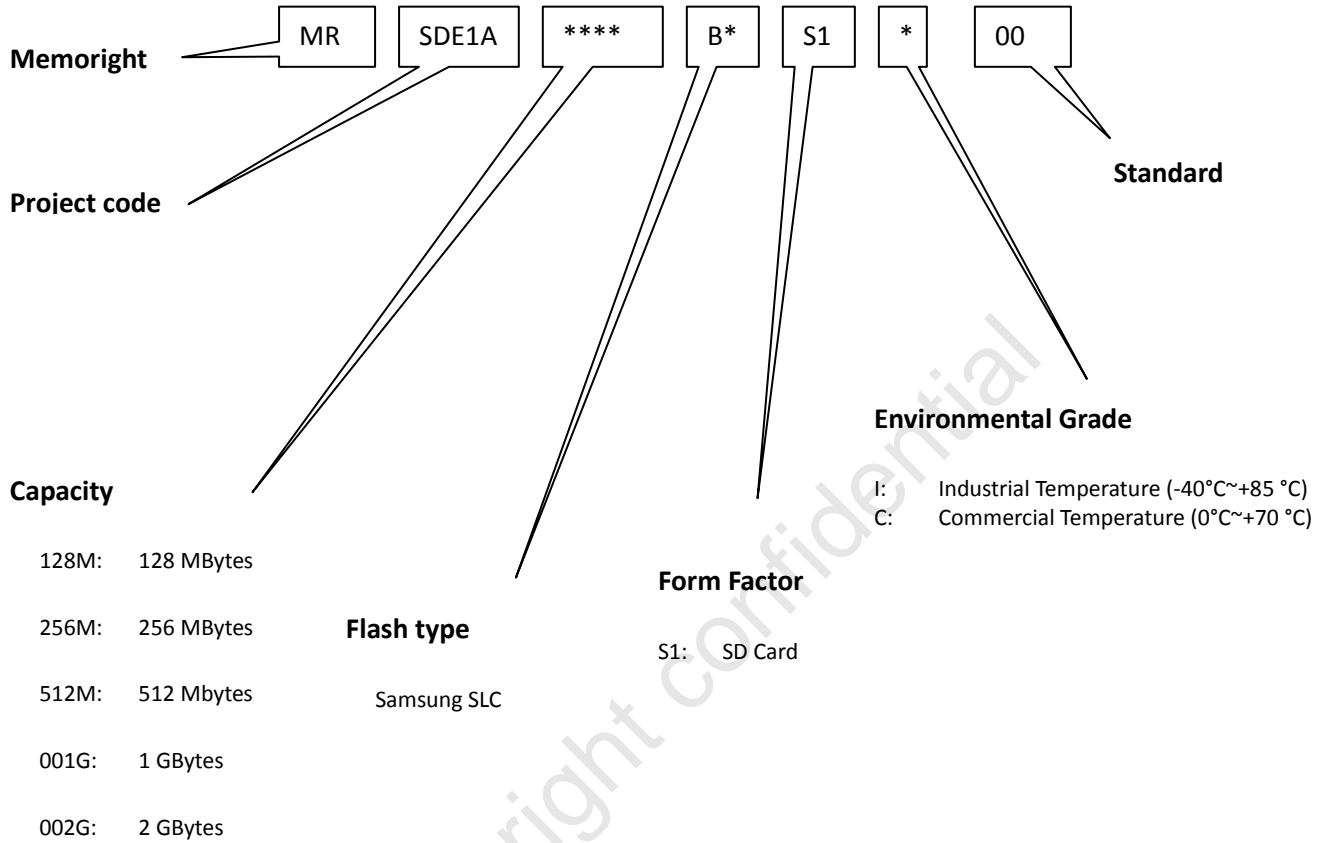
Product code

Memoright MSDR Series(I-Temp)	
Part Number	Description
MRSDE1A128MB2S1I00	128 MB, SLC, Secure Digital Card, Industrial Solution
MRSDE1A256MB4S1I00	256 MB, SLC, Secure Digital Card, Industrial Solution
MRSDE1A512MB6S1I00	512 MB, SLC, Secure Digital Card, Industrial Solution
MRSDE1A001GB8S1I00	1 GB, SLC, Secure Digital Card, Industrial Solution
MRSDE1A002GB0S1I00	2 GB, SLC, Secure Digital Card, Industrial Solution

Memoright MSDR Series(C-Temp)	
Part Number	Description
MRSDE1A128MB1S1C00	128 MB, SLC, Secure Digital Card, Commercial Solution
MRSDE1A256MB3S1C00	256 MB, SLC, Secure Digital Card, Commercial Solution
MRSDE1A512MB5S1C00	512 MB, SLC, Secure Digital Card, Commercial Solution
MRSDE1A001GB7S1C00	1 GB, SLC, Secure Digital Card, Commercial Solution
MRSDE1A002GB9S1C00	2 GB, SLC, Secure Digital Card, Commercial Solution

For the latest ordering information, please consult Memoright's sales representatives or check on our website: http://www.memoright.com

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General Description

Memoright MSDR Industrial Series, SD 3.0 compliant Secure Digital Card consists solely of semiconductor devices and durable SLC NAND Flash.

As MSDR Series Industrial SD Card is a power efficient solution in a slim form factor, will fit most demanding mobile, portable and ultra portable storage requirements. Memoright MSDR Series Class 10 SDHC high reliability and compatibility is suitable for industrial use under extreme environment for wide range applications, from digital camera to specialized IPC platforms.

1.1 Capacity
128, 256,512 Mbytes, 1 & 2 GBytes

1.2 Form Factor
SD Card: 24.00 x 32.00 x 2.10 mm

1.3 Compliance
Support SD specification 1.01/1.1/2.0/3.0
SDHC Class 2,4,6,10

1.4 Performance
(Single channel)
Sustained Read transfer: up to 15MB/s
Sustained Write transfer: up to 10MB/s

1.5 Reliability

1.5.1 Endurance
> 5 yrs sequential write (for one full drive's capacity write per day)
1.5.2 ECC
Hardware BCH ECC engine, with enhanced algorithm, which reduces error rate and enforces write endurance at same time.

1.5.3 Bad block management
Memoright MSDR has a certain number of reserved blocks. When a user data block fails, a reserved block will replace the failed block. The replacement of bad block is transparent to user.

1.5.4 Data Retention
Data retention : >10 years

1.6 Power consumption
Input voltage: DC +3.3V
Write :   <0.1W (typical)
Read :   <0.1W (typical)
Standby :   <0.3mW (typical)
Test under room temperature @ 3.3V

1.7 Environmental
1.7.1 Temperature range
Operating (I-Temp) : -40°C ~ +85°C
Operating (C-Temp) : 0°C ~ +70°C
Non-Operating: -55°C ~ +95°C (non condensing)

1.7.2 Physical stress

Drop: 1.5m free fall
Pull/Plug: 10000 items
Twisting: ±2.5°, 1min
Bending: 10N, 1min, 5 times:
Vibration: 10Hz~2000Hz, 2g, 5minutes
Shock: 50g, 11ms
Salt spray: 3%(5%) NaCl/35°C

Functional Block Diagram

Figure 1: MSDR Internal Block diagram
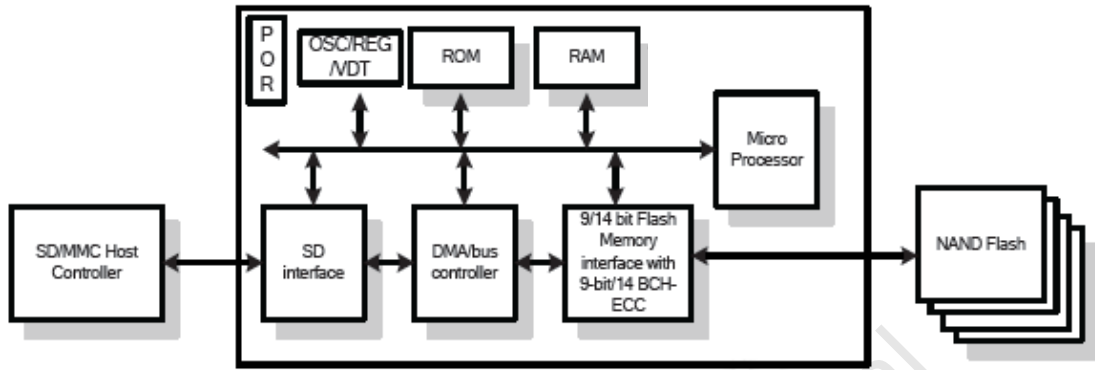
Figure 2: MSDR Application Block Diagram
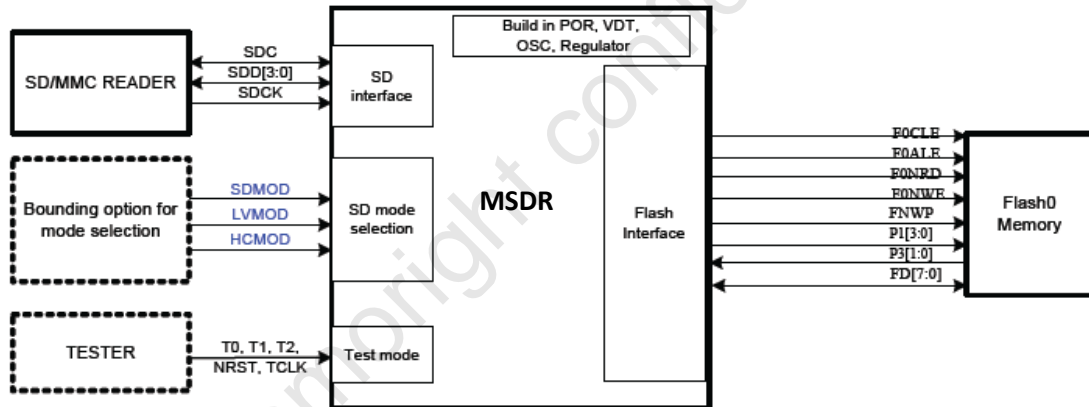
Physical specifications

Interface

Table 1: MSDR pin definition

Secure Digital Card Interface			
PIN NO	NAME	TYPE	DESCRIPTION
1	CD/DAT	I/O/PP3	Card Detect/Data Line [Bit3]
2	CMD	PP	Command / Response
3	VSS1	S	Supply voltage ground
4	VDD	S	Supply voltage
5	CLK	I	Clock
6	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit0]
8	DAT1	I/O/PP	Data Line [Bit1]
9	DAT2	I/O/PP	Data Line [Bit2]

Figure 3: MSDR 9 pins connector
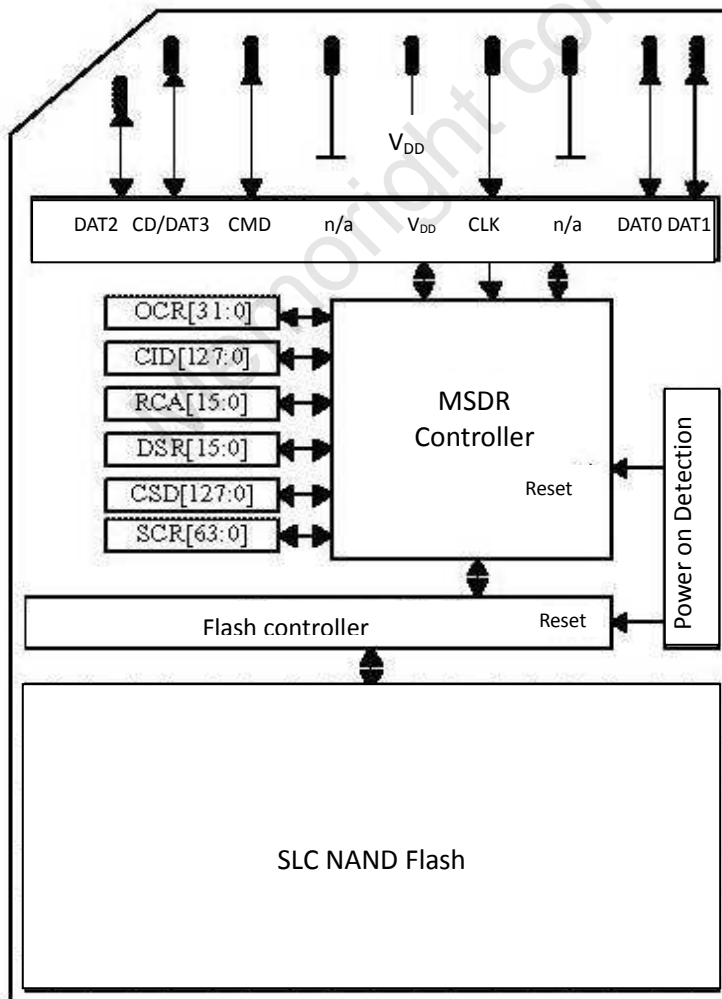
Pin Description

Flash Interface

Table 2: Flash interface

Signal name	Type	Description
FD[7:0]	I/O	Flash interface data bus, direct connect to the flash memory.
FCLE	O	Flash0 interface command latch enable, direct connect to the flash memory.
FALE	O	Flash0 interface address latch enable, direct connect to the flash memory.
FNRD	O	Flash0 interface read strobe control, direct connect to the flash memory.
FNWE	O	Flash0 interface write strobe control, direct connect to the flash memory.
FNWP	O	Flash interface write protection, direct connect to the flash memory.
P3[1:0]	I	Used as busy signal from flash memory.
P1[3:0]	O	Used as flash chip select signal. Max. 4 flash chips can connect to SM2681BB
VCCIO1	Power in	Power supply for flash group I/O pad.

SD Interface

Table 3: SD Interface

Signal name	Type	Description
SDC	I/O	SD interface command line
SDD[3:0]	I/O	SD interface data line
SDCK	I	SD interface synchronous clock input
VCCIO2	Power in	Power supply for SD group I/O pad.

Mechanical characteristics

Table 4: MSDR mechanical dimension

Length	32 mm ± 0.1 mm
Width	24 mm ± 0.1 mm
Thickness	2.1 mm ± 0.15 mm

Figure 4: MSDR blueprint
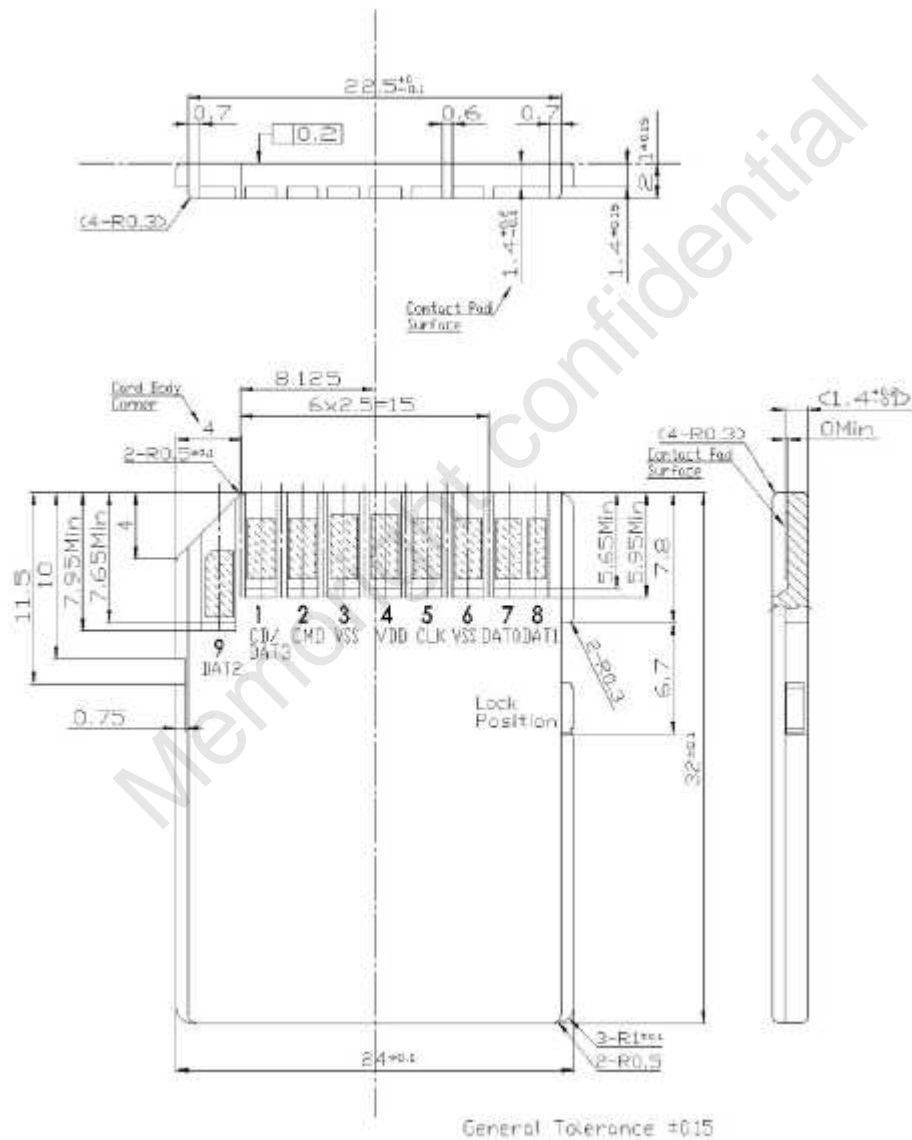
Environmental Specification

Temperature

Table 5: Environmental specification

Temperature	Industrial	-40°C to 85°C
	Commercial	0°C to 70°C
	Non-Operating	-55°C to 95°C (I-temp)
		-40°C to 85°C (C-temp)
Humidity	Operating	8%~95% non condensing
	Non-Operating	

Physical test

Table 6: Physical test

Drop	1.5m free fall
Pull/Plug	10000 items
Twisting	±2.5°, 1min
Bending	10N, 1min, 5 times:
Vibration	10Hz~2000Hz, 2g, cycle time: 5minutes
Shock	50g, 11ms
Salt spray	3%(5%) NaCl/35°C

Reliability

Number of insertions	10,000 minimum
Endurance	> 5 yrs sequential write (for one full drive's capacity write per day)
MTBF @ 25°C	>4,000,000 hours

Regulation

FCC	Federal Communications Commission Rules and Regulations
CE	European Community Directive
RoHS	Restriction of Hazardous Substance Directive

Device Electrical Characteristics

General DC Characteristics

Table 7: DC Characteristics

Symbol	Parameter	Min	Typical	Max	Unit
	Peak voltage on all lines	-0.3		3.6	V
	All input leakage current	-10		10	uA
	All output leakage current	-10		10	uA
VDDL	Supply voltage for low voltage range	1.7		1.95	V
VDDH	Supply voltage for high voltage range	2.7		3.6	V
	Supply voltage differential	-0.5		0.5	V

Bus Signal

Table 8: Bus Signal Line Loading

Symbol	Parameter	Min	Typical	Max	Unit
R$_{CMD}$	Pull up resistance for SDC line	10		100	K Ohm
R$_{DAT}$	Pull up resistance for SDD line	10		100	K Ohm
C$_L$	Total Bus capacitance for each signal line			40	pF
	Signal line inductance			16	nH
R$_{DAT3}$	Pull-up resistance inside card	10		90	K Ohm

Figure 5: Bus Signal Level
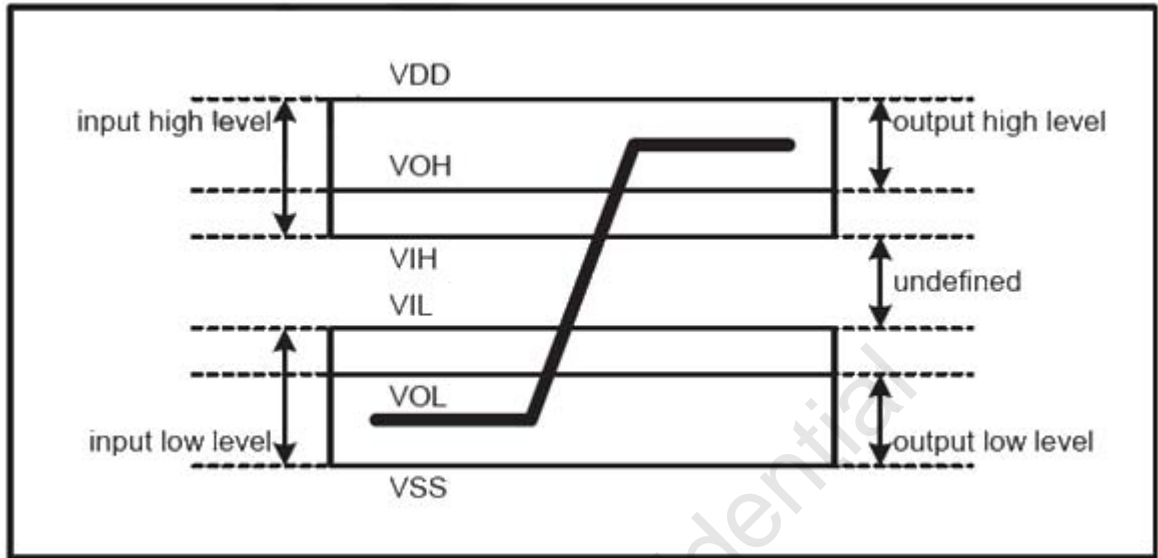
Table 9: Bus Signal Level

Symbol	Parameter	Min	Typical	Max	Unit
V_{OH}	Output High voltage (V_{DD} = 3.3V)	2.4			V
V_{OL}	Output Low voltage (V_{DD} = 3.3V)			0.4	V
V_{IH}	Input High voltage (V_{DD} = 3.3V)	2.0		3.6	V
V_{IL}	Input Low voltage (V_{DD} = 3.3V)	-0.3		0.8	V
V_{OH}	Output High voltage (V_{DD} = 1.8V)	1.6			V
V_{OL}	Output Low voltage (V_{DD} = 1.8V)			0.2	V
V_{IH}	Input High voltage (V_{DD} = 1.8V)	1.26		2.1	V
V_{IL}	Input Low voltage (V_{DD} = 1.8V)	-0.3		0.54	V

Bus Timing   (High-Speed Mode)

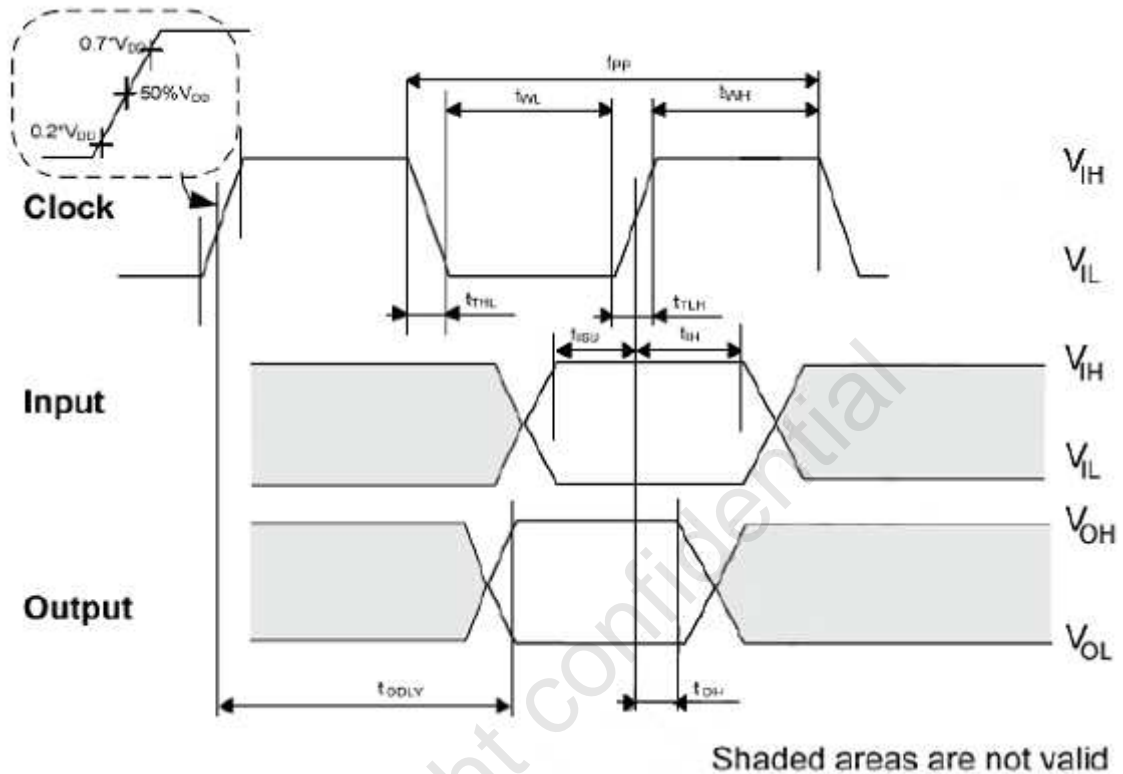Figure 6: Timing diagram data input/output referenced to clock (High-Speed)

Table- 1 High Speed Mode Timing

Table 10: Bus Timing (High Speed)

Symbol	Parameter	Min	Typical	Max	Unit
Input SDCK					
f_{PP}	Clock frequency data transfer mode	0		50	MHz
t_{WL} / t_{WH}	Clock low time / Clock high time	7			ns
t_{TLH} / t_{THL}	Clock rise time / Clock fall time			3	ns
Input SDD/SDC, reference to SDCK					
t_{ISU}	Input set-up time	6		0.2	ns
t_{IH}	Input hold time	2		2.1	ns
Output SDD/SDC, reference to SDCK					
t_{ODLY}	Output delay time during Data Transfer Mode			14	ns
t_{OH}	Output hold time	2.5			ns
C_L	Total System capacitance for each line			40	pF

(1)   All timing values are measured relative to 50% of voltage level.

(2)   Rise and fall times are measured from 10% - 90% of voltage level.

Bus Timing (Default)

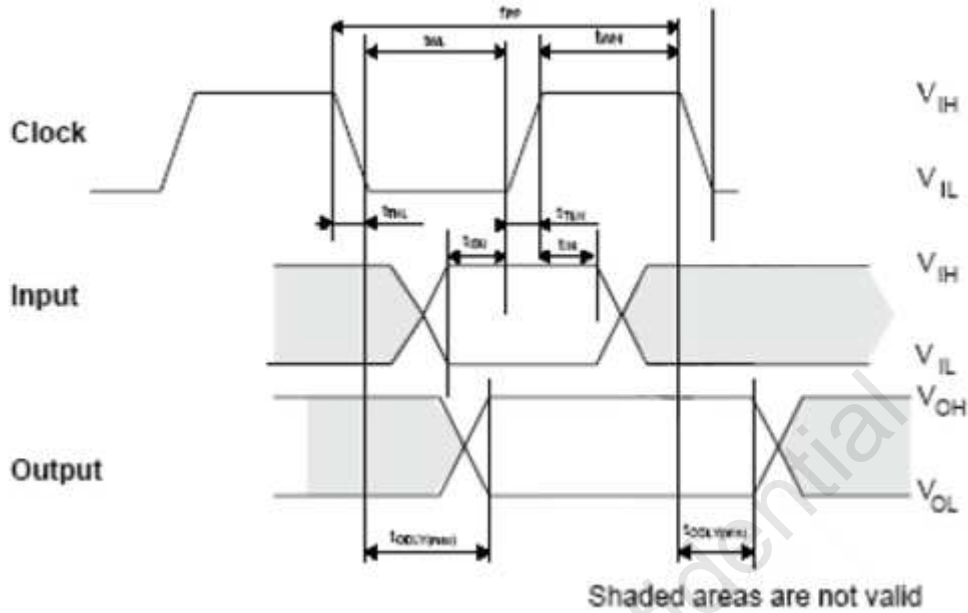Figure 7: Timing diagram data input/output referenced to clock (Default)

Shaded areas are not valid

Table 11: Low Speed Mode Timing (Backward compatible)

Symbol	Parameter	Min	Typical	Max	Unit
Input SDCK					
f_{PP}	Clock frequency data transfer mode	0		25	MHz
t_{WL} / t_{WH}	Clock low time / Clock high time	10			ns
f_{OD}	Clock frequency identification mode	0		400	KHz
t_{TLH} / t_{THL}	Clock rise time / Clock fall time			10	ns
Input SDD/SDC, reference to SDCK					
t_{ISU}	Input set-up time	5			ns
t_{IH}	Input hold time	5			ns
Output SDD/SDC, reference to SDCK					
t_{ODLY}	Output delay time during Data Transfer Mode			14	ns
C_L	Total System capacitance for each line			50	pF

(1)   All timing values are measured relative to 50% of voltage level.

(2) Clock Rise and fall times are measured from V_{IH} to V_{IL} of voltage level.

Flash Interface AC Characteristic

Table 12: Flash Interface AC Characteristic

Symbol	Parameter	Min	Typical	Max	Unit
tCLS	CLE SETUP TIME	27.5			ns
tCLH	CLE Hold Time	12.4			ns
tALS	ALE Setup Time	25			ns
tALH	ALE Hold Time	10			ns
tWP	WE Pulse Width	15			ns
tDS	Data Setup Time	25			ns
tDH	Data Hold Time	12.5			ns
tWC	Write Cycle Time	37.5			ns
tWH	WE High Hold Time	20			ns
tRC	Read Cycle Time	37.5			ns
tRP	RE pulse Width	17.5			ns
tREH	RE High Hold Time	20			ns

Command Latch Cycle

Figure- 1 Command Latch Cycle (Start)
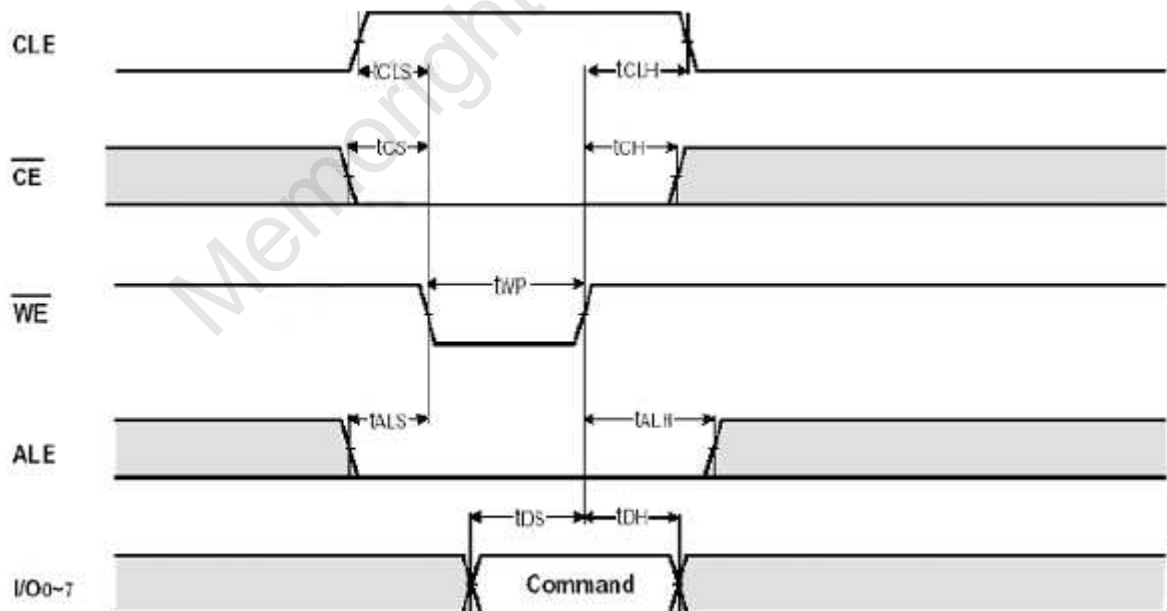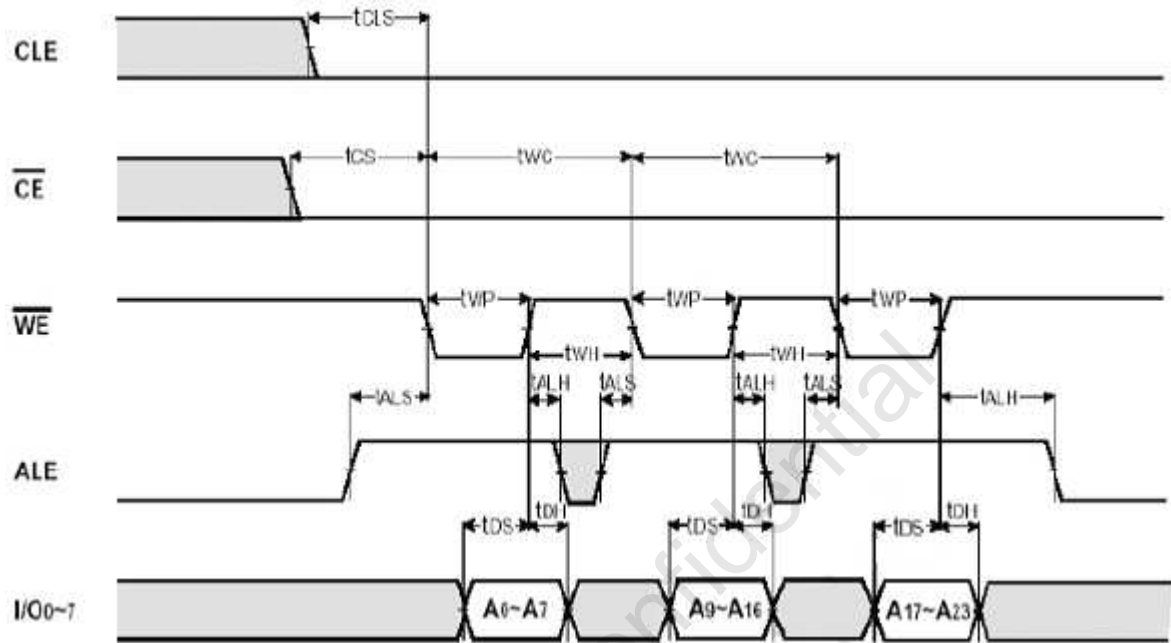
Figure- 2   Command Latch Cycle (End)

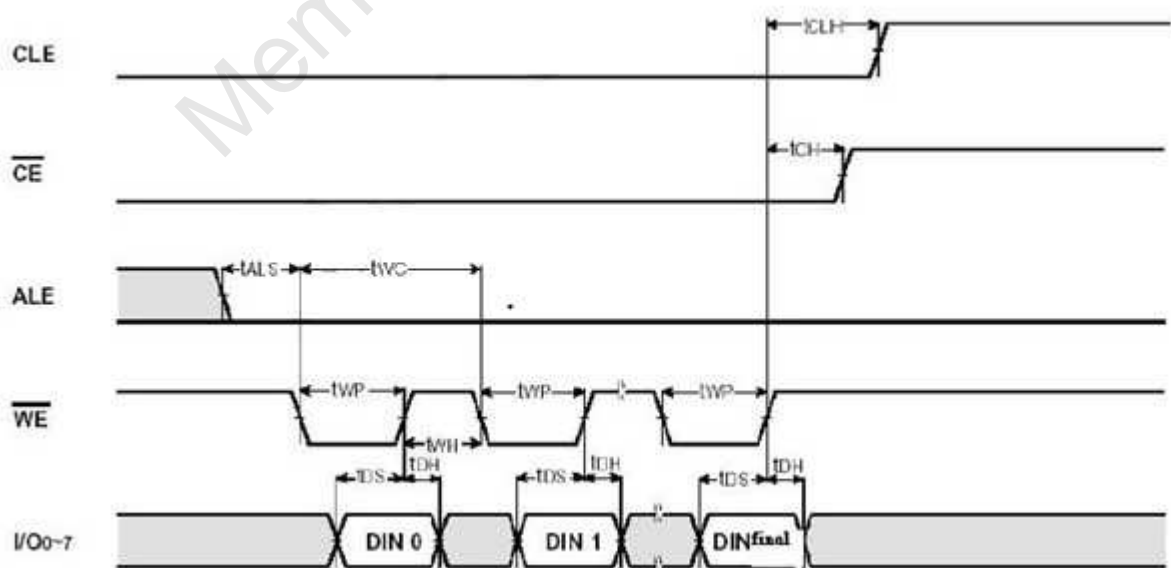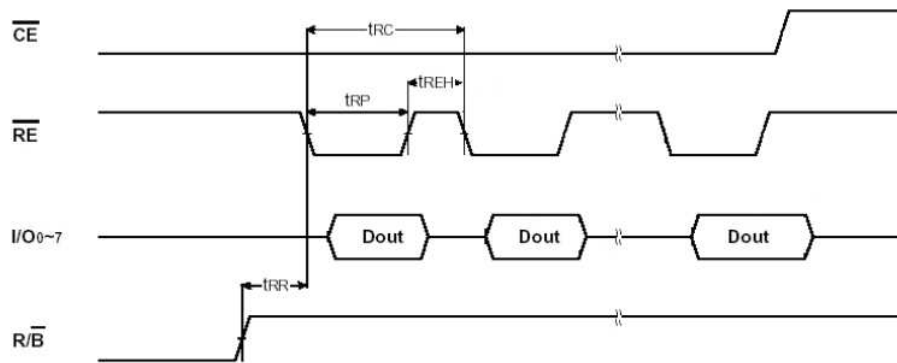Figure- 3   Input Data Latch Cycle

Figure- 4   Sequential Out Cycle after Read (CLE=L, /WE=H, ALE=L)

Power Consumption

Table 13: Power Consumption

Symbol	Parameter	Min	Typical	Max	Unit
	Read current at 3.3V		28	35	mA
	Write current at 3.3V		28	35	mA
	Pre-initialization standby current at 3.3V		80	100	uA
	Post-initialization standby current at 3.3V		80	100	uA

Sales and technical support

For data sheet, documentation, customization for specific application and technical support, please contact Memoright SSD Design Center

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