DATA SHEET

SILICONDRIVE II CF
SSD-Cxxx(I)-4000

OVERVIEW

The SiliconDrive II CF is an optimal time-to-market replacement for hard drives and flash cards or in host systems that require low power and scalable storage solutions.

SiliconDrive II technology is engineered exclusively for the high performance, high reliability and multi-year product lifecycle requirements of the Enterprise System OEM market. Typical end-market applications include broadband data and voice networks, military systems, flight system avionics, medical equipment, industrial control systems, video surveillance, storage networking, VoIP, wireless infrastructure, and interactive kiosks.

Every SiliconDrive II CF is integrated with SiliconSystems patented PowerArmor and patent-pending SiSMART and SiSecure technologies.

PowerArmor prevents data corruption and loss from power disturbances by integrating patented technology into every SiliconDrive II.

SiSMART acts as an early warning system to eliminate unscheduled downtime by constantly monitoring and reporting the exact amount of remaining storage system useful life.

SiSecure is a comprehensive suite of user-selectable security technologies that solves the critical need for robust storage security for embedded systems applications that have a small footprint and low-power requirement.

SISECURE

SiZone	Data zones with different security parameters.
SiKey	Ties SiliconDrive to a specific host and/or software IP.
SiProtect	Protection software for password-required, read/write, or read-only access.
SiSweep	Ultra-fast data erasure.
SiPurge	Non-recoverable data erasure.
AutoLock	Automatically locks the SiliconDrive.

FEATURES

- RoHS 6 of 6 compliant
- Integrated PowerArmor, SiSMART, and SiSecure technology
- Capacity range: 1GB to 16GB
- Supports both 8-bit and 16-bit data register transfers
- Supports dual-voltage 3.3V or 5V interface
- MTBF >4,000,000 hours
- ATA-5 compliant
- Industry standard Type I CF form factor
- Supports PIO modes 0-6, multi-word DMA 0-4, and UDMA modes 0-4

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REVISION HISTORY

Document No.	Release Date	Changes
4000C-12DSR	June 13, 2008	**Updated:** • PIO mode. • Read and Write (Typical/Peak) in the “System Power Requirements” table. • 16GB & 32GB in the "Product Capacity Specifications" table. • “Pin Assignments” table. • “Signal Descriptions” table. • "Absolute Maximum Ratings" table." • "Capacitance" table. • "DC Characteristics" table. • "Attribute and Common Memory Read Timing" table. • "Attribute and Common Memory Write Timing" table. • "I/O Access Read Timing" table. • "I/O Access Write Timing" table. • "True IDE Read/Write Access Timing" table. • "True IDE Multiword DMA Read/Write Access Timing" table. • “Identify Drive — Drive Attribute Data” table. **Added:** • “Ultra DMA Data Burst Timing Requirements.” **Removed:** • “Capacitance.”
4000C-11DSR PRELIMINARY	May 7, 2008	Updated “Overview.”
SSDS10-4000C-R PRELIMINARY	April 3, 2008	Updated part pictures.

Document No.	Release Date	Changes
SSDS09-4000C-R PRELIMINARY	March 20, 2008	**Updated:** • “Overview.” • “Features.” • SiProtect in the “SiSecure” and “Related Documentation” tables. • Read and Write Transfer rates in the “System Performance” table. **Added:** • SiSecure verbiage. • “MTBF.” **Removed:** • SiSecure rows from the “SiSecure” and “Related Documentation” tables. • “System Reliability.”
SSDS08-4000C-R PRELIMINARY	February 8, 2008	**Updated:** • Document’s title. • 16GB cylinder value in the “Product Capacity Specifications” table. **Added:** • “SiliconDrive II Secure” to the cover, which includes AutoLock. **Removed:** • The Note under the “Product Capacity Specifications” table.
SSDS07-4000C-R PRELIMINARY	January 29, 2008	Added a Note below the “DC Characteristics” table.
SSDS06-4000C-R PRELIMINARY	December 21, 2007	Updated the Endurance in the “System Reliability” table.
SSDS05-4000C-R PRELIMINARY	December 19, 2007	**Updated:** • Capacity range. • Transfer Rates in the “System Performance” table. • “Product Capacity Specifications” table. **Removed:** • Endurance from the “System Reliability” table.

Document No.	Release Date	Changes
SSDS04-4000C-R PRELIMINARY	December 17, 2007	Updated the t_{RWD} Maximum in the “True IDE Multiword DMA Read/Write Access Timing” table.
SSDS03-4000C-R PRELIMINARY	August 16, 2007	**Updated:** • RoHS information. • Cylinder Low in the “Task File Register Specification” table. • "Part Numbering Nomenclature" table. • “Sample Label.”
SSDS02-4000C-R PRELIMINARY	May 10, 2007	**Updated:** • Capacity range. • “System Performance” table. • “Related Documentation” table. **Removed:** • NOP command from the "ATA Command Set" table.
SSDS01-4000C-PRELIMINARY	April 10, 2007	Updated the capacity range.
SSDS00-4000C-R PRELIMINARY	February 27, 2007	Initial release.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

PHYSICAL SPECIFICATIONS

The SiliconDrive II CF products are offered in an industry-standard Type I form factor. See "Part Numbering" on page 110 for details regarding CF capacities.

PHYSICAL DIMENSIONS

This section provides diagrams that describe the physical dimensions for the CF.

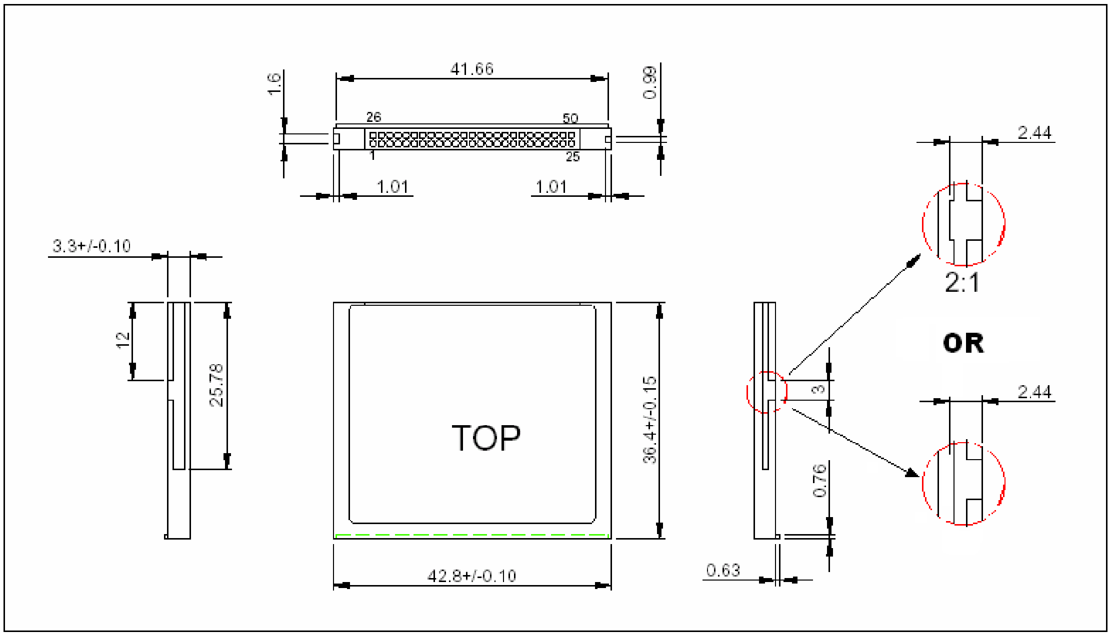

Figure 1: Physical Dimensions

PRODUCT SPECIFICATIONS

Note: All SiliconDrive II CF values quoted are typical at 25°C and nominal supply voltage.

SYSTEM PERFORMANCE

Table 1: System Performance

Reset to Ready Startup Time (Typical/Maximum)	200ms/400ms
Read Transfer Rate (Typical)	34MBps
Write Transfer Rate (Typical)	19MBps
Burst Transfer Rate	66MBps
Controller Overhead (Command to DRQ)	2ms (maximum)

SYSTEM POWER REQUIREMENTS

Table 2: System Power Requirements

DC Input Voltage	3.3 ± 10%	5.0 ± 10%
Sleep (Standby Current)	<0.5mA	<1.0mA
Read (Typical/Peak)	50mA/100mA	60mA/120mA
Write (Typical/Peak)	50mA/100mA	60mA/120mA

MTBF

Table 3: MTBF

MTBF (@ 25ºC)	>4,000,000 hours

PRODUCT CAPACITY SPECIFICATIONS

Table 4: Product Capacity Specifications

Product Capacity	Formatted Capacity (Bytes)	Number of Sectors	Number of Cylinders	Number of Heads	Number of Sectors/ Track
1GB	1,024,966,656	2,001,888	1986	16	63
2GB	2,048,901,120	4,001,760	3970	16	63
4GB	4,110,188,544	8,027,712	7964	16	63
8GB	8,195,604,480	16,007,040	15,880	16	63
16GB	16,391,208,960	32,014,080	16,383	16	63

ENVIRONMENTAL SPECIFICATIONS

Table 5: Environmental Specifications

Temperature	0ºC to 70ºC (Commercial) -40ºC to 85ºC (Industrial)
Humidity	8% to 95% non-condensing
Vibration	16.3gRMS, MIL-STD-810F, Method 514.5, Procedure I, Category 24
Shock	1000G, Half-sine, 0.5ms Duration 50g Pk, MIL-STD-810F, Method 516.5, Procedure I
Altitude	80,000ft, MIL-STD-810F, Method 500.4, Procedure II

ELECTRICAL SPECIFICATION

PIN ASSIGNMENTS

The following table describes the SiliconDrive II CF 50-pin IDE connector signals.

Table 6: Pin Assignments

Pin	PC Card Memory Mode	PC Card I/O Mode	IDE-ATA Mode	Ultra DMA Mode	Pin	PC Card Memory Mode	PC Card I/O Mode	IDE-ATA Mode	Ultra DMA Mode
1	GND	GND	GND	GND	26	CD1#	CD1#	CD1#	CD#1
2	D3	D3	D3	D3	27	D11[1]	D11[1]	D11[1]	D11[1]
3	D4	D4	D4	D4	28	D12[1]	D12[1]	D12[1]	D12[1]
4	D5	D5	D5	D5	29	D13[1]	D13[1]	D13[1]	D13[1]
5	D6	D6	D6	D6	30	D14[1]	D14[1]	D14[1]	D14[1]
6	D7	D7	D7	D7	31	D15[1]	D15[1]	D15[1]	D15[1]
7	CE1#	CE1#	CS0#	CS0#	32	CE2#	CE2#	CS1#	CS1#
8	A10	A10	A10	A10	33	VS1#	VS1#	VS1#	VS1#
9	OE#	OE#	ATA-SEL#	ATA-SEL#	34	IORD#	IORD#	IORD#	HSTROBE HDMARDY#
10	A9	A9	A9	A9	35	IOWR#	IOWR#	IOWR#	STOP
11	A8	A8	A8	A8	36	WE#	WE#	WE#	WE#
12	A7	A7	A7	A7	37	RDY/BSY	IREQ#	INTRQ	INTRQ
13	V_{CC}	V_{CC}	V_{CC}	V_{CC}	38	V_{CC}	V_{CC}	V_{CC}	V_{CC}
14	A6	A6	A6	A6	39	CSEL#	CSEL#	CSEL#	CSEL#
15	A5	A5	A5	A5	40	VS2#	VS2#	VS2#	VS2#
16	A4	A4	A4	A4	41	RESET#	RESET	RESET#	RESET#
17	A3	A3	A3	A3	42	WAIT#	WAIT#	WAIT#	DDMARDY# DSTROBE
18	A2	A2	A2	A2	43	INPACK#	INPACK#	DMARQ	DMARQ#
19	A1	A1	A1	A1	44	REG#	REG#	DMACK#	DMACK#
20	A0	A0	A0	A0	45	BVD2	SPKR#	DASP#	DASP#
21	D0	D0	D0	D0	46	BVD1	STSCHG#	PDIAG#	PDIAG#
22	D1	D1	D1	D1	47	D8[1]	D8[1]	D8[1]	D8[1]
23	D2	D2	D2	D2	48	D9[1]	D9[1]	D9[1]	D9[1]
24	WP	IOIS16#	IOCS16#	IOCS16#	49	D10[1]	D10[1]	D10[1]	D10[1]
25	CD2#	CD2#	CD2#	CD2#	50	GND	GND	GND	GND

Note:

1 = These signals are required only for 16-bit access, and not required when installed in 8-bit systems.

SIGNAL DESCRIPTIONS

Table 7: Signal Descriptions

Signal Name	Pin	Type	Description
A10-A0	8, 10, 11, 12, 14, 15, 16, 17, 18, 19, 20	I	These address lines along with the -REG signal are used to select the following: • The I/O port address registers within the SiliconDrive II CF • The memory-mapped port address registers within the SiliconDrive II CF • A byte in the card's information structure and its configuration control and status registers
A10-A0 (PC Card I/O mode)			This signal is the same as the PC Card Memory Mode signal.
A2-A0 (True IDE mode)	18, 19, 20	I	In true IDE mode, only A[2:0] are used to select the one of eight registers in the Task File. The remaining address lines should be grounded by the host.
BVD1 (PC Card memory mode)	46	I/O	This signal is asserted high, because BVD1 is not supported.
-STSCHG (PC Card I/O mode)			This signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states while the I/O interface is configured. This signal’s use is controlled by the Card Configuration and Status register.
-PDIAG (True IDE mode)			In the true IDE mode, this input/ output is the Pass Diagnostic signal in the Master/Slave handshake protocol.

Table 7: Signal Descriptions (Continued)

Signal Name	Pin	Type	Description
BVD2 (PC Card memory mode)	45	I/O	This signal is asserted high, as BVD2 is not supported.
-SPKR (PC Card I/O mode)			This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated.
-DASP (True IDE mode)			In the true IDE mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card memory mode)	26, 25	O	These Card Detect pins are connected to ground on the SiliconDrive II CF, and are used by the host to determine that the SiliconDrive II CF is fully inserted into its socket.
-CD1, -CD2 (PC Card I/O Mode)			This signal is the same for all modes.
-CD1, -CD2 (True IDE mode)			This signal is the same for all modes.

Table 7: Signal Descriptions (Continued)

Signal Name	Pin	Type	Description
-CE1, -CE2 (PC Card memory mode) Card Enable	7, 32	I	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. • -CE2 always accesses the odd byte of the word. • -CE1 accesses the even byte or the odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, and -CE2 allows 8-bit hosts to access all data on D0-D7. See "Attribute Memory Read Operations" on page 37, "Attribute Memory Write Operations" on page 38, "Common Memory Read Operations" on page 55, and "Common Memory Write Operations" on page 55.
-CE1, -CE2 (PC Card I/O mode) Card Enable			This signal is the same as the PC Card Memory Mode signal. See "I/O Space Read Operations" on page 56 and "I/O Space Write Operations" on page 56.
-CS0, -CS1 (True IDE mode)			In the true IDE mode, -CS0 is the chip select for the task file registers while -CS1 is used to select the Alternate Status register and the Device Control register.
-CSEL (PC Card memory mode)	39	I	This signal is not used for this mode.
-CSEL (PC Card I/O mode)			This signal is not used for this mode.

Table 7: Signal Descriptions (Continued)

Signal Name	Pin	Type	Description
-CSEL (True IDE mode)			This internally pulled-up signal is used to configure this device as a master or slave when configured in the true IDE mode. When this pin is: • Grounded, this device is configured as a master. • Open, this device is configured as a slave.
-INPACK (PC Card memory mode)	43	O	This signal is not used in this mode.
-INPACK (PC Card I/O mode) Input Acknowledge			This signal is asserted by the SiliconDrive II CF when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enabling of any input data buffers between the SiliconDrive II CF and the CPU.

Table 7: Signal Descriptions (Continued)

Signal Name	Pin	Type	Description
-DMARQ (UDMA Protocol active)			This signal is a DMA request that is used for DMA data transfers between host and device. It is asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by -IORD and -IOWR. This signal is used in a handshake manner with -DMACK (i.e., the device waits until the host asserts (-)DMACK before negating (-)DMARQ, and reasserting (-)DMARQ if there is more data to transfer). In PCMCIA I/O mode, the -DMARQ is ignored by the host while the host is performing an I/O Read cycle to the device. The host does not initiate an I/O Read cycle while -DMARQ is asserted by the device. In True IDE mode, DMARQ is not driven when the device is not selected in the Drive-Head register. While a DMA operation is in progress, -CS0 (-CE1) and -CS1 (-CE2) are held negated and the width of the transfers is 16 bits. If there is no hardware support for True IDE DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers do not attempt DMA mode operation.

Table 7: Signal Descriptions (Continued)

Signal Name	Pin	Type	Description
DMARQ (True IDE mode)	43	O	In true IDE mode, this signal is used for DMA transfers between the host and device. DMARQ is asserted by the device when the device is ready to transfer data to/from the host. The direction of data transfer is controlled by -IORD and -IOWR. This signal is used in a handshake manner with -DMACK (i.e., the device waits until the host asserts -DMACK before negating DMARQ, and reasserts DMARQ if there is more data to transfer). The DMARQ/-DMACK handshake is used to provide flow control during the transfer.
D15-D00 (PC Card memory mode)	31, 30, 29, 28, 27, 49, 48, 47, 6, 5, 4, 3, 2, 23, 22, 21	I/O	These lines carry the data, commands, and status information between the host and the controller. • D00 is the LSB of the word's even byte. • D08 is the LSB of the word's odd byte.
D15-D00 (PC Card I/O mode)			This signal is the same as the PC Card Memory Mode signal.
D15-D00 (True IDE mode)			In true IDE mode, all Task File operations occur in byte mode on the low-order bus D00-D07, while all data transfers are 16 bits using D00-D15.
GND (PC Card memory mode)	1, 50	-	Ground.
GND (PC Card I/O mode)			This signal is the same for all modes.
GND (True IDE mode)			This signal is the same for all modes.

Table 7: Signal Descriptions (Continued)

Signal Name	Pin	Type	Description
-IORD (PC Card memory mode)	34	I	This signal is not used in this mode.
-IORD (PC Card I/O mode)			This is an I/O read strobe generated by the host. This signal gates I/O data onto the bus from the SiliconDrive II CF when the card is configured to use the I/O interface.
-IORD (True IDE mode)			In true IDE mode, this signal has the same function as the PC Card I/O mode.
-HDMARDY (UDMA read protocol active)			When UDMA mode DMA read is active in all modes, this signal is asserted by the host to indicate that the host is ready to receive UDMA data-in bursts. The host may negate -HDMARDY to pause a UDMA transfer.
HDSTROBE (UDMA write protocol active)			When UDMA mode DMA write is active in all modes, this signal is the data out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause a UDMA data-out burst.
-IOWR (PC Card memory mode)	35	I	This signal is not used in this mode.
-IOWR (PC Card I/O mode)			The I/O write strobe pulse is used to clock I/O data on the Card data bus into the SiliconDrive II CF controller registers when the SiliconDrive II CF is configured to use the I/O interface. The clocking occurs on the negative-to-positive edge of the signal (the trailing edge).

Table 7: Signal Descriptions (Continued)

Signal Name	Pin	Type	Description
-IOWR (True IDE mode)			In true IDE mode, this signal has the same function as the PC Card I/O mode.
STOP (UDMA protocol active)			In all modes, while the UDMA mode protocol is active, the assertion of this signal causes the termination of the UDMA data burst.
-OE (PC Card memory mode)	9	I	This is an output enable strobe generated by the host interface, which is used to read: • Data from the SiliconDrive II CF in memory mode. • The CIS and configuration registers.
-OE (PC Card I/O mode)			In PC Card I/O mode, this signal is used to read the CIS and configuration registers.
-ATA SEL (True IDE mode)			To enable true IDE mode, this input should be grounded by the host.

Table 7: Signal Descriptions (Continued)

Signal Name	Pin	Type	Description
RDY/BSY (PC Card memory mode)	37	O	In memory mode, this signal is: • Set high when the SiliconDrive II CF is ready to accept a new data transfer operation. • Held low when the card is busy. The host memory card socket must provide a pull-up resistor. At power-up and reset, the RDY/-BSY signal is held low (busy) until the SiliconDrive II CF has completed its power-up or reset function. No access of any type should be made to the SiliconDrive II CF during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the SiliconDrive II CF has been powered up with +RESET continuously disconnected or asserted.
-IREQ (PC Card I/O mode) Input Acknowledge			**I/O Operation.** After the SiliconDrive II CF has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE mode)			In true IDE mode, this signal is the active high Interrupt Request to the host.
-REG (PC Card memory mode) Attribute Memory Select	44	I	This signal is used during memory cycles to distinguish between common memory and register (attribute) memory accesses. This signal is set: • High for common memory. • Low for attribute memory.

Table 7: Signal Descriptions (Continued)

Signal Name	Pin	Type	Description
-REG (PC Card I/O mode)			The signal must also be active (low) during I/O cycles when the I/O address is on the bus.
-DMACK (True IDE mode)			In true IDE mode, this signal is used by the host in response to DMARQ to initiate DMA transfers. The DMARQ/ -DMACK handshake is used to provide flow control during the transfer. When -DMACK is asserted, -CS0 and -CS1 are not asserted and transfers are 16-bits wide.
DMACK (UDMA protocol active)			In UDMA mode, this signal is used by the host in response to DMARQ to initiate DMA transfers. The DMARQ/ DMACK handshake is used to provide flow control during the transfer. When DMACK is asserted, -CS0 and -CS1 are not asserted and transfers are 16-bits wide.
-RESET (PC Card memory mode)	41	I	When the pin is high, this signal resets the SiliconDrive II CF. The SiliconDrive II CF is reset only at power-up if this pin is left high or open from power-up. The SiliconDrive II CF is also reset when the Soft Reset bit in the Card Configuration Option register is set.
-RESET (PC Card I/O mode)			This signal is the same as the PC Card Memory Mode signal.
-RESET (True IDE mode)			In the true IDE mode, this input pin is the active low hardware reset from the host.
V_{CC} (PC Card memory mode)	13, 38	-	+5V, +3.3V power.

Table 7: Signal Descriptions (Continued)

Signal Name	Pin	Type	Description
V_{CC} (PC Card I/O mode)			This signal is the same for all modes.
V_{CC} (True IDE mode)			This signal is the same for all modes.
-VS1, -VS2	33, 40	O	**Voltage Sense Signals.** • -VS1 is grounded so that the SiliconDrive II CF CIS can be read at 3.3V. • -VS2 is reserved by PC Card for a secondary voltage.
-VS1, -VS2 (PC Card I/O mode)			This signal is the same for all modes.
-VS1, -VS2 (True IDE mode)			This signal is the same for all modes.
-WAIT (PC Card memory mode)	42	O	The -WAIT signal is driven low by the SiliconDrive II CF to signal the host to delay completion of a memory or I/O cycle that is in progress.
-WAIT (PC Card I/O mode)			This signal is the same as the PC Card Memory Mode signal.
-IORDY (True IDE mode)			In true IDE mode, this output signal may be used as IORDY.
-DDMARDY (UDMA write protocol active)			In all modes, when UDMA mode DMA write is active, this signal is asserted by the device during a data burst to indicate that the device is ready to receive UDMA data out bursts. The device may negate -DDMARDY to pause a UDMA transfer.

Table 7: Signal Descriptions (Continued)

Signal Name	Pin	Type	Description
DSTROBE (UDMA read protocol active)			In all modes, when UDMA mode DMA read is active, this signal is the data in strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause a UDMA data in burst.
-WE (PC Card memory mode)	36	I	This is a signal driven by the host and used for strobing memory write data to the registers of the SiliconDrive II CF when the card is configured in the memory interface mode. This signal is also used for writing the configuration registers.
-WE (PC Card I/O mode)			In PC Card I/O mode, this signal is used for writing the configuration registers.
-WE (True IDE mode)			In true IDE mode, this input signal is not used and should be connected to V_{CC} by the host.
WP (PC Card memory mode)	24	O	**Write Protect Memory Mode.** The SiliconDrive II CF does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
-IOIS16 (PC Card I/O mode)			**I/O Operation.** When the SiliconDrive II CF is configured for I/O operation, pin 24 is used for the -I/O Selected, which is a 16-bit port (-IOIS16) function. A low signal indicates that a 16-bit or odd byte only operation can be performed at the addressed port.
-IOCS16 (True IDE mode)			In true IDE mode, this output signal is the Pass Diagnostic signal in the Master/Slave handshake protocol..

ABSOLUTE MAXIMUM RATINGS

Table 8: Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Units
T_S	Storage Temperature	-55	125	°C
T_A	Operating Temperature	-40	85	°C
V_{CC}	V_{CC} with Respect to GND	-0.5	V_{CC} + 0.5	V
V_{IN}	Input Voltage	-0.3	V_{CC} + 0.3	V
V_{OUT}	Output Voltage	-	6.0	V

DC CHARACTERISTICS

Table 9: DC Characteristics

Symbol	Parameter	3.3 V ± 5%		5V ± 10%		Units
		Minimum	Maximum	Minimum	Maximum	
V_{CC}	Power Supply Voltage	3.15	3.45	4.5	5.5	V
I_{LI}	Input Leakage *(1) Current	-	10	-	10	µA
I_{LO}	Output Leakage *(1) Current	-	10	-	10	µA
V_{CCR}	V_{CC} Read Current	50	100	60	120	mA
V_{CCW}	V_{CC} Write Current	50	100	60	120	mA
V_{CCS}	V_{CC} Standby Current	-	0.3	-	0.5	mA
V_{IL}	Input Low Voltage	-0.3	V_{CC} x 0.3	-0.3	V_{CC} x 0.3	V
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	-	0.45	-	0.45	V
V_{OH}	Output High Voltage	2.4	-	2.4	-	V

AC CHARACTERISTICS

Attribute and Common Memory Read Timing

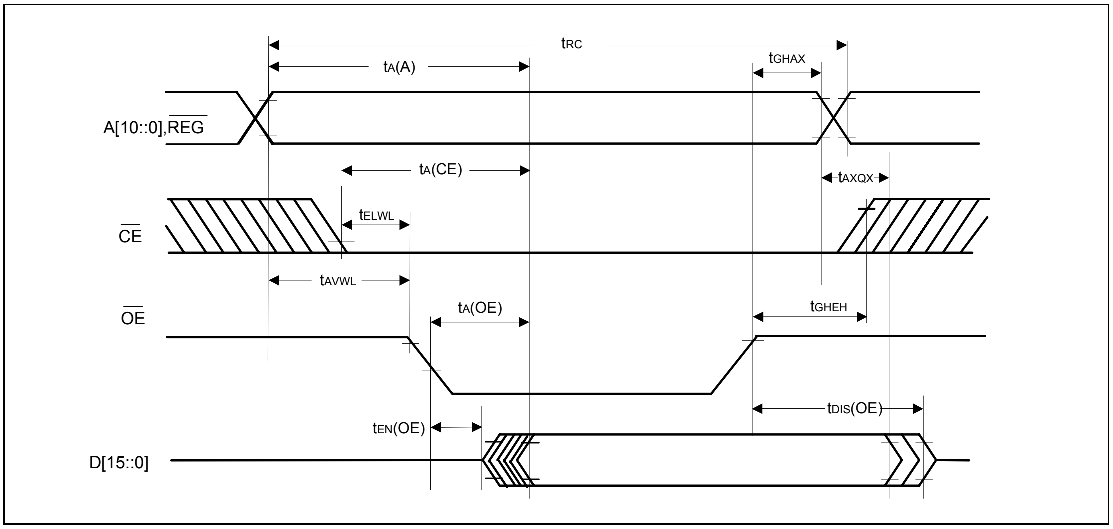

Figure 2: Attribute and Common Memory Read Timing Diagram

Table 10: Attribute and Common Memory Read Timing

Symbol	Parameter	Minimum	Maximum	Units
t_{RC}	Read Cycle Time	250	-	ns
$t_A(A)$	Address Access Time	-	250	ns
$t_A(CE)$	Card Enable Access Time	-	250	ns
$t_A(OE)$	Output Enable Access Time	-	125	ns
$t_{DIS}(OE)$	Output Disable Time from OE	-	100	ns
$t_{EN}(OE)$	Output Enable Time from OE	5	-	ns
t_{AXQX}	Data Valid from Address Change	0	-	ns
t_{AVWL}	Address Setup Time	30	-	ns
t_{AXQX}	Address Hold Time	20	-	ns
t_{ELWL}	Card Enable Setup Time before OE	10	-	ns
t_{GHEH}	Card Enable Hold Time following OE	15	-	ns

Attribute and Common Memory Write Timing

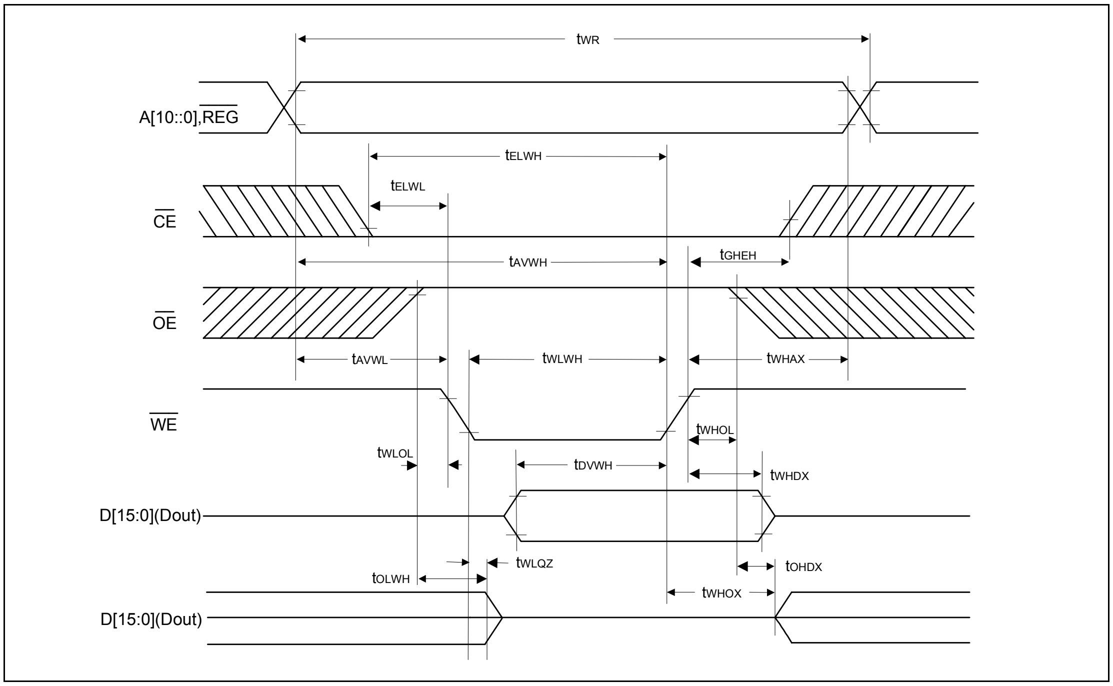

Figure 3: Attribute and Common Memory Write Timing Diagram

Table 11: Attribute and Common Memory Write Timing

Symbol	Parameter	Minimum	Maximum	Units
t_{WR}	Write Cycle Time	250	-	ns
t_{WLWH}	Write Pulse Width	150	-	ns
t_{AVWL}	Address Setup Time	30	-	ns
t_{AVWH}	Address Setup Time for WE	30	-	ns
t_{ELWH}	Card Enable Setup Time for WE	30	-	ns
t_{WHDX}	Data Hold Time	30	-	ns
t_{WHAX}	Write Recover Time	15	-	ns
t_{WLQZ}	Output Disable Time from WE	-	100	ns
t_{OLWH}	Output Disable Time from OE	-	100	ns
t_{WHOX}	Output Enable Time from WE	10	-	ns
t_{OHDX}	Output Enable Time from OE	10	-	ns
t_{WLOL}	Output Enable Setup for WE	10	-	ns
t_{WHOL}	Output Enable Hold from WE	10	-	ns
t_{ELWL}	Card Enable Setup Time before WE	0	-	ns
t_{GHEH}	Card Enable Hold Time from WE	15	-	ns
t_{DVWH}	Data Setup Time	80	-	ns

I/O Access Read Timing

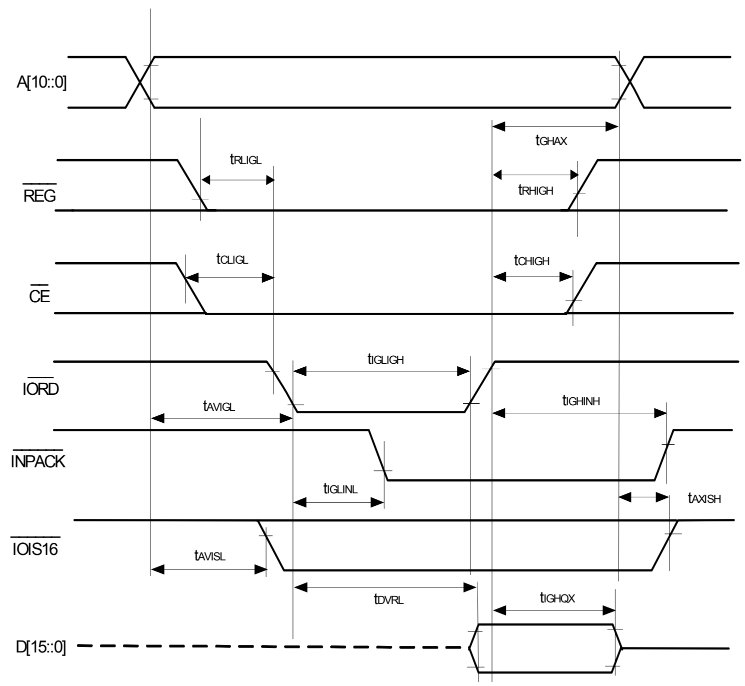

Figure 4: I/O Access Read Timing Diagram

Table 12: I/O Access Read Timing

Symbol	Parameter	Minimum	Maximum	Units
t_{DVRL}	Data Delay after IORD	-	45	ns
t_{IGHQX}	Data Hold following IORD	5	-	ns
t_{IGLIGH}	IORD Pulse Width	55	-	ns
t_{AVIGL}	Address Setup before IORD	15	-	ns
t_{GHAX}	Address Hold following IORD	10	-	ns
t_{CLIGL}	CE Setup before IORD	5	-	ns
t_{CHIGH}	CE Hold following IORD	10	-	ns
t_{RLIGL}	REG Setup before IORD	5	-	ns
t_{RHIGH}	REG Hold following IORD	0	-	ns
t_{IGLINL}	INPACK Delay falling from IORD	0	45	ns
t_{IGHINH}	INPACK Delay Rising from IORD	-	45	ns
t_{AVISL}	IOIS16 Delay Falling from Address	-	35	ns
t_{AXISH}	IOIS16 Delay Rising from Address	-	35	ns

I/O Access Write Timing

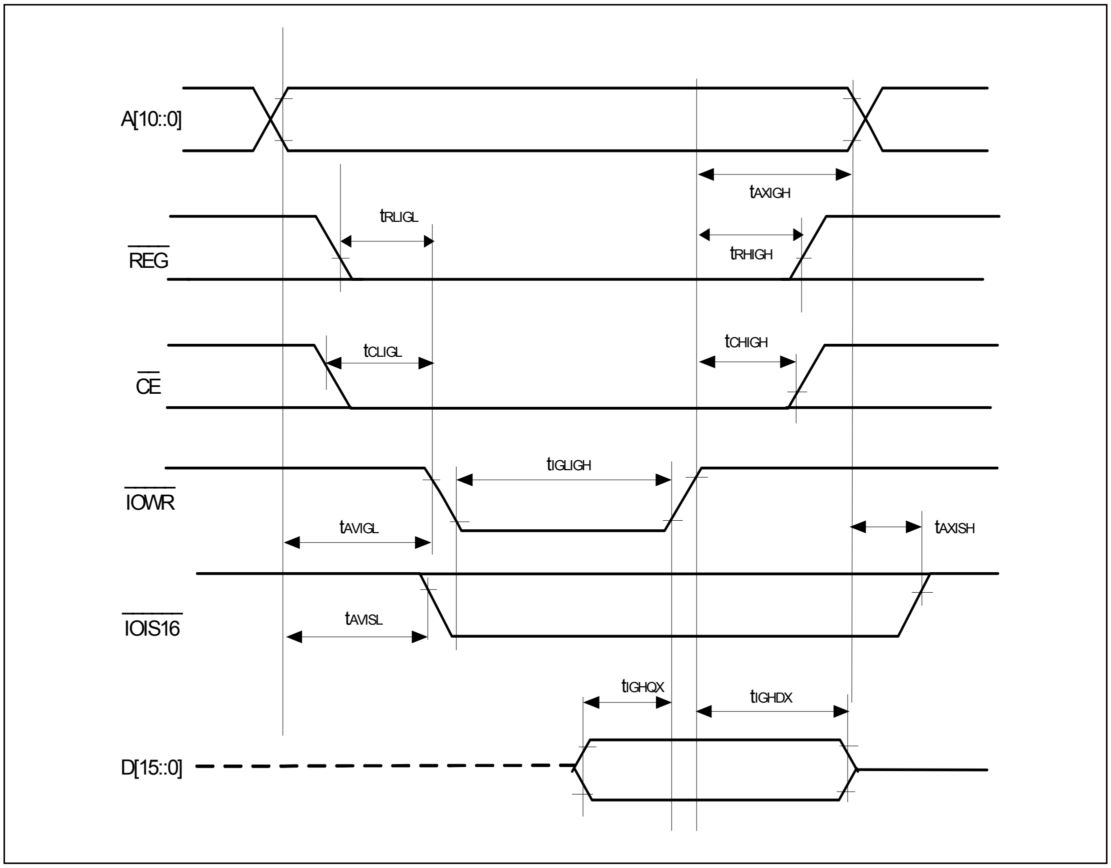

Figure 5: I/O Access Write Timing Diagram

Table 13: I/O Access Write Timing

Symbol	Parameter	Minimum	Maximum	Units
t_{IGHDX}	Data Hold following IOWR	5	-	ns
t_{IGHQX}	Data Setup before IOWR	15	-	ns
t_{IGLIGH}	IOWR Pulse Width	55	-	ns
t_{AVIGL}	Address Setup before IOWR	15	-	ns
t_{AXIGH}	Address Hold following IOWR	10	-	ns
t_{CLIGL}	CE Setup before IOWR	5	-	ns
t_{CHIGH}	CE Hold following IOWR	10	-	ns
t_{RLIGL}	REG Setup before IOWR	5	-	ns
t_{RHIGH}	REG Hold following IOWR	0	-	ns
t_{AVISL}	IOIS16 Delay Falling from Address	-	35	ns
t_{AXISH}	IOIS16 Delay Rising from Address	-	35	ns

True IDE PIO Mode Read/Write Access Timing

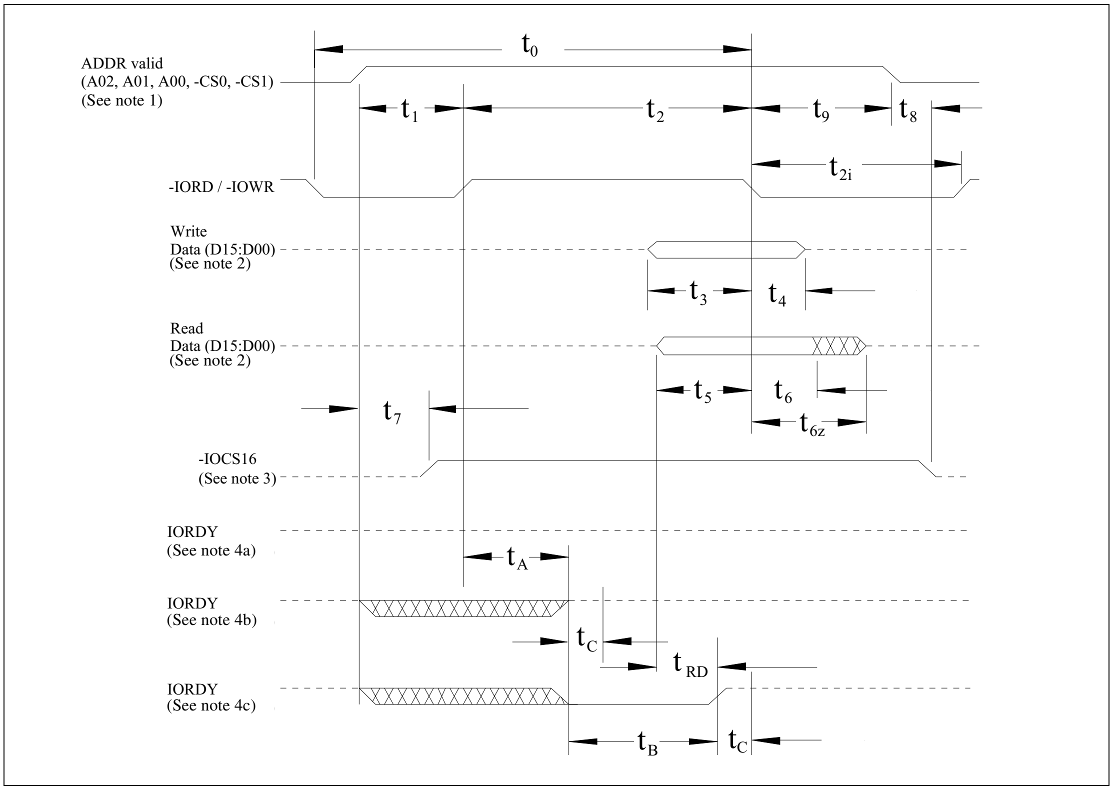

Figure 6: True IDE PIO Mode Read/Write Access Timing Diagram

Notes:

1. The device address consists of -CS0, -CS1, and A[02::00].
2. The data consists of D[15::00] (16-bit) or D[07::00] (8 bit).
3. -IOCS16 is shown for PIO modes 0, 1, and 2. For other modes, this signal is ignored.
4. The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after t_A from the assertion of -IORD or -IOWR. The assertion and negation of IORDY is described in the following three cases:
   a. The device never negates IORDY; no wait is generated.
   b. The device starts to drive IORDY low before t_A, but causes IORDY to be asserted before t_A; no wait generated.
   c. The device drives IORDY low before t_A; wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and -IORD is asserted, the device places read data on D15-D00 for t_{RD} before causing IORDY to be asserted.

Table 14: True IDE PIO Mode Read/Write Access Timing

Symbol	Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Note	Units
t_0	Cycle Time (minimum)	600	383	240	180	120	100	80	1	ns
t_1	Address Valid to IORD/-IOWR Setup (minimum)	70	50	30	30	25	15	10	-	ns
t_2	-IORD/-IOWR (minimum)	165	125	100	80	70	65	55	1	ns
t_2	-IORD/-IOWR (minimum) register (8 bit)	290	290	290	80	70	65	55	1	ns
t_{2i}	-IORD/-IOWR Recovery Time (minimum)	-	-	-	70	25	25	20	1	ns
t_3	-IOWR Data Setup (minimum)	60	45	30	30	20	20	15	-	ns
t_4	-IOWR Data Hold (minimum)	30	20	15	10	10	5	5	-	ns
t_5	-IORD Data Setup (minimum)	50	35	20	20	20	15	10	-	ns
t_6	-IORD Data Hold (minimum)	5	5	5	5	5	5	5	-	ns
t_{6Z}	-IORD Data Tristate (maximum)	30	30	30	30	30	20	20	2	
t_7	Address Valid to IOCS16 Assertion (maximum)	90	50	40	N/A	N/A	N/A	N/A	4	ns
t_8	Address Valid to IOCS16 Released (maximum)	60	45	30	N/A	N/A	N/A	N/A	4	ns
t_9	-IORD/-IOWR to Address Valid Hold	20	15	10	10	10	10	10	-	ns
t_{RD}	Read Data Valid to IORDY Active (minimum), if IORDY is initially low after t_A	0	0	0	0	0	0	0	-	ns
t_A	IORDY Setup Time	35	35	35	35	35	N/A[5]	N/A[5]	3	ns
t_B	IORDY Pulse Width (maximum)	1250	1250	1250	1250	1250	N/A[5]	N/A[5]	-	ns
t_C	IORDY Assertion to Release (maximum)	5	5	5	5	5	N/A[5]	N/A[5]	-	ns

Notes:

1. The symbol t_0 is the minimum total cycle time, t_2 is the minimum command active time, and t_{2i} is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_2, and t_{2i} must be met. The minimum total cycle time requirement is greater than the sum of t_2 and t_{2i}. This means a host implementation can lengthen either or both t_2 or t_{2i} to ensure that t_0 is equal to or greater than the value reported in the device's identify device data.
2. This parameter specifies the time from the negation edge of -IORD to the time that the data bus is no longer driven by the CF (tristate).

3. The delay from the activation of -IORD or -IOWR until the state of IORDY is first sampled. If IORDY is inactive, then the host waits until IORDY is active before the PIO cycle can be completed. If the CF is not driving IORDY negated at t_A after the activation of -IORD or -IOWR, then t_5 must be met and t_{RD} is not applicable. If the CF is driving IORDY negated at the time t_A after the activation of -IORD or -IOWR, then t_{RD} must be met and t_5 is not applicable.
4. The symbols t_7 and t_8 apply only to modes 0, 1, and 2. For other modes, this signal is not valid.
5. IORDY is not supported in this mode.

True IDE Multiword DMA Read/Write Access Timing

This function does not apply to SiliconDrive IIs that have DMA disabled.

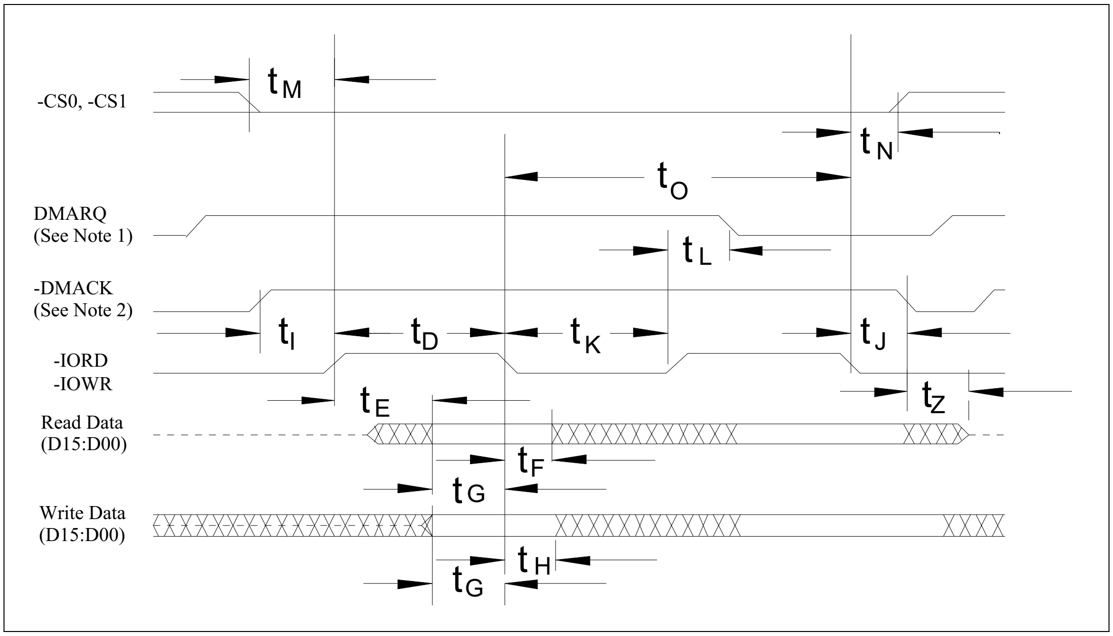

Figure 7: True IDE Multiword DMA Read/Write Access Timing

Notes:

1. If the drive cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of a DMA transfer cycle to suspend the DMA transfers in progress, and reassert the signal at a later time to continue the DMA operation.
2. This signal may be negated by the host to suspend the DMA transfer in progress.

Table 15: True IDE Multiword DMA Read/Write Access Timing

Symbol	Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Note	Units
t_O	Cycle Time (minimum)	480	150	120	100	80	1	ns
t_D	-IORD/-IOWR Asserted Width (minimum)	215	80	70	65	55	1	ns
t_E	-IORD Data Access (maximum)	150	60	50	50	45	-	ns
t_F	-IORD Data Hold (minimum)	5	5	5	5	5	-	ns
t_G	-IORD/-IOWR Data Setup (minimum)	100	30	20	15	10	-	ns

Table 15: True IDE Multiword DMA Read/Write Access Timing

Symbol	Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Note	Units
t_H	-IOWR Data Hold (minimum)	20	15	10	5	5	-	ns
t_I	DMACK to –IORD/-IOWR Setup (minimum)	0	0	0	0	0	-	ns
t_J	-IORD / -IOWR to -DMACK Hold (minimum)	20	5	5	5	5	-	ns
t_{KR}	-IORD Negated Width (minimum)	50	50	25	25	20	1	ns
t_{KW}	-IOWR Negated Width (minimum)	215	50	25	25	20	1	ns
t_{LR}	-IORD to DMARQ Delay (maximum)	120	40	35	35	35	-	ns
t_{LW}	-IOWR to DMARQ Delay (maximum)	40	40	35	35	35	-	ns
t_M	CS(1:0) Valid to –IORD / -IOWR	50	30	25	10	5	-	ns
t_N	CS(1:0) Hold	15	10	10	10	10	-	ns
t_Z	-DMACK	20	25	25	25	25	-	ns

Notes:

1. The symbol t_0 is the minimum total cycle time and t_D is the minimum command active time, while t_{KR} and t_{KW} are the minimum command recovery times or command inactive times for input and output cycles, respectively. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_D, t_{KR}, and t_{KW} must be met. The minimum total cycle time requirement is greater than the sum of t_D and t_{KR}, or t_{KW} for input and output cycles, respectively. This means a host implementation can lengthen either or both of t_D and either of t_{KR} and t_{KW} as needed to ensure that t_0 is equal to or greater than the value reported iN The device’s identify device data.

Ultra DMA Data Burst Timing Requirements

The following figures and table describe the requirements for the Ultra DMA (UDMA) data burst timing.

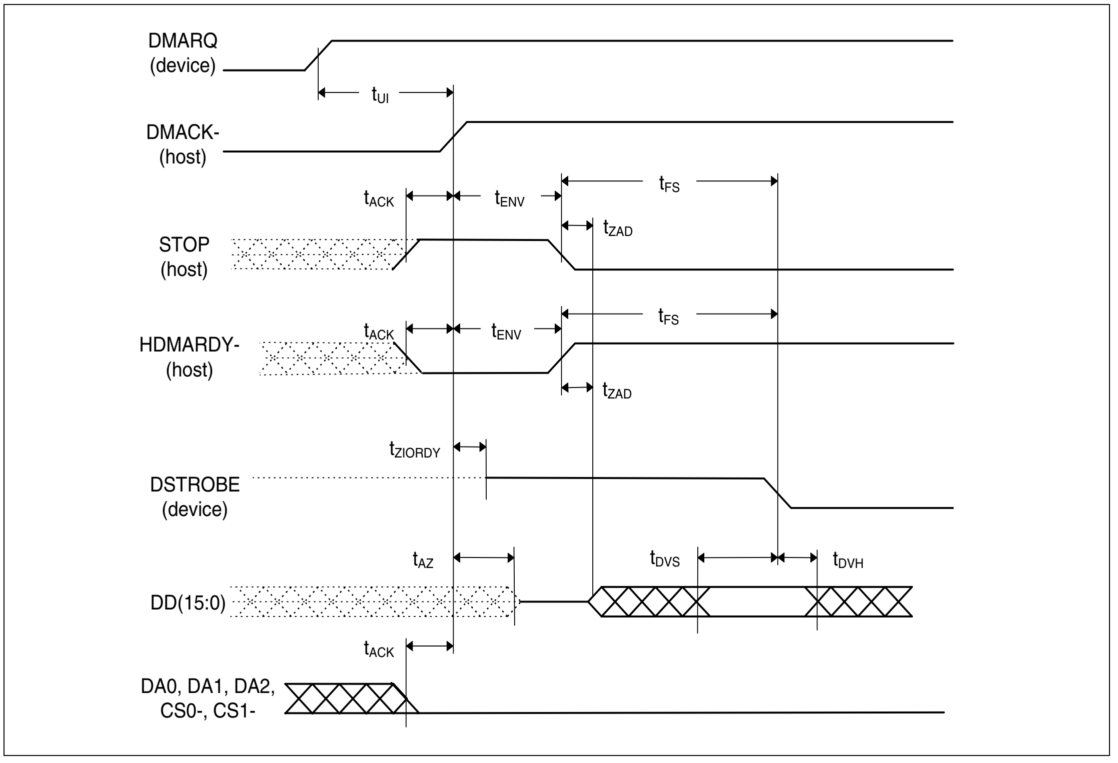

Figure 8: Initiating a UDMA Data-In Burst

Note: The definitions for the DIOW-:STOP, DIOR-:HDMARDY-:HSTROBE, and IORDY:DDMARDY-:DSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

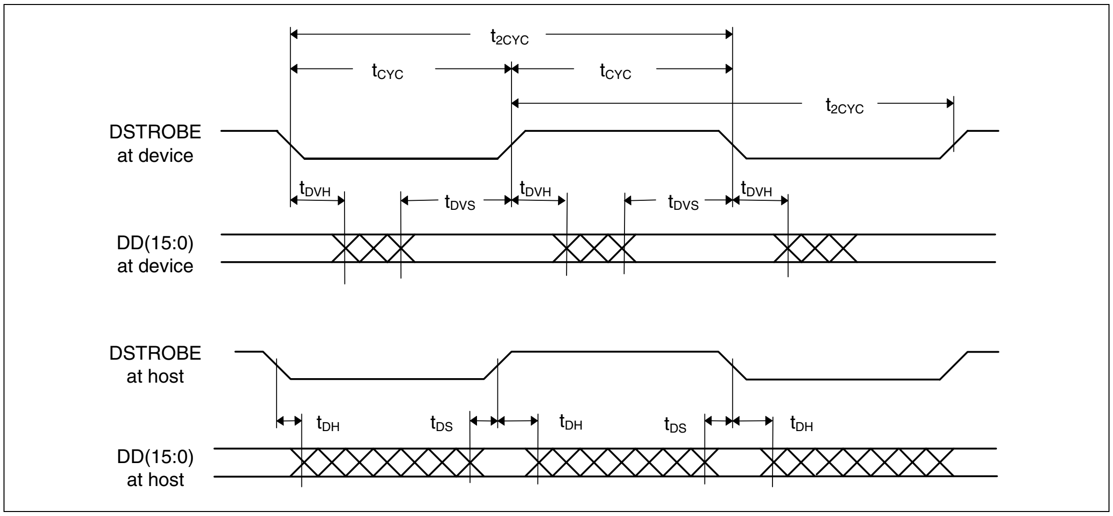

Figure 9: Sustained UDMA Data-In Burst

Note: DD(15:0) and DSTROBE signals are shown at both the host and the device to emphasize that the cable settling time as well as cable propagation delay does not allow the data signals to be considered stable at the host until some time after they are driven by the device.

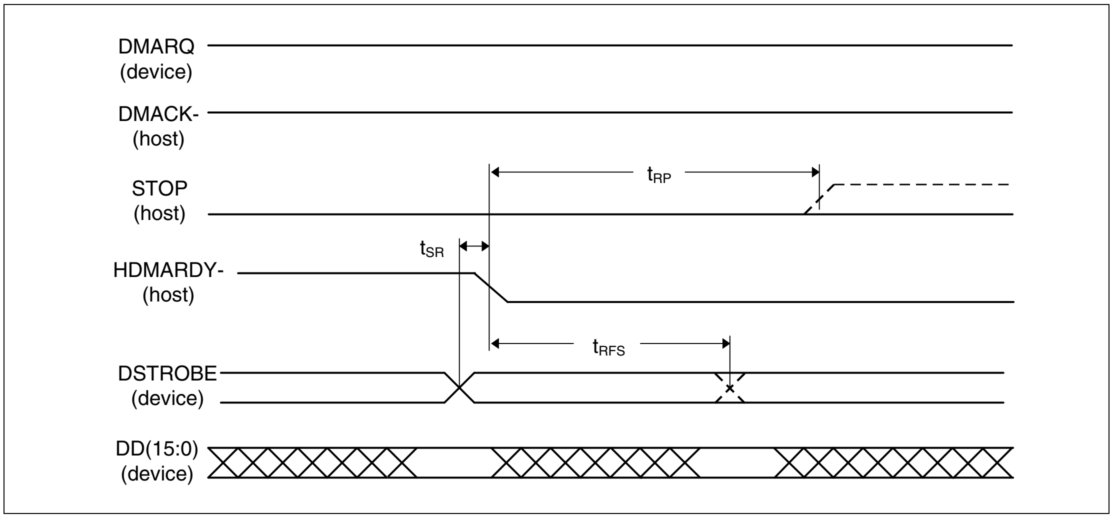

Figure 10: Host Pausing a UDMA Data-In Burst

Notes:

1. The host may assert STOP to request termination of the UDMA burst no sooner than t_{RP} after HDMARDY- is negated.
2. If the t_{SR} timing is not satisfied, the host may receive zero, one, or two more data words from the device.

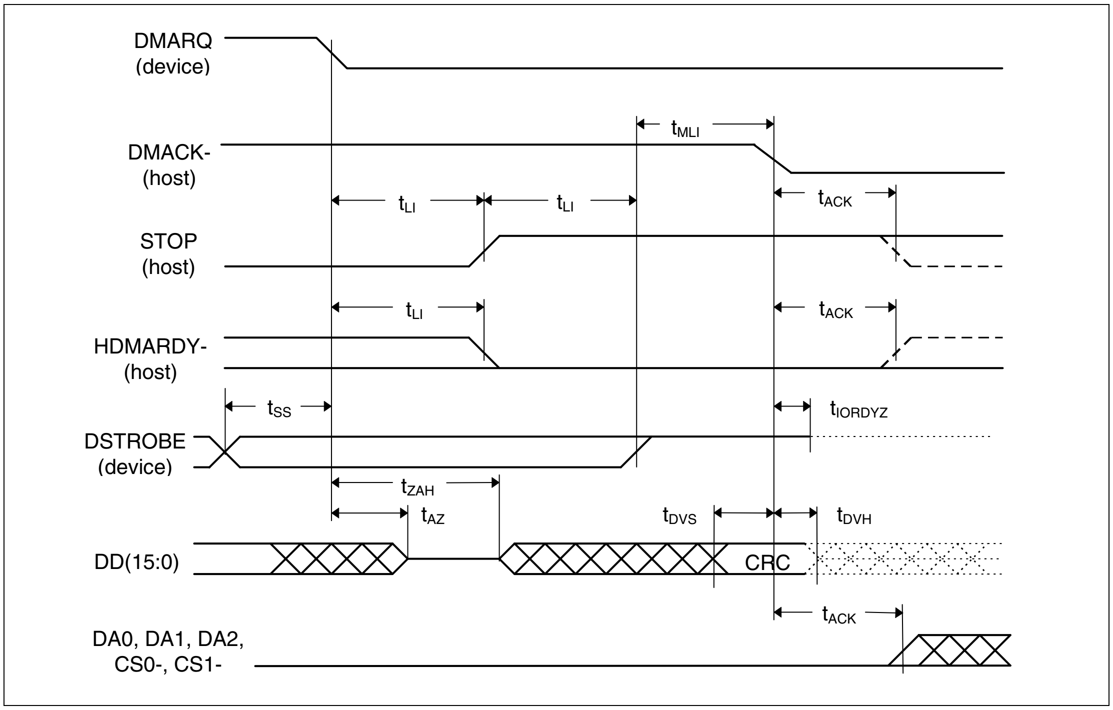

Figure 11: Device Terminating a UDMA Data-In Burst

Note: The definitions for the DIOW-:STOP, DIOR-:HDMARDY-:HSTROBE, and IORDY:DDMARDY-:DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

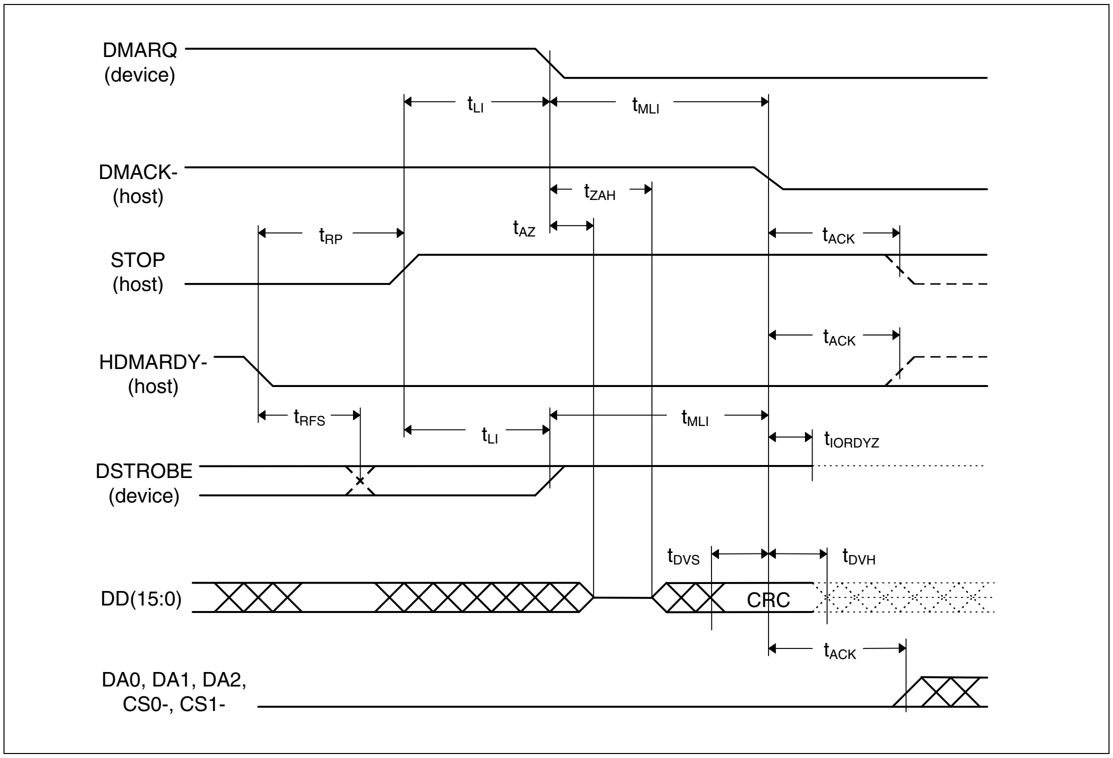

Figure 12: Host Terminating a UDMA Data-In Burst

Note: The definitions for the DIOW-:STOP, DIOR-:HDMARDY-:HSTROBE, and IORDY:DDMARDY-:DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

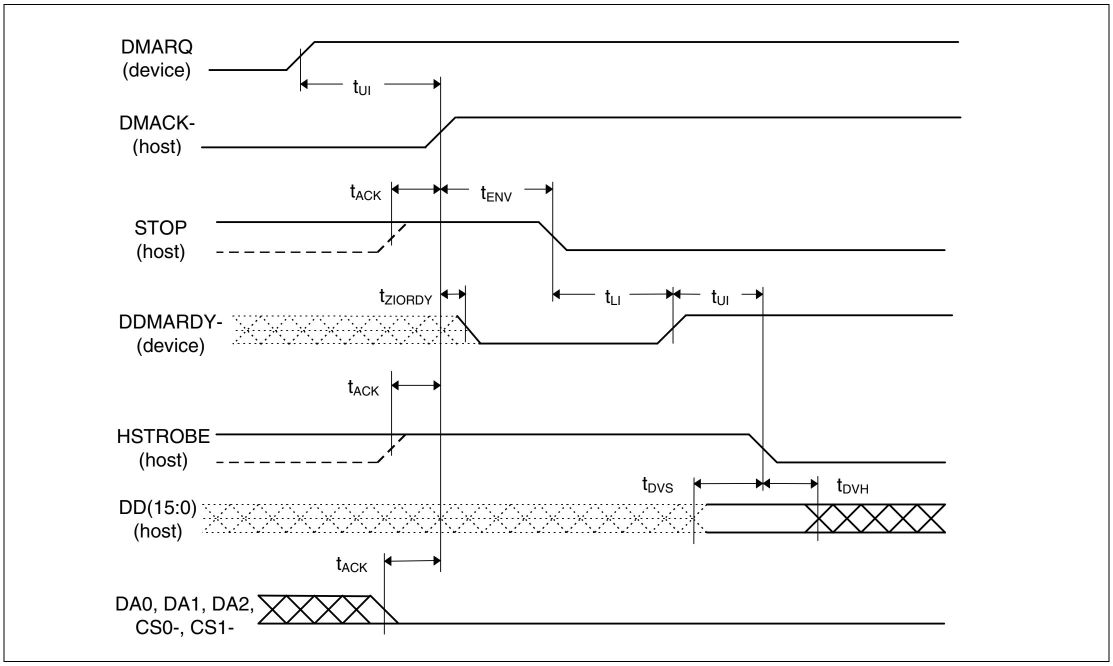

Figure 13: Initiating a UDMA Data-Out Burst

Note: The definitions for the DIOW-:STOP, IORDY:DDMARDY-:DSTROBE, and DIOR-:HDMARDY-:HSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

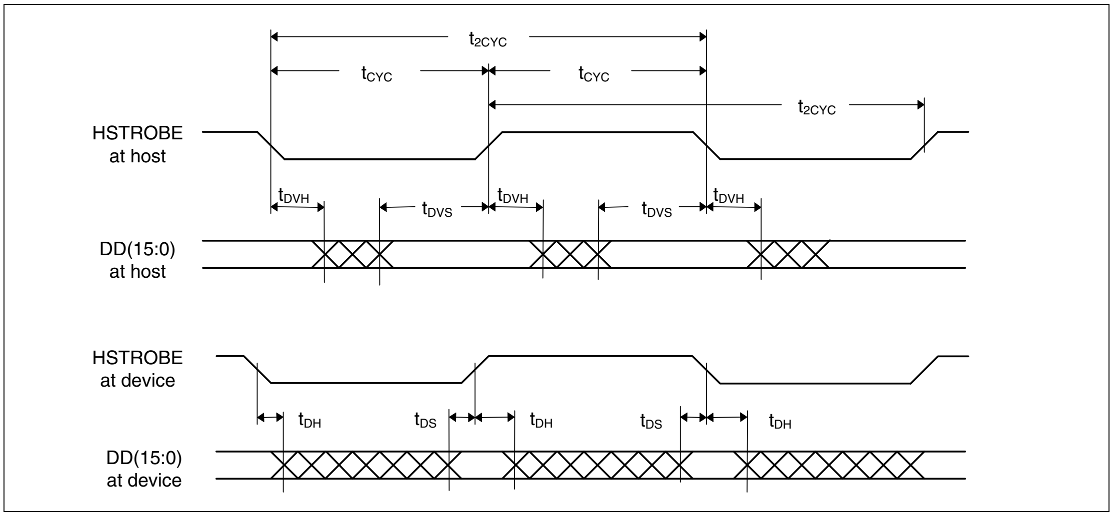

Figure 14: Sustained UDMA Data-Out Burst

Note: DD(15:0) and HSTROBE signals are shown at both the device and the host to emphasize that the cable settling time as well as cable propagation delay does not allow the data signals to be considered stable at the device until some time after they are driven by the host.

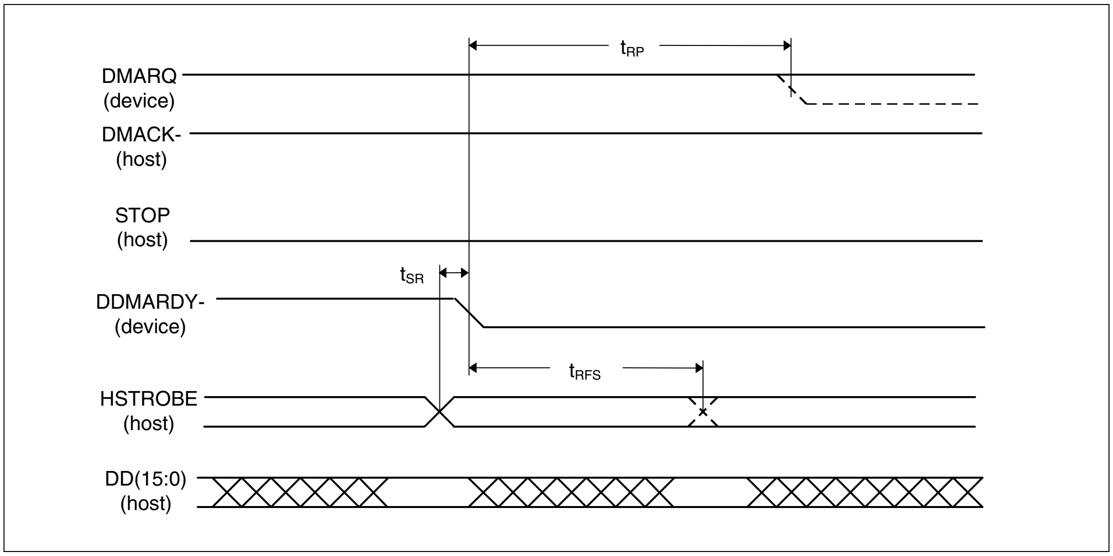

Figure 15: Device Pausing a UDMA Data-Out Burst

Notes:

1. The device may negate DMARQ to request termination of the UDMA burst no sooner than t_{RP} after DDMARDY- is negated.
2. If the t_{SR} timing is not satisfied, the host may receive zero, one, or two more data words from the host.

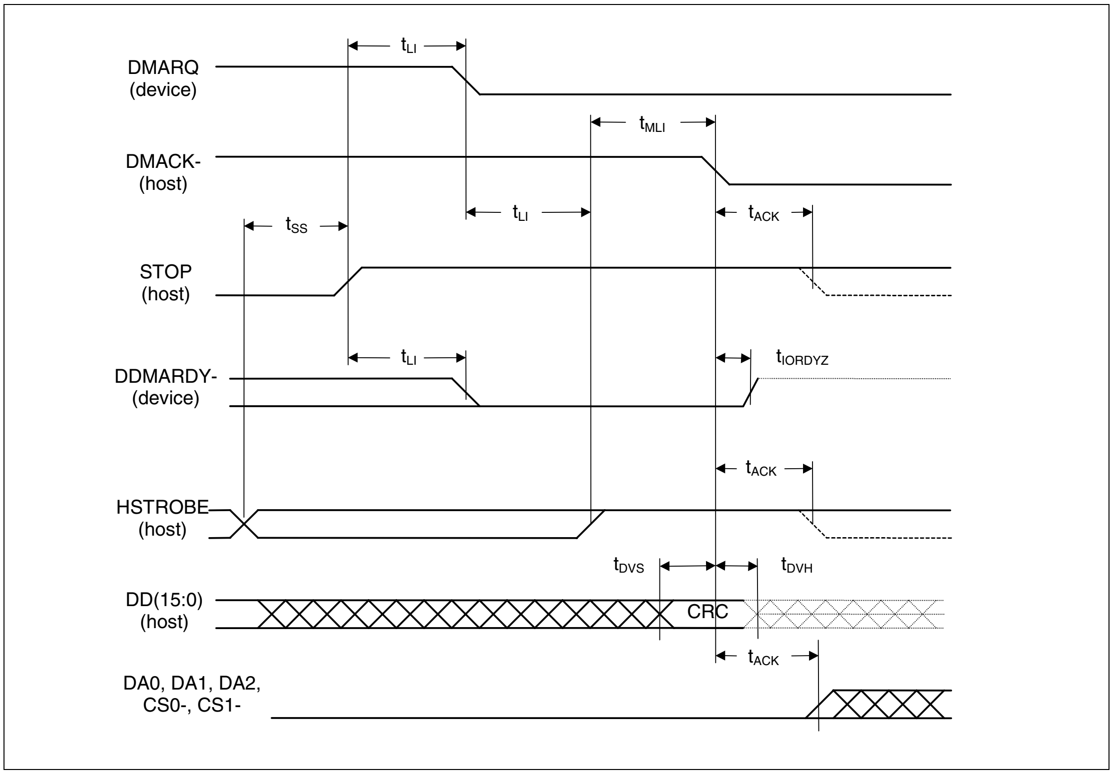

Figure 16: Host Terminating a UDMA Data-Out Burst

Note: The definitions for the DIOW-:STOP, IORDY:DDMARDY-:DSTROBE, and DIOR-:HDMARDY-:HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

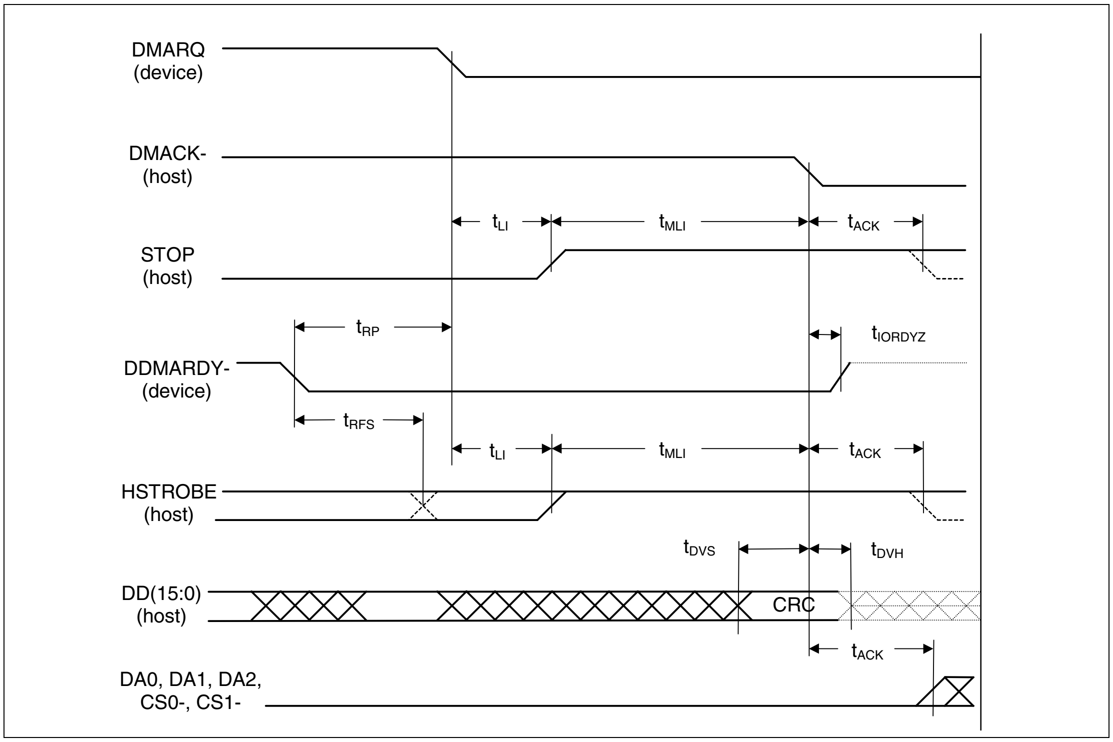

Figure 17: Device Terminating a UDMA Data-Out Burst

Note: The definitions for the DIOW-:STOP, IORDY:DDMARDY-:DSTROBE, and DIOR-:HDMARDY-:HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Table 16: UDMA Data Burst Timing Requirements

Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Comment (see Notes 1 and 2)	Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$t_{2CYCTYP}$	240	-	160	-	120	-	90	-	60	-	Typical sustained average two-cycle time.	ns
t_{CYC}	112	-	73	-	54	-	39	-	25	-	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge).	ns
t_{2CYC}	230	-	154	-	115	-	86	-	57	-	Two-cycle time allowing for clock variations (from rising edge to next rising edge, or from falling edge to next falling edge of STROBE).	ns
t_{DS}	15		10		7		7		5		Data setup time at recipient.	ns
t_{DH}	5	-	5	-	5	-	5	-	5	-	Data hold time at recipient.	ns
t_{DVS}	70	-	48	-	30	-	20	-	6	-	Data valid setup time at sender (from data valid until STROBE edge) (see Note 4).	ns
t_{DVH}	6	-	6	-	6	-	6	-	6	-	Data valid hold time at sender (from STROBE edge until data may become invalid) (see Note 4).	ns
t_{FS}	0	230	0	200	0	170	0	130	0	120	First STROBE time (for device to first negate DSTROBE from STOP during a data-in burst).	ns
t_{LI}	0	150	0	150	0	150	0	100	0	100	Limited interlock time (see Note 3).	ns
t_{MLI}	20	-	20	-	20	-	20	-	20	-	Interlock time with minimum (see Note 3).	ns
t_{UI}	0	-	0	-	0	-	0	-	0	-	Unlimited interlock time (see Note 3).	ns
t_{AZ}	-	10	-	10	-	10	-	10	-	10	Maximum time allowed for output drivers to release (from asserted or negated).	ns
t_{ZAH}	20	-	20	-	20	-	20	-	20	-	Minimum delay time required for output.	ns
t_{ZAD}	0	-	0	-	0	-	0	-	0	-	Drivers to assert or negate (from released).	ns
t_{ENV}	20	70	20	70	20	70	20	55	20	55	Envelope time (from DMACK- to STOP and HDMARDY- during data-in burst initiation, and from DMACK to STOP during data-out burst initiation).	ns

Table 16: UDMA Data Burst Timing Requirements (Continued)

Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Comment (see Notes 1 and 2)	Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{SR}	-	50	-	30	-	20	-	NA	-	NA	STROBE to DMARDY- time (if DMARDY- is negated before this long after STROBE edge, the recipient receives no more than one additional data word).	ns
t_{RFS}	-	75	-	70	-	60	-	60	-	60	Ready-to-final STROBE time (no STROBE edges are sent this long after negation of DMARDY-).	ns
t_{RP}	160	-	125	-	100	-	100		100	-	Minimum time to assert STOP or negate DMARQ.	ns
t_{IORDYZ}	-	20	-	20	-	20	-	20	-	20	Maximum time before releasing IORDY.	ns
t_{ZIORDY}	0	-	0	-	0	-	0	-	0	-	Minimum time before driving STROBE (see note 5).	ns
t_{ACK}	20	-	20	-	20	-	20	-	20	-	Setup and hold times for DMACK- (before assertion or negation).	ns
t_{SS}	50	-	50	-	50	-	50	-	50	-	Time from STROBE edge to negation of DMARQ or assertion of STOP (when the sender terminates a burst).	ns

Notes:

1. Timing parameters are measured at the connector of the sender or receiver to which the parameter applies. Both STROBE and DMARDY- timing measurements are taken at the sender's connector.

   Example: For example, the sender stops generating STROBE edges t_{RFS} after the negation of DMARDY-.
2. All timing measurement switching points (low-to-high and high-to-low) are taken at 1.5V.
3. The symbols t_{UI}, t_{MLI}, and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks (i.e., either the sender or recipient is waiting for the other to respond with a signal before proceeding). The symbol t_{UI} is an unlimited interlock that has no maximum time value, t_{MLI} is a limited time-out that has a defined minimum, and t_{LI} is a limited time-out that has a defined maximum.
4. The test load for t_{DVS} and t_{DVH} are a lumped capacitor load with no cable or receivers. Timing for t_{DVS} and t_{DVH} are met for all capacitive loads from 15pf to 40pf where all signals have the same capacitive load value.
5. The symbol t_{ZIORDY} may be greater than t_{ENV} since the device has a pull-up on IORDY- giving it a known state when released.

ATTRIBUTE MEMORY DESCRIPTION AND OPERATION

The attribute memory plane can be read or written to by asserting the REG# signal, qualified by the appropriate combination of CE1#, OE#, and WE#. An attribute memory map describing the type and location of the information maintained in the attribute memory plane is provided in "Attribute Memory Map" on page 39.

With respect to SiliconDrive II CF, attribute memory consists of two sections:

- Card Information Structure (CIS), which contains a description of the Card's capabilities and specifications.
- Function Configuration Registers (FCRs), which consists of four registers, that can be read or written to by a host to configure the Card for specific purposes.

ATTRIBUTE MEMORY READ OPERATIONS

Attribute memory read operations are enabled by asserting REG#, OE#, and CE1# low. Odd byte read operations from the attribute memory plane are not valid.

Table 17: Attribute Memory Read Operations

Function Mode	REG#	CE1#	CE2#	A0	OE#	WE#	D[15:8]	D[7:0]
Standby	L	H	H	X	X	X	High-Z	High-Z
Byte Access	L	L	H	L	L	H	High-Z	Even
	L	H	L	H	L	H	High-Z	Not Valid
Word Access	L	L	L	X	L	H	Not Valid	Even
Odd Byte Only Access	L	L	H	X	H	H	Not Valid	High-Z

ATTRIBUTE MEMORY WRITE OPERATIONS

Attribute memory write operations are enabled by asserting REG#, WE#, and CE1# low. Odd byte write operations from the attribute memory plane are not valid.

Table 18: Attribute Memory Write Operations

Function Mode	REG#	CE1#	CE2#	A0	OE#	WE#	D[15:8]	D[7:0]
Standby	L	H	H	X	X	X	High-Z	High-Z
Byte Access	L	L	H	L	H	L	High-Z	Even
	L	H	L	H	H	L	High-Z	Not Valid
Word Access	L	L	L	X	H	L	Not Valid	Even
Odd Byte Only Access	L	L	H	X	H	H	Not Valid	High-Z

ATTRIBUTE MEMORY MAP

As stated earlier, the Attribute Memory plane is comprised of two components, the CIS and the FCRs. The following tables detail the type, location, and read/ write requirements for each of the four FCRs maintained in the attribute memory plane.

Table 19: Attribute Memory Map

Register	Operation	Addr	CE1#	REG#	WE#	OE#
Card Information Structure	Read	X	0	0	1	0
	Write	X	0	0	0	1
Configuration Option	Read	200h	0	0	1	0
	Write	200h	0	0	0	1
Card Configuration and Status	Read	202h	0	0	1	0
	Write	202h	0	0	0	1
Pin Replacement	Read	204h	0	0	1	0
	Write	204h	0	0	0	1
Socket and Copy	Read	206h	0	0	1	0
	Write	206h	0	0	0	1

CARD INFORMATION STRUCTURE

The CIS is data that describes the SiliconDrive II CF, and is described by the CFA standard. This information can be used by the host system to determine a number of things about the Card that has been inserted. For information regarding the exact nature of this data and how to design the host software to interpret it, refer to the *PC Card Standard Metaformat Specification*.

Table 20: Card Information Structure

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
00h	01h	CISTPL_DEVICE								Device information tuple	Tuple code
02h	03h	-								Link length is 3 bytes	Link to next tuple
04h	D9h	Device Type Code Dh = I/O				W 1	Device Speed 1			• I/O device • No WP • Speed = 100ns	• Device ID • WPS • Device speed
06h	01h	1X					2K			2KB of address space	Device size
08h	FFh	List End Marker								End of device	END marker
0Ah	1Ch	CISTPL_DEVICE_OC								Other conditions device in tuple code	Tuple code
0Ch	04h	TPL_LINK								Link length is 4 bytes	Link to next tuple
0Eh	02h	EXT Reserved V_{CC} MWAIT								3V, wait is Not Used	Other conditions information field
10h	D9h	Device Type				W P S	Device Speed			• Device type = DH: I/O • Device WPS = 1: No WP • Device speed = 1: 250ns	-
12h	01h	1x				2K units				2KB of address space	Device size
14h	FFh	List End Marker								End of device	End marker
16h	18h	CISTPL_JEDEC_C								JEDEC ID common memory	Tuple code
18h	02h	TPL_LINK								Link length is 2 bytes	Link to next tuple
1Ah	DFh	PCMCIA Manufacturer's JEDEC								Manufacturer's ID code -	- JEDEC ID
1Ch	01h	PCMCIA JEDEC Device Code								Second byte of JEDEC ID	-
1Eh	20h	CISTPL_MANFID								Manufacturer's ID code	Tuple code
20h	04h	TPL_LINK								-	-
22h	00h	Low Byte of PCMCIA Manufacturer's Code								JEDEC manufacturer's ID	Low byte of manufacturer's code
24h	00h	High Byte of PCMCIA Manufacturer's Code								Code of 0, because the other byte is the JEDEC 1 byte manufacturer's ID	High byte of the manufacturer's code
26h	00h	Low Byte of Product Code								Manufacturer's code for SiliconDrive II CF	Low byte of the product code
28h	00h	High Byte of Product Code								Manufacturer's code for SiliconDrive II CF	High byte of the product code
2Ah	21h	CISTPL_FUNCID								Function ID tuple	Tuple code
2Ch	02h	TPL_LINK								Link length is 2 bytes	Link to next tuple

Table 20: Card Information Structure (Continued)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
2Eh	04h	TPLFID_FUNCTION = 04H								Disk function, which may be silicon or removable	PC Card function code
30h	01h	Reserved				R	P			• R = 0: No BIOS ROM • P = 1: Configure card at power-on	System initialization byte
32h	22h	CISTPL_FUNCE								Function extension tuple	Tuple code
34h	02h	TPL_LINK								Link length is 2 bytes	Link to next tuple
36h	01h	Disk Function Extension Tuple Type								Disk interface type	Extension tuple type for disk
38h	01h	Disk Interface Type								PC Card interface type	Interface type
3Ah	22h	CISTPL_FUNCE								Function extension tuple	Tuple code
3Ch	03h	TPL_LINK								Link length is 3 bytes	Link to next tuple
3Eh	02h	Disk Function Extension Tuple Type								Basic PCMCIA-ATA extension tuple	Extension tuple type for disk
40h	04h	Reserved			D	U	S	V		No Vpp, silicon, single drive • V = 0: No Vpp required • S = 0: Silicon • U = 1: Unique serial number • D = 0: Single drive on Card	Basic ATA option parameters byte 1
42h	07h	R	I	E	N	P3	P2	P1	P0	• P0: Sleep mode supported • P1: Standby mode supported • P2: Idle mode supported • P3: Drive auto power control • N: Some configuration excludes 3X7 • E: Index bit is emulated • I: Twin IOIS16# data register only • R: Reserved	Basic ATA option parameters byte 2
44h	1Ah	CISTPL_CONFIG								Configuration tuple	Tuple code
46h	05h	TPL_LINK								Link length is 5 bytes	Link to next tuple
48h	01h	RAS		RMS		RAS		-		• RFS: Reserved • RMS: TPCC RMSK size -1 = 0 • RAS: TPCC_RADR size -1 = 1 • 1-byte register mask • 2-byte configuration base address	Size of fields byte TPCC_SZ
4Ah	07h	TPCC_LAST								Entry with configuration index of 7 is final entry in table	Last entry of configuration registers
4Ch	00h	TPCC_RADR (LSB)								Configuration registers are located at 200H in REG space	Location of configuration registers
4Eh	02h	TPCC_RADR (MSB)								-	-
50h	0Fh	Reserved			S	P	C	I	-	• I: Configuration index • C: Configuration and status • P: Pin replacement • S: Socket and copy	Configuration registers present mask TPCC_RMSK
52h	1Bh	CISTPL_TABLE_ENTRY								Configuration table entry tuple	Tuple code
54h	0Bh	TPL_LINK								Link length is 11 bytes	Link to next tuple

Table 20: Card Information Structure (Continued)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
56h	C0h	I	D	Configuration index						Memory-mapped I/O configuration • I = 1: Interface byte follows • D = 1: Default entry • Configuration index = 0	Configuration table index byte TPCE_INDX
58h	C0h	W	R	P	B	Interface Type				• W = 0: Wait not used • R = 1: Ready active • P = 0: WP used • B = 0: BVD1 and BVD2 not used • IF type = 0: Memory interface	Interface description field TPCE_IF
5Ah	A1h	M	MS	IR	IO	T		P		• M = 1: Miscellaneous information present • MS = 01: Memory space information single 2-byte length • IR = 0: No interrupt information present • IO = 0: No I/O port information present • T = 0: No timing information present • P = 1: V_{CC} only information	Feature selection byte TPCE_FS
5Ch	27h	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows • R: Reserved • DI: Powerdown current information • PI: Peak current information • AI: Average current information • SI: Static current information • HV: Maximum voltage information • LV: Minimum voltage information • NV: Nominal voltage information	Power parameters for V_{CC}
5Eh	55h	X	Mantissa				Exponent			Nominal voltage = 5V	V_{CC} nominal value
60h	4Dh	X	Mantissa			Exponent				V_{CC} nominal 4.5V	V_{CC} minimum value
62h	5Dh	X	Mantissa			Exponent				V_{CC} nominal 5.5V	V_{CC} maximum value
64h	75h	X	Mantissa			Exponent				Maximum average current over 10ms is 80mA	Maximum average current
66h	08h	Length in 256 bytes pages (LSB)								Length of memory space is 2KB	Memory space description structures (TPCE_MS)
68h	00h	Length in 256 bytes pages (MSB)								Length of memory space is 2KB	Memory space description structures (TPCE_MS)
6Ah	21h	X	R	P	RO		AT		-	• X = 0: No more miscellaneous fields • R: Reserved • P = 1: Powerdown supported • RO = 0: Not read only mode • A = 0: Audio not supported • T = 0: Single drive	Miscellaneous features field TPCE_MI
6Ch	1Bh	CISTPL_TABLE_ENTRY								Configuration table entry tuple	Tuple code
6Eh	06h	TPL_LINK								Link length is 6 bytes	Link to next tuple

Table 20: Card Information Structure (Continued)

<table>
<tr><th>Attribute Offset</th><th>Data</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th><th>Description of Contents</th><th>CIS Function</th></tr>
<tr><td>70h</td><td>00h</td><td>I</td><td>D</td><td>IR</td><td>IQ</td><td>T</td><td>P</td><td colspan="2">-</td><td>Memory-mapped I/O configuration
• I = 0: No interface byte
• D = 0: No default entry
• Configuration index = 0</td><td>Configuration table index byte TPCE_INDX</td></tr>
<tr><td>72h</td><td>01h</td><td>M</td><td>MS</td><td>IR</td><td>IO</td><td>T</td><td>P</td><td colspan="2">-</td><td>• M = 0: No miscellaneous information
• MS = 00: No memory space information
• IR = 0: No interrupt information present
• IO = 0: No I/O port information present
• T = 0: No timing information present
• P = 1: V_{CC} only information</td><td>Feature selection byte TPCE_FS</td></tr>
<tr><td>74h</td><td>21h</td><td>R</td><td>DI</td><td>PI</td><td>AI</td><td>SI</td><td colspan="3">HV/LV/NV</td><td>Nominal voltage only follows
• R: Reserved
• DI: Powerdown current information
• PI: Peak current information
• AI: Average current information
• SI: Static current information
• HV: Maximum voltage information
• LV: Minimum voltage information
• NV: Nominal voltage information</td><td>Power parameters for V_{CC}</td></tr>
<tr><td>76h</td><td>B5h</td><td>X</td><td colspan="3">Mantissa</td><td colspan="4">Exponent</td><td>Nominal voltage = 3.0 V</td><td>V_{CC} nominal value</td></tr>
<tr><td>78h</td><td>1Eh</td><td colspan="8">Extension</td><td>+0.3 V</td><td>Extension byte</td></tr>
<tr><td>7Ah</td><td>4Dh</td><td>X</td><td colspan="3">Mantissa</td><td colspan="4">Exponent</td><td>Maximum average current over 10ms is 45 mA</td><td>Maximum average current</td></tr>
<tr><td>7Ch</td><td>1Bh</td><td colspan="8">CISTPL_TABLE_ENTRY</td><td>Configuration table entry tuple</td><td>Tuple code</td></tr>
<tr><td>7Eh</td><td>0Dh</td><td colspan="8">TPL_LINK</td><td>Link length is 10 bytes</td><td>Link to next tuple</td></tr>
<tr><td>80h</td><td>C1h</td><td>I</td><td>D</td><td colspan="3">Configuration</td><td colspan="3">INDEX</td><td>Contiguous I/O mapped ATA registers configuration
• I = 1: Interface byte follows
• D = 1: Default entry
• Configuration index = 1</td><td>Configuration table index byte TPCE_INDX</td></tr>
<tr><td>82h</td><td>41h</td><td>W</td><td>R</td><td>P</td><td>B</td><td colspan="4">Interface Type</td><td>• W = 0: Wait not used
• R = 1: Ready active
• P = 0: WP not used
• B = 0: BVS1 and BVD2 not used
• IF type = 1: I/O interface</td><td>Interface description field TPCE_IF</td></tr>
<tr><td>84h</td><td>99h</td><td>M</td><td>MS</td><td>IR</td><td>IO</td><td>T</td><td>P</td><td colspan="2">-</td><td>• M = 1: Miscellaneous information present
• MS = 00: No memory space information
• IR = 1: Interrupt information present
• IO = 1: I/O port information present
• T = 0: No timing information present
• P = 1: V_{CC} only information</td><td>Feature selection byte TPCE_FS</td></tr>
</table>

Table 20: Card Information Structure (Continued)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
86h	27h	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows • R: Reserved • DI: Powerdown current information • PI: Peak current information • AI: Average current information • SI: Static current information • HV: Maximum voltage information • LV: Minimum voltage information • NV: Nominal voltage information	Power parameters for V_{CC}
88h	55h	X	Mantissa			Exponent				Nominal voltage = 5V	V_{CC} nominal value
8Ah	4Dh	X	Mantissa			Exponent				V_{CC} nominal 4.5V	V_{CC} minimum value
8Ch	5Dh	X	Mantissa			Exponent				V_{CC} nominal 5.5V	V_{CC} maximum value
8Eh	75h	X	Mantissa			Exponent				Maximum average current over 10ms is 80mA	Maximum average current
90h	64h	R	S	E	I	O	AddrLine			• S = 1: 16-bit hosts supported • E = 1: 8-bit hosts supported • IO AddrLine: 4 lines decoded	I/O space description field TPCE_IO
92h	F0h	S	P	L	M	V	B	I	N	• S = 1: Share logic active • P = 1: Pulse mode IRQ supported • L = 1: Level mode IRQ supported • M = 1: Bit mask of IRQs present • V = 0: No vender unique IRQ • B = 0: No bus error IRQ • I = 0: No IO check IRQ • N = 0: No NMI	Interrupt request description structure TPCE_IR
94h	FFh	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0	SiliconSystems recommends the IRQ level to be routed 0 to 15	Mask extension byte 1 TPCE_IR
96h	FFh	IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10	IRQ9	IRQ8	SiliconSystems recommends routing to any normal, maskable IRQ.	Mask extension byte 2 TPCE_IR
98h	21h	X	R	P	R	O	A	T	-	• X = 0: No more miscellaneous fields • R: Reserved • P = 1: Powerdown supported • RO = 0: Not read only mode • A = 0: Audio not supported • T = 0: Single drive	Miscellaneous features field TPCE_MI
9Ah	1Bh	CISTPL__TABLE_ENTRY								Configuration table entry tuple	Tuple code
9Ch	06h	TPL_LINK								Link length is 6 bytes	Link to next tuple
9Eh	01h	I	D	Configuration Index						Contiguous I/O mapped ATA registers configuration • I = 0: No Interface byte • D = 0: No Default entry • Configuration index = 1	Configuration table index Byte TPCE_INDX

Table 20: Card Information Structure (Continued)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
A0h	01h	M	MS	IR	IO	T	P	-		• M = 0: No miscellaneous information • MS = 00: No memory space information • IR = 0: No interrupt information present • IO = 0: No I/O port information present • T = 0: No timing information present • P = 1: V_{CC} only information	Feature selection byte TPCE_FS
A2h	21h	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows • R: Reserved • DI: Powerdown current information • PI: Peak current information • AI: Average current information • SI: Static current information • HV: Maximum voltage information • LV: Minimum voltage information • NV: Nominal voltage information	Power parameters for V_{CC}
A4h	B5h	X	Mantissa			Exponent				Nominal voltage = 3.0V	V_{CC} nominal value
A6h	1Eh	X	Mantissa			Exponent				+0.3V	Extension byte
A8h	4Dh	X	Mantissa			Exponent				Maximum average current over 10ms is 45mA	Maximum average current
AAh	1Bh	CISTPL_TABLE_ENTRY								Configuration table entry tuple	Extension byte
ACh	12h	TPL_LINK								Link length is 18 bytes	Link to next tuple
AEh	C2h	I	D	Configuration Index						ATA primary I/O mapped configuration • I = 1: Interface byte follows • D = 1: default entry follows • Configuration index = 2	Configuration table index byte TPCE_INDX
B0h	41h	W	R	P	B	Interface Type				• W = 0: Wait not used • R = 1: Ready active • P = 0: WP not used • B = 0: BVS1 and BVD2 not used • IF type = 1: I/O interface	Interface description field TPCE_IF
B2h	99h	M	MS	IR	IO	T	P	-		• M = 1: Miscellaneous information present • MS = 00: No memory space information • IR = 1: Interrupt information present • IO = 1: I/O port information present • T = 0: No timing information present • P = 1: V_{CC} only information	Feature selection byte TPCE_FS
B4h	27h	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows • R: Reserved • DI: Powerdown current information • PI: Peak current information • AI: Average current information • SI: Static current information • HV: Maximum voltage information • LV: Minimum voltage information • NV: Nominal voltage information	Power parameters for V_{CC}

Table 20: Card Information Structure (Continued)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
B6h	55h	X	Mantissa			Exponent				Nominal voltage = 5V	V_{CC} nominal value
B8h	4Dh	X	Mantissa			Exponent				V_{CC} nominal 4.5V	V_{CC} minimum value
BAh	5Dh	X	Mantissa			Exponent				V_{CC} nominal 5.5V	V_{CC} maximum value
BCh	75h	X	Mantissa			Exponent				Maximum average current over 10ms is 80mA	Maximum average current
BEh	EAh	R	S	E	I	O	AddrLine			• R = 1: Range follows • S = 1: 16-bit hosts supported • E = 1: 8-bit hosts supported IO AddrLines: 10 lines decoded	I/O space description field TPCE_IO
C0h	61h	LS	AS	N Range						• LS = 1: Size of lengths is 1 byte • AS = 2: Size of address is 2 bytes • N Range = 1: Address Range-1	I/O range format description
C2h	F0h	First I/0 Base Address								First I/O base address (LSB)	First I/O range address
C4h	01h	First I/0 Base Address								First I/O base address (MSB)	-
C6h	07h	First I/0 Base Address								First I/O length -1	First I/O range length
C8h	F6h	Second I/O Base Address								Second I/O base address (LSB)	Second I/O range address
CAh	03h	Second I/O Base Address								Second I/O base address (MSB)	
CCh	01h	Second I/O Range Length								Second I/O length -1	Second I/O range length
CEh	EEh	S	P	L	M	IRQ	Level			• S = 1: Share logic active • P = 1: Pulse mode IRQ supported • L = 1: Level mode IRQ supported • M = 0: Bit mask of IRQs present — IRQ level is IRQ14	Interrupt request description structure TPCE_IR
D0h	21h	X	R	P	R	O	A	T	-	• X = 0: No more miscellaneous fields • R: Reserved • P = 1: Powerdown supported • RO = 0: Not read only mode • A = 0: Audio not supported • T = 0: Single drive	Miscellaneous features field TPCE_MI
D2h	1Bh	CISTPL_TABLE_ENTRY								Configuration table entry tuple	Tuple code
D4h	06h	TPL_LINK								Link length is 6 bytes	Link to next tuple
D6h	02h	I	D	Configuration Index						ATA primary I/O mapped configuration • I = 0: No Interface byte • D = 0: No Default entry • Configuration index = 2	Configuration table index byte TPCE_INDX
D8h	01h	I	D	Configuration Index						Contiguous I/O mapped ATA registers configuration • I = 0: No interface byte • D = 0: No default entry • Configuration index = 1	Configuration table index byte TPCE_INDX

Table 20: Card Information Structure (Continued)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
DAh	21h	M	MS	IR	IO	T	P	-		• M = 0: No miscellaneous information • MS = 00: No memory space information • IR = 0: No interrupt information present • IO = 0: No I/O port information present • T = 0: No timing information present • P = 1: V_{CC} only information	Feature selection byte TPCE_FS
DCh	B5h	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows • R: Reserved • DI: Powerdown current information • PI: Peak current information • AI: Average current information • SI: Static current information • HV: Maximum voltage information • LV: Minimum voltage information • NV: Nominal voltage information	Power parameters for V_{CC}
DEh	1Eh	X	Mantissa			Exponent				Nominal voltage = 3.0V	V_{CC} nominal value
E0h	4Dh	Extension								+0.3V	Extension byte
E2h	1Bh	CISTPL_TABLE_ENTRY								Configuration table entry tuple	Tuple code
E4h	12h	TPL_LINK								Link length is 18 bytes	Link to next tuple
E6h	C3h	M	MS	IR	IO	T	P	-		• M = 0: No miscellaneous information • MS = 00: No memory space information • IR = 0: No interrupt information present • IO = 0: No I/O port information present • T = 0: No timing information present • P = 1: V_{CC} only information	Feature selection byte TPCE_FS
E8h	41h	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows • R: Reserved • DI: Powerdown current information • PI: Peak current information • AI: Average current information • SI: Static current information • HV: Maximum voltage information • LV: Minimum voltage information • NV: Nominal voltage information	Power parameters for V_{CC}
EAh	99h	M	MS	IR	IO	T	P	-		• M = 1: No miscellaneous information • MS = 00: No Memory space information • IR = 1: No interrupt information present • IO = 1: No I/O port information present • T = 0: No timing information present • P = 01: V_{CC} only information	Feature selection byte TPCE_FS

Table 20: Card Information Structure (Continued)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
ECh	27h	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows • R: Reserved • DI: Powerdown current information • PI: Peak current information • AI: Average current information • SI: Static current information • HV: Maximum voltage information • LV: Minimum voltage information • NV: Nominal voltage information	Power parameters for V_{CC}
EEh	55h	X	Mantissa			Exponent				Nominal voltage = 5V	V_{CC} nominal value
F0h	4Dh	X	Mantissa			Exponent				V_{CC} nominal 4.5V	V_{CC} minimum value
F2h	5Dh	X	Mantissa			Exponent				V_{CC} nominal 5.5V	V_{CC} maximum value
F4h	75h	X	Mantissa			Exponent				Maximum average current over 10ms is 80mA	Maximum average current
F6h	EAh	R	S	E	I	O	AddrLine			• R = 1: Range follows • S = 1: 16-bit hosts supported • E = 1: 8-bit hosts supported • IO AddrLines: 10 lines decoded	I/O space description field TPCE_IO
F8h	61h	LS	AS	N Range						• LS = 1: Size of lengths is 1 byte • AS = 2: Size of address is 2 bytes • N Range = 1: Address range -1	I/O range format description
FAh	70h	-								First I/O base address (LSB)	First I/O range address
FCh	01h	-								First I/O base address (MSB)	-
FEh	07h	-								First I/O length -1	First I/O range length
100h	76h	-								Second I/O base address (LSB)	Second I/O range address
102h	03h	-								Second I/O base address (MSB)	-
104h	01h	-								Second I/O length	Second I/O range length
106h	EEh	S	P	L	M	IRQ	Level			• S = 1: Share logic active • P = 1: Pulse mode IRQ supported • L = 1: Level mode IRQ supported • M = 0: Bit mask of IRQs present — IRQ level is IRQ14	Interrupt request description structure TPCE_IR miscellaneous features field TPCE_MI
108h	21h	X	R	P	R	O	A	T	-	• X = 0: No more miscellaneous fields • R: Reserved • P = 1: Powerdown supported • RO = 0: Not read only mode • A = 0: Audio not supported • T = 0: Single drive	-
10Ah	1Bh	CISTPL_TABLE_ENTRY								Configuration table entry tuple	Tuple code
10Ch	06h	TPL_LINK								Link length is 6 bytes	Link to next tuple

Table 20: Card Information Structure (Continued)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
10Eh	03h	I	D	Configuration Index						ATA primary I/O mapped configuration • I = 0: No interface byte • D = 0: No default entry • Configuration index = 2	Configuration table index byte TPCE_INDX
110h	01h	M	MS	IR	IO	T	P	-		• M = 0: No miscellaneous information • MS = 00: No memory space information • IR = 0: No interrupt information present • IO = 0: No I/O port information present • T = 0: No timing information present • P = 1: V_{CC} only information	Feature selection byte TPCE_FS
112h	21h	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows • R: Reserved • DI: Powerdown current information • PI: Peak current information • AI: Average current information • SI: Static current information • HV: Maximum voltage information • LV: Minimum voltage information • NV: Nominal voltage information	Power parameters for V_{CC}
114h	B5h	X	Mantissa				Exponent			Nominal voltage = 3.0V	V_{CC} nominal value
116h	1Eh	Extension								+0.3V	Extension byte
118h	4Dh	X	Mantissa				Exponent			Maximum average current over 10ms is 45mA	Maximum average current
11Ah	1Bh	CISTPL_MANFID								Manufacturer's ID code	Tuple code
11Ch	04h	TPL_LINK								Link length is 4 bytes	Link to next tuple
11Eh	07h	I	D	Configuration Index						AT fixed disk secondary I/O 3.3V configuration	TPCE_INDX
120h	00h	M	MS	IR	IO	T	P	-		P: Power information type	TPCL_FS
122h	28h	-								Manufacturer code for SiliconDrive II CF	Reserved
124h	D3h	-								Manufacturer code for SiliconDrive II CF	Reserved
126h	14h	CISTPL_NO_LINK								No link control tuple	Tuple code
128h	00h	-								Link is 0 bytes	Link to next tuple
12Ah	15h	CISTPL_VERS_1								Level 1 version	Tuple code
12Ch	1Ah	TPL_LINK								Link length is 26h bytes	Link to next tuple
12Eh	04h	TPPLV1_MAJOR								PC Card 2.0/JEIDA4.1	END marker
130h	01h	TPPLV1_MINOR								PC Card 2.0/JEIDA4.1	Tuple code
132h	53h	-								S	Information string
134h	49h	-								I	-
136h	4Ch	-								L	-
138h	49h	-								I	-
13Ah	43h	-								C	-

Table 20: Card Information Structure (Continued)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
13Ch	4Fh	-								O	-
13Eh	4Eh	-								N	-
140h	53h	-								S	-
142h	59h	-								Y	-
144h	53h	-								S	-
146h	54h	-								T	-
	45h	-								E	-
14Ah	4Dh	-								M	-
14Ch	53h	-								S	-
14Eh	00h	-								Space	-
150h	56h	-								V	-
152h	45h	-								E	-
154h	52h	-								R	-
156h	32h	-								2	-
158h	2Eh	-								-	-
15Ah	30h	-								0	-
15Ch	30h	-								0	-
	00h	-								-	-
160h	FFh	-								-	-

CONFIGURATION OPTION REGISTER (200H)

The Configuration Option register is used to configure the SiliconDrive II CF, define the address decoding, and initiate the software RESET sequence.

Table 21: Configuration Option Register (200h)

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/ Write	SRESET	LevIREQ	Configuration Index					
Default Value	0	0	0	0	0	0	0	0

Bit(s)	Description
SRESET	When set, this bit initiates a software-reset sequence, which is equivalent to a power-on reset or hardware reset.
LevIREQ	IREQ# interrupt signal level mode select: • Logic 0 = Pulse mode • Logic 1 = Level mode
Configuration Index	• Memory-mapped mode 000000B • Independent I/O mode 000001B • Primary mode 000010B • Secondary mode 000011B

CONFIGURATION AND STATUS REGISTER (202H)

The Configuration and Status Register (CSR) informs the host of any status changes with regard to power-down.

Table 22: Configuration and Status Register (202h)

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read	Changed	SigChg	IOis8	0	0	PwrDn	Int	0
Write	Changed	SigChg	IOis8	0	0	PwrDn	Int	0
Default Value	0	0	0	0	0	0	0	0

Bit(s)	Description
Changed	Indicates that either CREADY (D5) or CWPort (D4) of the Pin Replacement register is set. Additionally, this bit changes state as the Powerdown (D2) bit changes.
SigChg	Outputs the inverse state of the Changed bit to the hardware interface signal STSCHG# at the card interface.
Iois8	Informs the host of the valid data bus width for the operations in progress: • 0 = 16-bit data transfer • 1 = 8-bit data transfer
PwrDwn	Indicates the state of the Card, which is either operating -0 or powerdown mode 1. During powerdown mode, no commands are accepted. Additionally, the host may not initiate a powerdown request when the card is busy via the Status register or the Hardware RDY/BSY pin.
Int	Indicates the inverse of the IREQ# status signal.

PIN PLACEMENT REGISTER (204H)

Table 23: Pin Placement Register (204h)

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/ Write	CBVD1	CBVD2	CRDY	CWProt	RBVD1	RBVD2	RRDY	RWProt
Default Value	0	0	0	0	1	1	0	0

Bit(s)	Description
CRDY	Indicates a bit change in the RRDY (D1) bit.
CWProt	Indicates a bit change in the RWProt (D0) bit.
RRDY	When set: • High 1 informs the host that the card is ready • Low 0 state indicates the card is busy
RWProt	Indicates Write Protect is enabled when set to 1, and disabled when 0.

SOCKET AND COPY REGISTER (206H)

Table 24: Socket and Copy Register (206h)

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	RFU	Copy Number			Socket Number			
Default Value	0	0	0	0	0	0	0	0

Bit(s)	Description
RFU	Reserved for future use.
Copy Number	Indicates the card number. Allows the host to differentiate between identical cards by writing to the bit of the card that is being accessed. This value is compared to the DRV bit in the ATA Drive/Head register. • Card 0: 000B = (D6, D5, D4) (default) • Card 1: 001B = (D6, D5, D4) (alternate)
Socket Number	The host writes the socket number that identifies the inserted card.

COMMON MEMORY DESCRIPTION AND OPERATION

Common memory space can be accessed when the SiliconDrive II is configured in memory-mapped mode.

COMMON MEMORY READ OPERATIONS

Common memory read operations are issued by asserting CE1#, CE2#, or both, and OE# low, REG#, and WE# must be inactive.

Table 25: Common Memory Read Operations

Function Mode	REG#	CE1#	CE2#	A0	OE#	WE#	D[15:8]	D[7:0]
Standby	X	H	H	X	X	X	High-Z	High-Z
Byte Access	H	L	H	L	L	H	High-Z	Even
	H	L	H	H	L	H	High-Z	Odd
Word Access	H	L	L	X	L	H	Odd	Even
Odd Byte Only Access	H	H	L	X	L	H	Odd	High-Z

COMMON MEMORY WRITE OPERATIONS

Common memory write operations are issued by asserting CE1#, CE2#, or both, and WE# low, REG#, and OE# must be inactive.

Table 26: Common Memory Write Operations

Function Mode	REG#	CE1#	CE2#	A0	OE#	WE#	D[15:8]	D[7:0]
Standby	X	H	H	X	X	X	High-Z	High-Z
Byte Access	H	L	H	L	H	L	High-Z	Even
	H	L	H	H	H	L	High-Z	Odd
Word Access	H	L	L	X	H	L	Odd	Even
Odd Byte Only Access	H	H	L	X	H	L	Odd	High-Z

I/O SPACE DESCRIPTION AND OPERATION

I/O SPACE READ OPERATIONS

Table 27: I/O Space Read Operations

Function Mode	REG#	CE1#	CE2#	A0	IORD#	IOWR#	D[15:8]	D[7:0]
Standby	X	H	H	X	X	X	High-Z	High-Z
Byte Access	L	L	H	L	L	H	High-Z	Even
	L	L	H	H	L	H	High-Z	Odd
Word Access	L	L	L	L	L	H	Odd	Even
I/O Inhibit	H	X	X	X	L	H	High-Z	High-Z
Odd Byte Only Access	L	H	L	X	L	H	Odd	High-Z

I/O SPACE WRITE OPERATIONS

Table 28: I/O Space Write Operations

Function Mode	REG#	CE1#	CE2#	A0	IORD#	IOWR#	D[15:8]	D[7:0]
Standby	X	H	H	X	X	X	X	X
Byte Access	L	L	H	L	H	L	X	Even
	L	L	H	H	H	L	X	Odd
Word Access	L	L	L	L	H	L	Odd	Even
I/O Inhibit	H	X	X	X	H	L	X	X
Odd Byte Only Access	L	H	L	X	H	L	Odd	X

ATA AND TRUE IDE REGISTER DECODING

SiliconDrive II can be configured as either a a memory-mapped or an an I/O devices. As noted earlier, communication to and from the drive is accomplished using the ATA Command Block.

MEMORY-MAPPED REGISTER DECODING

In memory-mapped mode, the SiliconDrive II registers are accessed via standard memory references (i.e., OE# and WE#). The ATA registers are mapped to common memory space in a 2KB window starting at address 0.

Table 29: Memory-Mapped Register Decoding

Reg#	Offset	A10	A9:A4	A3	A2	A1	A0	OE# = L	WE# = L
1	0	0	X	0	0	0	0	Even Data Read	Even Data Write
1	1	0	X	0	0	0	1	Error	Feature
1	2	0	X	0	0	1	0	Sector Count	Sector Count
1	3	0	X	0	0	1	1	Sector Number	Sector Number
1	4	0	X	0	1	0	0	Cylinder Low	Cylinder Low
1	5	0	X	0	1	0	1	Cylinder High	Cylinder High
1	6	0	X	0	1	1	0	Drive/Head	Drive/Head
1	7	0	X	0	1	1	1	Status	Command
1	8	0	X	1	0	0	0	Duplicate Even Data Read	Duplicate Even Data Write
1	9	0	X	1	0	0	1	Duplicate Odd Data Read	Duplicate Odd Data Write
1	D	0	X	1	1	0	1	Duplicate Error	Duplicate Feature
1	E	0	X	1	1	1	0	Alternate Status	Device Control
1	F	0	X	1	1	1	1	Drive Address	Reserved
1	X	1	X	X	X	X	0	Even Data Read	Even Data Write
1	X	1	X	X	X	X	1	Odd Data Read	Odd Data Write

INDEPENDENT I/O MODE REGISTER DECODING

Independent I/O mode or contiguous I/O mode requires the host to decode a continuous block of 16 I/O registers to select the SiliconDrive II.

Table 30: Independent I/O Mode Register Decoding

Reg#	Offset	A10	A9:A4	A3	A2	A1	A0	OE# = L	WE# = L
0	0	X	X	0	0	0	0	Even Data Read	Even Data Write
0	1	X	X	0	0	0	1	Error	Feature
0	2	X	X	0	0	1	0	Sector Count	Sector Count
0	3	X	X	0	0	1	1	Sector Number	Sector Number
0	4	X	X	0	1	0	0	Cylinder Low	Cylinder Low
0	5	X	X	0	1	0	1	Cylinder High	Cylinder High
0	6	X	X	0	1	1	0	Drive/Head	Drive/Head
0	7	X	X	0	1	1	1	Status	Command
0	8	X	X	1	0	0	0	Duplicate Even Data Read	Duplicate Even Data Write
0	9	X	X	1	0	0	1	Duplicate Odd Data Read	Duplicate Odd Data Write
0	D	X	X	1	1	0	1	Duplicate Error	Duplicate Feature
0	E	X	X	1	1	1	0	Alternate Status	Device Control
0	F	X	X	1	1	1	1	Drive Address	Reserved

PRIMARY AND SECONDARY I/O MAPPED REGISTER DECODING

Table 31: Primary and Secondary I/O Mapped Register Decoding

Reg#	A10	A9:A4 Primary	A9:A4 Secondary	A3	A2	A1	A0	IORD# = L	IOWR# = L
0	X	1Fxh	17xh	0	0	0	0	Even Data Read	Even Data Write
0	X	1Fxh	17xh	0	0	0	1	Error	Feature
0	X	1Fxh	17xh	0	0	1	0	Sector Count	Sector Count
0	X	1Fxh	17xh	0	0	1	1	Sector Number	Sector Number
0	X	1Fxh	17xh	0	1	0	0	Cylinder Low	Cylinder Low
0	X	1Fxh	17xh	0	1	0	1	Cylinder High	Cylinder High
0	X	1Fxh	17xh	0	1	1	0	Drive/Head	Drive/Head
0	X	1Fxh	17xh	0	1	1	1	Status	Command
0	X	3Fxh	37xh	0	1	1	0	Alternate Status	Device Control
0	X	3Fxh	37xh	0	1	1	1	Drive Address	Reserved

TASK FILE REGISTER SPECIFICATION

The Task File registers are used for reading and writing the storage data in the SiliconDrive II. The decoded addresses are as shown in the following table.

Table 32: Task File Register Specification

CS0#	CS1#	DA02	DA01	DA00	DIOR# = L	DIOW# = L
0	1	0	0	0	Data	Data
0	1	0	0	1	Error	Feature
0	1	0	1	0	Sector Count	Sector Count
0	1	0	1	1	Sector Number	Sector Number
0	1	1	0	0	Cylinder Low	Cylinder Low
0	1	1	0	1	Cylinder High	Cylinder High
0	1	1	1	0	Drive/Head	Drive/Head
0	1	1	1	1	Status	Command
0	0	X	X	X	Invalid	Invalid
1	1	X	X	X	High-Z	Not Used
1	0	0	X	X	High-Z	Not Used
1	0	1	0	X	High-Z	Not Used
1	0	1	1	0	Alternate Status	Device Control
1	0	1	1	1	Device Address	Not Used

ATA REGISTERS

DATA REGISTER

The Data register is a 16-bit register used to transfer data blocks between the host and drive buffers. The register may set to 8-bit mode by using the Set Features Command defined in "Seek — 7Xh" on page 92.

ERROR REGISTER

The Error register contains the error status, if any, generated from the last executed ATA command. The contents are qualified by the ERR bit being set in "Status Register" on page 68.

Table 33: Error Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read	BBK	UNC	MC	IDNF	MCR	ABRT	TKNOF	AMNF
Default Value	0	0	0	0	0	0	0	0

Bit(s)	Description
7	**Bad Block Detected (BBK).** Set when a bad block is detected.
6	**Uncorrectable Data Error (UNC).** Set when an uncorrectable error is encountered.
5	**Media Changed (MC).** Set to 0.
4	**ID Not Found (IDNF).** Set when the sector ID is not found.
3	**MCR (Media Change Request).** Set to 0.
2	**Aborted Command (ABRT).** Set when a command is aborted due to a drive error.
1	**Track 0 Not Found (TKONF).** Set when the executive drive diagnostic command is executed.
0	**Address Mark Not Found (AMNF).** Set in the case of a general error.

FEATURE REGISTER

The Feature register is command-specific and used to enable and disable interface features. This register supports only either odd or even byte data transfers.

Table 34: Feature Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	Feature Byte							

SECTOR COUNT REGISTER

The Sector Count register is used to read or write the sector count of the data for which an ATA transfer has been made.

Table 35: Sector Count Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	Sector Count							
Default Value	0	0	0	0	0	0	0	1

SECTOR NUMBER REGISTER

The Sector Number register is set by the host to specify the starting sector number associated with the next ATA command to be executed. Following a qualified ATA command sequence, the device sets the register value to the last sector read or written as a result of the previous AT command.

When Logical Block Addressing (LBA) mode is implemented and the host issues a command, the contents of the register describe the Logical Block Number bits A[7:0]. Following an ATA command, the device loads the register with the LBA block number resulting from the last ATA command.

Table 36: Sector Number Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	Sector Number (CHS Addressing)							
	Logical Block Number bits A07-A00 (LBA Addressing)							
Default Value	0	0	0	0	0	0	0	1

CYLINDER LOW REGISTER

The Cylinder Low register is set by the host to specify the cylinder number low byte. Following an ATA command, the content of the register is written by the device, identifying the cylinder number low byte.

In LBA mode, the 8-bit register maintains the contents of the Logical Block number address bits A15:A08.

Table 37: Cylinder Low Register

Operation	**D_7**	**D_6**	**D_5**	**D_4**	**D_3**	**D_2**	**D_1**	**D_0**
Read/Write	Cylinder Number Low Byte (CHS Addressing)							
	Logical Block Number bits A15-A08 (LBA Addressing)							
Default Value	0	0	0	0	0	0	0	0

CYLINDER HIGH REGISTER

The Cylinder High register is set by the host to specify the cylinder number high byte. Following an ATA command, the content of the register is set internally by the device, identifying the cylinder number high byte.

In LBA mode, the 8-bit register maintains the contents of the Logical Block number address bits A23:A16.

Table 38: Cylinder High Register

Operation	**D_7**	**D_6**	**D_5**	**D_4**	**D_3**	**D_2**	**D_1**	**D_0**
Read/Write	Cylinder Number Low Byte (CHS Addressing)							
	Logical Block Number bits A23-A16 (LBA Addressing)							
Default Value	0	0	0	0	0	0	0	0

DRIVE/HEAD REGISTER

The Drive/Head register is used by the host and the device to select the type of addressing (CHS or LBA), the drive letter, and either bits 3-0 of the head number in CHS mode or logical block number bits 27-24 in LBA mode.

Table 39: Drive/Head Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	1	LBA	1	DRV	HS3 LBA27	HS2 LBA26	HS1 LBA25	HS0 LBA24
Default Value	1	0	1	0	0	0	0	0

The Drive/Head register is used by the host to specify one of a pair of ATA drives present in the platform.

Bit(s)	Description
6	**LBA.** Selects between CHS (0) and LBA (1) addressing mode.
4	**Drive Address (DRV).** Indicates the drive number selected by the host, either 0 or 1.
3-0	HS3 to 0. Indicates bits 3-0 of the head number in CHS addressing mode or LBA bits 27-24 in LBA mode. • CHS to LBA conversion: LBA = (C x HpC + H) x SpH + S -1 • LBA to CHS conversion: ○ C = LBA/(HpC x SpH) ○ H = (LBA/SpH) mod (HpC) ○ S = (LBA mod(SpH)) + 1 ...where: ○ C is the cylinder number ○ H is the head number ○ S is the sector count ○ HpC is the head count per cylinder count ○ SpH is the sector count per head count (track)

STATUS REGISTER

The Status register provides the device's current status to the host. The status register is an 8-bit read-only register. When the contents of the register are read by the host, the IREQ# bit is cleared.

Table 40: Status Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
Default Value	0	0	0	0	0	0	0	0

Bit(s)	Description
7	**Busy (BSY).** Set when the drive is busy and unable to process any new ATA commands.
6	**Data Ready (DRDY).** Set when the device is ready to accept ATA commands from the host.
5	**Drive Write Fault (DWF).** Always set to 0.
4	**Drive Seek Complete (DSC).** Set when the drive heads have been positioned over a specific track.
3	**Data Request (DRQ).** Set when a device is ready to transfer a word or byte of data to or from the host and the device.
2	**Corrected Data (CORR).** Always set to 0.
1	**Index (IDX).** Always set to 0.
0	**Error (ERR).** Set when an error occurs during the previous ATA command.

COMMAND REGISTER

The Command register specifies the ATA command code being issued to the drive by the host. Execution of the command begins immediately following the issuance of the command register code by the host.

Table 41: Command Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	ATA Command Code							

See "ATA Command Block and Set Description" on page 73 for a listing of the supported ATA commands.

ALTERNATE STATUS REGISTER

The Alternate Status register is a read-only register indicating the status of the device, following the previous ATA command. See "Status Register" on page 68 for specific details.

Table 42: Alternate Status Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
Default Value	0	0	0	0	0	0	0	0

DEVICE CONTROL REGISTER

The Device Control register is used to control the interrupt request and issue ATA software resets.

Table 43: Device Control Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Write	-	-	-	-	1	SRST	nIEN	0

Bit(s)	Description
7-4	Reserved bits.
3	Always set to 1.
2	**Software Reset (SRST).** When set, resets the ATA software.
1	**Interrupt Enable (nIEN).** When set, device interrupts are disabled. There is no function in the memory-mapped mode.
0	Always set to 0.

DEVICE ADDRESS REGISTER

The Device Address register is used to maintain compatibility with ATA disk drive interfaces.

Table 44: Device Address Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	-	nWTG	nHS3	nHS2	nHS1	nHS0	nDS1	nDS0
Default Value	0	0	1	1	1	1	1	0

Bit(s)	Description
7	Reserved bit.
6	**Write Gate (nWTG).** Low when a write to the device is in process.
5-2	**nHS3 to nHS0.** The negated binary address of the currently selected head.
1	**nDS1.** Low when drive 1 is selected and active.
0	**nDS0.** Low when drive 0 is selected and active.

ATA COMMAND BLOCK AND SET DESCRIPTION

In accordance with the *ANSI ATA Specification*, the device implements seven registers that are used to transfer instructions to the device by the host. These commands follow the ANSI standard ATA protocol. A description of the ATA command block is provided in the following table.

Table 45: ATA Command Block and Set Description

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	1	LBA	1	Drive	X			
Command	X							

ATA COMMAND SET

Table 46: ATA Command Set

Class	Command Name	Command Code	Registers Used					
			FR	SC	SN	CY	DH	LBA
1	Check Power Mode	98h, E5h	-	-	-	-	D	-
1	Execute Drive Diagnostics	90h	-	-	-	-	D	-
1	Erase Sector	C0h	-	Y	Y	Y	Y	Y
2	Format Track	50h	-	Y	-	Y	Y	Y
1	Identify Drive	ECh	-	-	-	-	D	-
1	Idle	97h, E3h	-	Y	-	-	D	-
1	Idle Immediate	95h, E1h	-		-	-	D	-
1	Initialize Drive Parameters	91h	-	Y	-	-	Y	-
1	Read Buffer	E4h	-	-	-	-	D	-
1	Read DMA*	C8h	-	Y	Y	Y	Y	Y
1	Read Multiple	C4h	-	Y	Y	Y	Y	Y

Table 46: ATA Command Set (Continued)

Class	Command Name	Command Code	Registers Used					
			FR	SC	SN	CY	DH	LBA
1	Read Long Sector	22h, 23h	-	-	Y	Y	Y	Y
1	Read Sector(s)	20h, 21h	-	-	Y	Y	Y	Y
1	Read Verify Sector(s)	40h, 41h	-	Y	Y	Y	Y	Y
1	Recalibrate	1Xh	-	-	-	-	Y	-
1	Request Sense	03h	-	-	-	-	D	-
1	Seek	7Xh	-	-	Y	Y	Y	Y
1	Set Features	EFh	Y		-	-	D	-
1	Set Multiple Mode	C6h	-	Y	-	-	D	-
1	Set Sleep Mode	99h, E6h	-	-	-	-	D	-
1	Standby	96h, E2h	-	-	-	-	D	-
1	Standby Immediate	94h, E0h	-	-	-	-	D	-
1	Translate Sector	87h	-	Y	Y	Y	Y	Y
1	Wear Level	F5h	-	-	-	-	Y	-
2	Write Buffer	E8h	-	-	-	-	D	-
1	Write DMA*	CAh	-	Y	Y	Y	Y	Y
2	Write Long Sector	32h, 33h	-		Y	Y	Y	Y
3	Write Multiple	C5h	-	Y	Y	Y	Y	Y
3	Write Multiple w/o Erase	CDh	-	Y	Y	Y	Y	Y
2	Write Sector(s)	30h, 31h	-	Y	Y	Y	Y	Y
2	Write Sector(s) w/o Erase	38h	-	Y	Y	Y	Y	Y
3	Write Verify	3Ch	-	Y	Y	Y	Y	Y

* = This function does not apply to SiliconDrive IIs that have DMA disabled.

Notes:

- CY = Cylinder
- SC = Sector Count
- DH = Drive/Head
- SN = Sector Number
- FR = Feature LBA — LBA bit of the Drive/Head register (D denotes that only the drive bit is used)

Check Power Mode — 98h, E5h

The Check Power Mode command verifies the device's current power mode. When the device is configured for standby mode or is entering or exiting standby, the BSY bit is set, the Sector Count register set to 00h, and the BSY bit is cleared. In idle mode, BSY is set and the Sector Count register is set to FFh. The BSY bit is then cleared and an interrupt is issued.

Table 47: Check Power Mode — 98h, E5h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive				
Command	98h or E5h							

Executive Drive Diagnostic — 90h

The Executive Drive Diagnostic performs an internal read write diagnostic test using (AA55h and 55AAh). If an error is detected in the read/write buffer, the Error register reports the appropriate diagnostic code.

Table 48: Executive Drive Diagnostic — 90h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive				
Command	90h							

Format Track — 50h

The Format Track command formats the common solid-state memory array.

Table 49: Format Track — 50h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	50h							

Identify Drive — ECh

Issued by the host, the Identify Drive command provides 256 bytes of drive attribute data (i.e., sector size, count, and so on) The identify drive data structure is detailed in the following table.

Table 50: Identify Drive — ECh

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	ECh							

Identify Drive — Drive Attribute Data

Table 51: Identify Drive — Drive Attribute Data

Word Address	Data Default	Bytes	Data Description
0	044Ah (fixed ID bit) in IDE mode 848A (removable ID bit) in PCMCIA memory and I/O modes	2	General configuration bit information • 15: Non-magnetic disk • 14: Formatting speed latency permissible gap needed • 13: Track Offset option supported • 12: Data Strobe Offset option supported • 11: Over 0.5% rotational speed difference • 10: Disk transfer rate > 10Mbps • 9: 10Mbps >= disk transfer rate > 5Mbps • 8: 5Mbps >= disk transfer rate • 7: Removable cartridge drive • 6: Fixed drive • 5: Spindle Motor Control option executed • 4: Over 15μs changing head time • 3: Non-MFM encoding • 2: Soft sector allocation • 1: Hard sector allocation • 0: Reserved
1	XXXXh	2	Number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Number of heads
4	0000h	2	Number of unformatted bytes per track
5	XXXXh	2	Number of unformatted bytes per sector
6	XXXXh	2	Number of sectors per track
7-8	XXXXh	4	Number of sectors per device
9	0000h	2	Reserved
10-19	XXXXh	20	Serial number

Table 51: Identify Drive — Drive Attribute Data (Continued)

Word Address	Data Default	Bytes	Data Description
20	0002h	2	Buffer type • 0000h: Not specified • 0001h: A single-ported, single-sector buffer • 0002h: A dual-ported multisector buffer • 0003h: A dual-ported multisector buffer with a read caching
21	0002h	2	Buffer size in 512-byte increments
22	0004h	2	Number of ECC bytes passed on read/ write long commands
23-26	XXXXh	8	Firmware revision (eight ASCII characters)
27-46	XXXXh	40	Model number (40 ASCII characters)
47	8001h	2	15-8: Maximum number of sectors that can be transferred with a Read/Write Multiple command per interrupt
48	0000h	2	Double word (32 bit) not supported
49	0002h	2	• 11: IORDY supported • 9: LBA supported • 8: DMA supported
50	0000h	2	Reserved
51	0100h	2	15-8: PIO data transfer cycle timing
52	0000h	2	15-8: DMA data transfer cycle timing
53	0007h	2	• 2: Word 88 is valid • 1: Words 64-70 are valid • 0: Words 54-58 are valid
54	XXXXh	2	Current number of cylinders
55	XXXXh	2	Current number of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors
59	010Xh	2	7-0: Current sectors can be transferred with a Read/Write Multiple command per interrupt
60-61	XXXXh	4	Total number of sectors addressable in LBA mode

Table 51: Identify Drive — Drive Attribute Data (Continued)

Word Address	Data Default	Bytes	Data Description
62	0000h	2	Single-word DMA modes supported
63	0007h	2	• 2: Multiword DMA mode 2 supported • 1: Multiword DMA mode 1 supported • 0: Multiword DMA mode 0 supported
64	0003h	2	7-0: Advanced PIO modes supported
65	0078h	2	15-0: Multiword DMA cycle time in nanoseconds
66	0078h	2	15-0: Multiword DMA transfer cycle time in nanoseconds
67	0078h	2	15-0: PIO mode cycle time without flow control
68	0078h	2	15-0: PIO mode cycle time with IORDY flow control
80	003Eh	2	• 5: ATA/ATAPI-5 supported • 4: ATA/ATAPI-4 supported • 3: ATA-3 supported • 2: ATA-2 supported • 1: ATA-2 supported • 0: Reserved
88	001Fh	2	• 4: UDMA mode 4 supported • 3: UDMA mode 3 supported • 2: UDMA mode 2 supported • 1: UDMA mode 1 supported • 0: UDMA mode 0 supported
163	0002h	2	2: Multiword DMA mode 4 and PIO mode 6 supported

Idle — 97h, E3h

When issued by the host, the device’s internal controller sets the BSY bit, enters the Idle mode, clears the BSY bit, and generates an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5ms, and the automatic power-down mode is enabled. If the sector count is zero, the automatic power-down mode is disabled.

Table 52: Idle — 97h, E3h

<table>
<tr><th>Register</th><th>D_7</th><th>D_6</th><th>D_5</th><th>D_4</th><th>D_3</th><th>D_2</th><th>D_1</th><th>D_0</th></tr>
<tr><td>Feature</td><td colspan="8">X</td></tr>
<tr><td>Sector Count</td><td colspan="8">Timer Count (5ms increments)</td></tr>
<tr><td>Sector Number</td><td colspan="8">X</td></tr>
<tr><td>Cylinder Low</td><td colspan="8">X</td></tr>
<tr><td>Cylinder High</td><td colspan="8">X</td></tr>
<tr><td>Drive Head</td><td>X</td><td>X</td><td>X</td><td>Drive</td><td colspan="4">X</td></tr>
<tr><td>Command</td><td colspan="8">97h or E3h</td></tr>
</table>

Idle Immediate — 95h, E1h

When issued by the host, the device's internal controller sets the BSY bit, enters Idle Mode, clears the BSY bit, and issues an interrupt. The interrupt is issued whether or not the Idle mode is fully entered.

Table 53: Idle Immediate — 95h, E1h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	95h or E1h							

Initialize Drive Parameters — 91h

Initialize Drive Parameters allows the host to set the sector counts per track and the head counts per cylinder to 1 Fixed. Upon issuance of the command, the device sets the BSY bit and associated parameters, clears the BSY bit, and issues an interrupt.

Table 54: Initialize Drive Parameters — 91h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count (Number of Sectors)							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	0	X	Drive	Head Number (Number of Heads — 1)			
Command	91h							

Recalibrate — 1Xh

The Recalibrate command sets the cylinder low and high, head number to 0h, and sector number to 1h in CHS mode. In LBA mode (i.e., LBA = 1), the sector number is set to 0h.

Table 55: Recalibrate — 1Xh

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	1	LBA	1	Drive	X			
Command	1Xh							

Read Buffer — E4h

The Read Buffer command allows the host to read the contents of the sector buffer. When issued, the device sets the BSY bit and sets up the sector buffer data in preparation for the read operation. When the data is ready, the DRQ bit is set and the BSY bit in the Status register are set and cleared, respectively.

Table 56: Read Buffer — E4h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	E4h							

Read DMA — C8h

The Read DMA command allows the host to read data using the DMA transfer protocol.

> ***Note:*** This function does not apply to SiliconDrive IIs that have DMA disabled.

Table 57: Read DMA — C8h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	C8h							

Read Multiple — C4h

The Read Multiple command executes similarly to the Read Sector command, with the exception that interrupts are issued only when a block containing the counts of sectors defined by the Set Multiple command is transferred.

Table 58: Read Multiple — C4h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	C4h							

Read Sector — 20h, 21h

The Read Sector command allows the host to read sectors 1 to 256 as specified in the Sector Count register. If the sector count is set to 0h, all 256 sectors of data are made available. When the command code is issued and the first sector of data has been transferred to the buffer, the DRQ bit is set. The Read Sector command is terminated by writing the cylinder, head, and sector number of the last sector read in the task file. On error, the read operation is aborted in the errant sector.

Table 59: Read Sector — 20h, 21h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	20h or 21h							

Read Long Sector(s) — 22h, 23h

The Read Long Sector(s) command operates similarly to the Read Sector(s) command, with the exception that it transfers requested data sectors and ECC data. The long instruction ECC byte transfer for Long commands is a byte transfer at a fixed length of 4 bytes.

Table 60: Read Long Sector(s) — 22h, 23h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	22h or 23h							

Read Verify Sector(s) — 40h, 41h

The Read Verify Sector(s) command operates similarly to the Read Sector(s) command, with the exception that is does not set the DRQ bit and does not transfer data to the host. When the requested sectors are verified, the onboard controller clears the BSY bit and issues an interrupt.

Table 61: Read Verify Sector(s) — 40h, 41h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	40h or 41h							

Seek — 7Xh

The Seek command seeks and picks up the head to the tracks specified in the task file. When the command is issued, the solid-state memory chips do not need to be formatted. After an appropriate amount of time, the DSC bit is set.

Table 62: Seek — 7Xh

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	7Xh							

Set Features — EFh

The Set Features command allows the host to configure the feature set of the device according to the attributes listed in Table 64.

Table 63: Set Features — EFh

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	Feature							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	EFh							

Table 64: Set Features' Attributes

Feature	Operation
01h	Enable 8-bit data transfer
66h	Disable reverting to power on defaults
81h	Disable 8-bit data transfer
BBh	4 bytes of data apply on Read/Write Long commands
CCh	Enable revert to power on defaults

On power-up or following a hardware reset, the device is set to the default mode 81h.

Set Multiple Mode — C6h

The Set Multiple Mode command allows the host to access the drive via Read Multiple and Write Multiple ATA commands. Additionally, the command sets the block count (i.e., the number of sectors within the block) for the Read/Write Multiple command. The sector count per block is set in the Sector Count register.

Table 65: Set Multiple Mode — C6h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	C6h							

Set Sleep Mode — 99h, E6h

The Set Sleep Mode command allows the host to set the device in sleep mode. When the onboard controller transitions to sleep mode, it clears the BSY bit and issues an interrupt. The device interface then becomes inactive. Sleep mode can be exited by issuing either a hardware or software reset.

Table 66: Set Sleep Mode — 99h, E6h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	99h or E6h							

Standby — 96h, E2h

When the Standby command is issued by the host, it transitions the device into standby mode. If the Sector Count register is set to a value other than 0h, the Auto Powerdown function is enabled and the device returns to Idle mode.

Table 67: Standby — 96h, E2h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Timer Count (5ms x Timer Count)							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	96h or E2h							

Standby Immediate — 94h, E0h

When the Standby Immediate command is issued by the host, it transitions the device into standby mode.

Table 68: Standby Immediate — 94h, E0h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_7
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	94h or E0h							

Write Buffer — E8h

The Write Buffer command allows the host to rewrite the contents of the 512- byte data buffer with the wanted data.

Table 69: Write Buffer — E8h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_7
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	E8h							

Write DMA — CAh

The Write DMA command allows the host to write data using the DMA transfer protocol.

> ***Note:*** This function does not apply to SiliconDrive IIs that have DMA disabled.

Table 70: Write DMA — CAh

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low(LBA15-8)							
Cylinder High	Cylinder High(LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number(LBA27-24)			
Command	CAh							

Write Multiple — C5h

The Write Multiple command operates in the same manner as the Write Sector command. When issued, the device sets the BSY bit within 400ns and generates an interrupt at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

Table 71: Write Multiple — C5h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low(LBA15-8)							
Cylinder High	Cylinder High(LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number(LBA27-24)			
Command	C5h							

Write Sector(s) — 30h, 31h

The Write Sector(s) command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. When issued, the device sets the BSY bit within 400ns and generates an interrupt at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

Table 72: Write Sector(s) — 30h, 31h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	30h or 31h							

Write Long Sector(s) — 32h, 33h

The Write Long Sector(s) command operates in the same manner as the Write Sector command — when issued, the device sets the BSY bit within 400ns and generates an interrupt at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

Table 73: Write Long Sector(s) — 32h, 33h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	32h or 33h							

Erase Sector(s) — C0h

The Erase Sector(s) command is issued prior to the issuance of a Write Sector(s) or Write Multiple w/o Erase command.

Table 74: Erase Sector(s) — C0h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	C0h							

Request Sense — 03h

The Request Sense command identifies the extended error codes generated by the preceding ATA command. The Request Sense command must be issued immediately following the detection of an error via the Error register.

Table 75: Request Sense — 03h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	1	X	1	Drive	X			
Command	03h							

The extended error codes are defined in the following table.

Table 76: Extended Error Codes

Extended Error Codes	Description
00h	No error detected
01h	Self test is OK (no error)
09h	Miscellaneous error
20h	Invalid command
21h	Invalid address (requested head or sector invalid)
2Fh	Address overflow (address too large)
35h, 36h	Supply or generated voltage out of tolerance
11h	Uncorrectable ECC error
18h	Corrected ECC error
05h, 30h-32h, 37h,3Eh	Self test of diagnostic failed
10h, 14h	ID not found
3Ah	Spare sectors exhausted
1Fh	Data transfer error/aborted command
0Ch, 38h, 3Bh, 3Ch, 3Fh	Computed media format
03h	Write/erase failed

Translate Sector — 87h

The Translate Sector command is not currently supported by the SiliconSystems' SiliconDrive II. If the host issues this command, the device responds with 0x00h in the data register.

Table 77: Translate Sector — 87h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	87h							

Wear-Level — F5h

The Wear-Level command is supported as an NOP command for the purposes of backward compatibility with the ANSI AT attachment standard. This command sets the Sector Count register to 0x00h.

Table 78: Wear-Level — F5h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Completion Status							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	Flag			
Command	F5h							

Write Multiple w/o Erase — CDh

The Write Multiple w/o Erase command functions identically to the Write Multiple command, with the exception that the implied pre-erase (i.e., Erase Sector(s) command) is not issued prior to writing the sectors.

Table 79: Write Multiple w/o Erase — CDh

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	CDh							

Write Sector(s) w/o Erase — 38h

The Write Sector(s) w/o Erase command functions similar to the Write Sector command, with the exception that the implied pre-erase (i.e., Erase Sector(s) command) is not issued prior to writing the sectors.

Table 80: Write Sector(s) w/o Erase — 38h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	38h							

Write Verify — 3Ch

The Write Verify command verifies each sector immediately after it is written. This command performs identically to the Write Sector(s) command, with the added feature of verifying each sector written.

Table 81: Write Verify — 3Ch

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	3Ch							

SALES AND SUPPORT

To order or obtain information on pricing and delivery, contact your SiliconSystems Sales Representative.

PART NUMBERING

NOMENCLATURE

The following table defines the SiliconDrive II CF part numbering scheme.

Table 82: Part Numbering Nomenclature

SSD-	**C**	**YYY**	**I**	**T**	**-4000** Part number suffix — contact your SiliconSystems' Sales Representative
				Temperature Range: • Blank = Commercial • I = Industrial	
			Interface: Blank = Parallel ATA (PATA)		
		Capacity: 01G = 1GB to 16G = 16GB			
	Form Factor: C = CF				
SiliconSystems' **S**ilicon**D**rive					

PART NUMBERS

The following table lists the SiliconDrive II's part numbers.

Table 83: Part Numbers

Part Number	Capacity
SSD-C16G(I)-4000	16GB
SSD-C08G(I)-4000	8GB
SSD-C04G(I)-4000	4GB
SSD-C02G(I)-4000	2GB
SSD-C01G(I)-4000	1GB

ROHS 6 OF 6 PRODUCT LABELING — PB-FREE IDENTIFICATION LABEL

The Pb-free identification label indicates that the enclosed components/devices and/or assemblies do not contain any lead (i.e., they are lead-free, as defined in RoHS directive 2002/95/ED). The above symbol is on all RoHS 6 of 6 compliant product labels, as seen in Figure 18.

SAMPLE LABEL

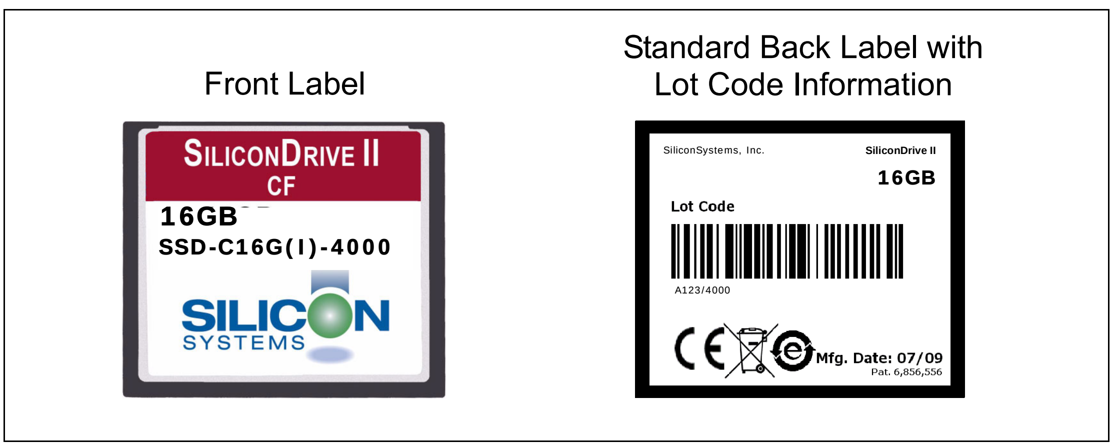

Figure 18: Sample Label

RELATED DOCUMENTATION

For more information, visit www.siliconsystems.com or contact your SiliconSystems Sales Representative.

Table 84: Related Documentation

SiliconDrive II Application-Specific Technology	Description	Document Number
SiProtect	Protection software for password-required, read/write, or read-only access.	SSANxx-SilDrvSec-R
SiSweep	Ultra-fast data erasure	SSANxx-SilDrvSec-R
SiPurge	Non-recoverable data erasure	SSANxx-SilDrvSec-R

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