



SiliconDrive™ 2.5" Drive: 128MB to 8GB of Solid-State Storage

Overview

SiliconDrive™ 2.5" drive products replace the functionality of rotating hard disk drives while providing enhanced levels of performance and reliability for Enterprise System OEMs targeting the netcom, military, industrial, interactive kiosk and medical markets. Typical end-market applications include broadband data and voice networks, military systems, flight system avionics, medical equipment, industrial control systems, and interactive kiosks.

SiliconDrives are designed to meet the growing OEM demands for high performance, high reliability, multi-year product lifecycles, low power consumption, compact size, and reliable operation in extreme environments. SiliconDrive 2.5" drive form factor products are available in capacities ranging from 128MB to 8GB.

SiliconSystems patented PowerArmor™ technology provides enhanced levels of drive integrity in the event of unexpected power disturbances and is integrated as a standard feature on all SiliconDrives. In addition, patent-pending technology advances of data sanitization and purge, write protection, and application-specific performance enhancements are available as options on all SiliconDrive products. Separate application notes covering these topics are available under NDA.



Features

- ATA-3 Compliant
- Capacity Range: 128MB to 8GB
- Supports Both 8 and 16 Bit Data Register Transfers
- Supports Dual Voltage 3.3V or 5V Interface
- < 1 Error in 10^{14} Bits Read
- MTBF $> 4,000,000$ Hours
- Industry Standard 2.5" Form Factor
- Solid-State, No Moving Parts
- Supports PIO Modes 0-4 and DMA Modes 0-2
- High Shock & Vibration Tolerance



SILICONSYSTEMS PROPRIETARY

TABLE OF CONTENTS

1. PHYSICAL SPECIFICATIONS	4
1.1. PHYSICAL DIMENSIONS	4
1.2. PIN LOCATIONS	5
1.3. JUMPER SETTINGS	5
2. PRODUCT SPECIFICATIONS	6
2.1. SYSTEM PERFORMANCE	6
2.2. SYSTEM POWER REQUIREMENTS	6
2.3. SYSTEM RELIABILITY	6
2.4. PRODUCT CAPACITY SPECIFICATIONS	7
2.5. ENVIRONMENTAL SPECIFICATIONS	7
3. ELECTRICAL SPECIFICATIONS.....	8
3.1. PIN ASSIGNMENTS	8
3.2. SIGNAL DESCRIPTIONS	9
3.3. ABSOLUTE MAXIMUM RATINGS.....	11
3.4. CAPACITANCE	11
3.5. DC CHARACTERISTICS.....	12
3.6. AC CHARACTERISTICS.....	13
3.6.1. I/O ACCESS READ TIMING	13
3.6.2. I/O ACCESS WRITE TIMING.....	14
3.6.3. TRUE IDE READ/WRITE ACCESS TIMING	15
3.6.4. TRUE IDE MULTIWORD DMA READ/WRITE ACCESS TIMING	16
4. ATA & TRUE IDE REGISTER DECODING	17
4.1. MEMORY MAPPED REGISTER DECODING	17
4.2. INDEPENDENT I/O MODE REGISTER DECODING	18
4.3. PRIMARY AND SECONDARY I/O MAPPED REGISTER DECODING	19
4.4. TASK FILE REGISTER SPECIFICATION.....	19
5. ATA REGISTERS	20
5.1. DATA REGISTER	20
5.2. ERROR REGISTER.....	20
5.3. FEATURE REGISTER	21
5.4. SECTOR COUNT REGISTER.....	21
5.5. SECTOR NUMBER REGISTER	21
5.6. CYLINDER LOW REGISTER	22
5.7. CYLINDER HIGH REGISTER	22
5.8. DRIVE/HEAD REGISTER.....	23
5.9. STATUS REGISTER	24
5.10.COMMAND REGISTER.....	24
5.11.ALTERNATE STATUS REGISTER	25
5.12.DEVICE CONTROL REGISTER	25
5.13.DEVICE ADDRESS REGISTER	26

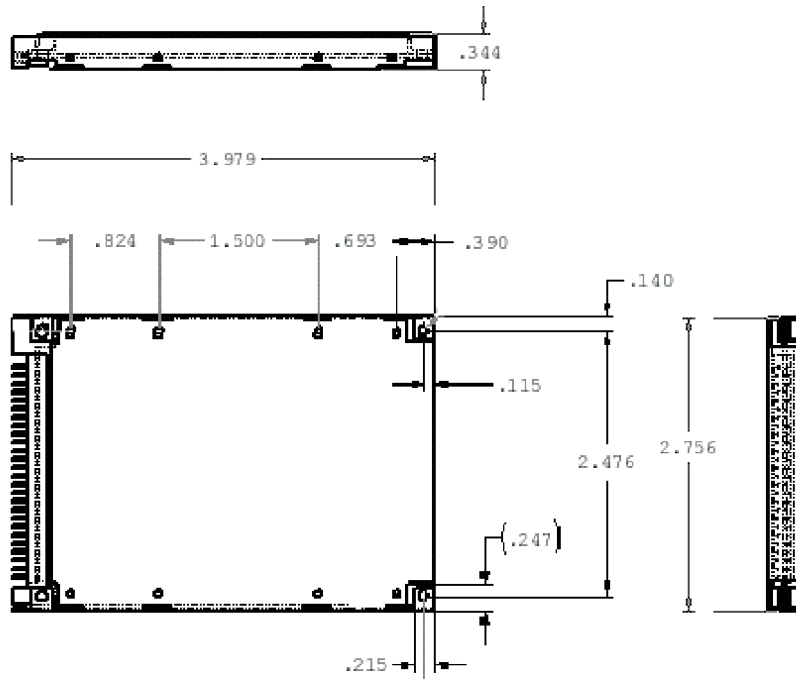
6. ATA COMMAND BLOCK & SET DESCRIPTION	27
6.1. ATA COMMAND SET.....	28
6.1.1. CHECK POWER MODE – 98H, E5H	29
6.1.2. EXECUTIVE DRIVE DIAGNOSTIC – 90H	29
6.1.3. FORMAT TRACK – 50H	30
6.1.4. IDENTIFY DRIVE – ECH.....	30
6.1.4.1. IDENTIFY DRIVE – DRIVE ATTRIBUTE DATA	31
6.1.5. IDLE – 97H, E3H	31
6.1.6. IDLE IMMEDIATE – 95H, E1H	33
6.1.7. INITIALIZE DRIVE PARAMETERS – 91H.....	33
6.1.8. RECALIBRATE – 1XH.....	34
6.1.9. READ BUFFER – E4H	34
6.1.10. READ DMA – C8H	34
6.1.11. READ MULTIPLE – C4H	35
6.1.12. READ SECTOR – 20H, 21H.....	36
6.1.13. LEAD LONG SECTOR(S) – 22H, 23H	37
6.1.14. READ VERIFY SECTOR(S) – 40H, 41H.....	37
6.1.15. SEEK – 7XH	38
6.1.16. SET FEATURES – EFH	38
6.1.17. SET MULTIPLE MODE – C6H	39
6.1.18. SET SLEEP MODE – 99H, E6H	40
6.1.19. STANDBY – 96H, E2H.....	40
6.1.20. STANDBY IMMEDIATE – 94H, E0H.....	41
6.1.21. WRITE BUFFER – E8H	41
6.1.22. WRITE DMA – CAH	41
6.1.23. WRITE MULTIPLE – C5H	42
6.1.24. WRITE SECTOR(S) – 30H, 31H	43
6.1.25. WRITE LONG SECTOR(S) – 32H, 33H.....	44
6.1.26. ERASE SECTOR(S) – C0H.....	44
6.1.27. REQUEST SENSE – 03H	45
6.1.28. TRANSLATE SECTOR – 87H	46
6.1.29. WEAR LEVEL – F5H	46
6.1.30. WRITE MULTIPLE W/O ERASE – CDH.....	47
6.1.31. WRITE SECTOR(S) W/O ERASE – 38H	47
6.1.32. WRITE VERIFY – 3CH	48
7. SALES AND SUPPORT	49
7.1. PART NUMBERING NOMENCLATURE	49

1. PHYSICAL SPECIFICATIONS

SiliconDrive 2.5" Drive products are offered in an industry standard 2.5" drive form factor. Refer to Section 7.1 Part Ordering Nomenclature for details regarding 2.5" drive capacities.

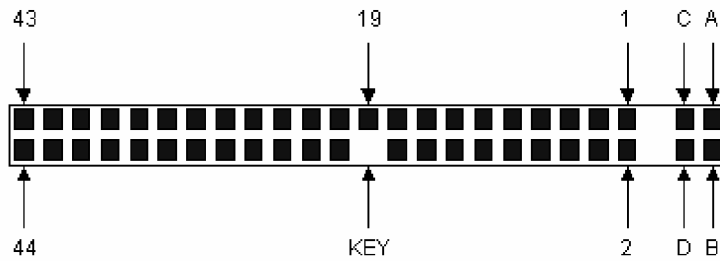
1.1. Physical Dimensions

The following diagram describes the physical dimensions of the SiliconDrive 2.5" drive:



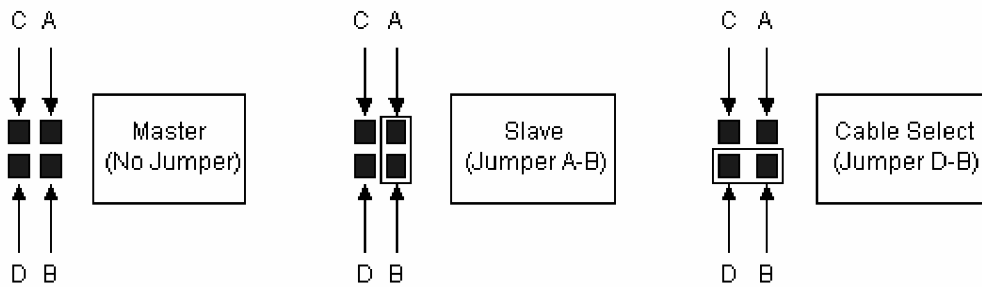
1.2. Pin Locations

The following diagram identifies the Pin Locations of the SiliconDrive 2.5" Drive:



1.3. Jumper Settings

The following diagram defines the SiliconDrive 2.5" Drive Jumper Settings:



2. PRODUCT SPECIFICATIONS¹

2.1. System Performance

Reset to Ready Startup Time (Typical/Max)	200ms/400ms
Read Transfer Rate (Typical)	8MB/s
Write Transfer Rate (Typical)	6MB/s
Burst Transfer Rate	16.7MB/s
Controller Overhead (Command to DRQ)	2ms (max)

2.2. System Power Requirements

DC Input Voltage	3.3 ± 10%	5.0 ± 10%
Sleep (Standby Current)	<0.5mA	<1.0mA
Read (Typical/Peak)	20mA/75mA	30mA/100mA
Write (Typical/Peak)	30mA/75mA	40mA/100mA

2.3. System Reliability

MTBF (@ 25°C)	> 4,000,000 Hours
Data Reliability	< 1 Non-Recoverable Error in 10 ¹⁴ Bits Read
Endurance	>2,000,000 write/erase cycles

¹ All SiliconDrive2.5" values quoted are typical at 25°C and nominal supply voltage.

2.4. Product Capacity Specifications

Product Density	Formatted Capacity (Bytes)	Number of Sectors	Number of Cylinders	Number of Heads	Number of Sectors/Track
128MB	130,154,496	254,208	993	8	32
256MB	260,571,136	508,928	994	16	32
512 MB	521,773,056	1,019,088	1011	16	63
1GB	1,047,674,880	2,046,240	2030	16	63
2GB	2,098,446,336	4,098,528	4066	16	63
4GB	4,224,761,856	8,251,488	8186	16	63
6GB	6,309,789,696	12,323,808	12226	16	63
8GB	8,456,749,056	16,517,088	16386	16	63

2.5. Environmental Specifications

Temperature	0°C to 70°C (Standard)
	-40°C to 85°C (Industrial)
Humidity	8% to 95% non-condensing
Vibration	16.3gRMS, MIL-STD-810F, Method 514.5, Procedure I, Category 24
Shock	1000G, Half-sine, 0.5ms Duration 50g Pk, MIL-STD-810F, Method 516.5, Procedure I
Altitude	80,000ft, MIL-STD-810F, Method 500.4, Procedure II

3. ELECTRICAL SPECIFICATIONS

3.1. Pin Assignments

The following Table describes the SiliconDrive 2.5" Drive 44-Pin IDE Connector Signals:

Pin	IDE-ATA	Pin	IDE-ATA
1	-RESET	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	KEY
21	DMARQ	22	GND
23	-IOWR	24	GND
25	-IORD	26	GND
27	IORDY	28	-CSEL
29	-DMACK	30	GND
31	INTRQ	32	-IOCS16
33	A1	34	-PDIAG
35	A0	36	A2
37	-CS0	38	-CS1
39	-DASP	40	GND
41	VCC	42	VCC
43	GND	44	NC

3.2. Signal Descriptions

3.2. Signal Descriptions			
Signal Name	Pin(s)	Type	Description
A2 - A0	36,33,35	I	ADDRESS INPUTS: The Address signals are asserted by the host to access the task registers in the device.
-CS0,-CS1	37,38	I	CHIP SELECTS: These are the chip select signals used to select the control block registers.
-CSEL	28	I	CABLE SELECT: This internally pulled up signal is used to configure this device as a Master or a Slave when the jumper configuration is in CSEL mode. When this pin is grounded by the host, this device is configured as a Master. When this pin is open, this device is configured as a slave.
D15-D0	18,16,14,12, 10,8,6,4, 3,5,7,9, 11,13,15,17	I/O	DATA INPUTS/OUTPUTS: This is 8 or 16 bit bi-directional interface between the host and device. The lower 8 bits are used for 8 bit register transfers.
-DMACK	29	I	DMA ACKNOWLEDGE: This signal is used by the host in response to DMARQ to initiate DMA transfers. The DMARQ/-DMACK handshake is used to provide flow control during the transfer. When -DMACK is asserted, -CS0 and -CS1 shall not be asserted and transfers shall be 16-bits wide.
DASP	39	I/O	DISK ACTIVE/SLAVE PRESENT: This open drain output signal is asserted low any time the drive is active. In a master/slave configuration, this signal is used by the slave to inform the master a slave is present.
DMARQ	21	O	DMA REQUEST: This signal is used for DMA transfers between the host and device. DMARQ shall be asserted by the device when the device is ready to transfer data to/from the host. The direction of data transfer is controller by -IORD and -IOWR. This signal is used in a handshake manner with -DMACK, i.e. the device shall wait until the host asserts -DMACK before negating DMARQ, and re-assert DMARQ if there is more data to transfer. The DMARQ/-DMACK handshake is used to provide flow control during the transfer.
GND	2,19,22,24, 26,30,40,43	-	GROUND: Device Ground.

3.2. Signal Descriptions

Signal Name	Pin(s)	Type	Description
INTRQ	31	O	INTERRUPT REQUEST: This signal is an active high interrupt request to the host.
IORDY	27	I	I/O CHANNEL READY: The signal is negated to extend the host transfer cycle of any host register access.
-IORD	25	I	DEVICE I/O READ: This is the read strobe signal from the host. The falling edge of IORD enables data from the device onto the data bus. The rising edge of IORD latches data at the host. The host shall not act on the data until it is latched.
-IOWR	23	I	DEVICE I/O WRITE: This is the write strobe signal from the host. The rising edge of IOWR# latches data from the data bit signals. The device will not act on the data until it is latched.
KEY	20	-	KEY: Reserved for the Connector Key.
-PDIAG	34	I/O	PASS DIAGNOSTIC: This open drain signal is asserted by the Slave to indicate to the Master that it has passed its diagnostics.
-RESET	1	I	DEVICE RESET: Active Low. When Active, this sets all internal registers to their default state. This signal shall be held asserted until at least 25us after power has been stabilized during the device power on.
VCC	41,42	-	DEVICE POWER SUPPLY: Device Power 3.3/5V.

3.3. Absolute Maximum Ratings

Vcc = 3.3 ± 10%

Symbol	Parameter	Min	Max	Units
Ts	Storage Temperature	-55	125	°C
TA	Operating Temperature	-40	85	°C
Vcc	Vcc with Respect to GND	-0.3	6.7	V
Vin	Input Voltage	-0.5	3.8	V
Vout	Output Voltage	-0.3	3.6	V

Vcc = 5.0 ± 10%

Symbol	Parameter	Min	Max	Units
Ts	Storage Temperature	-55	125	°C
TA	Operating Temperature	-40	85	°C
Vcc	Vcc with Respect to GND	-0.3	6.7	V
Vin	Input Voltage	-0.5	6.0	V
Vout	Output Voltage	-0.3	5.8	V

3.4. Capacitance

Symbol	Parameter	Max	Units
Cin	Input Capacitance	35	pF
Cout	Output Capacitance	35	
C/I/O	Bi-directional Capacitance	35	

3.5. DC Characteristics

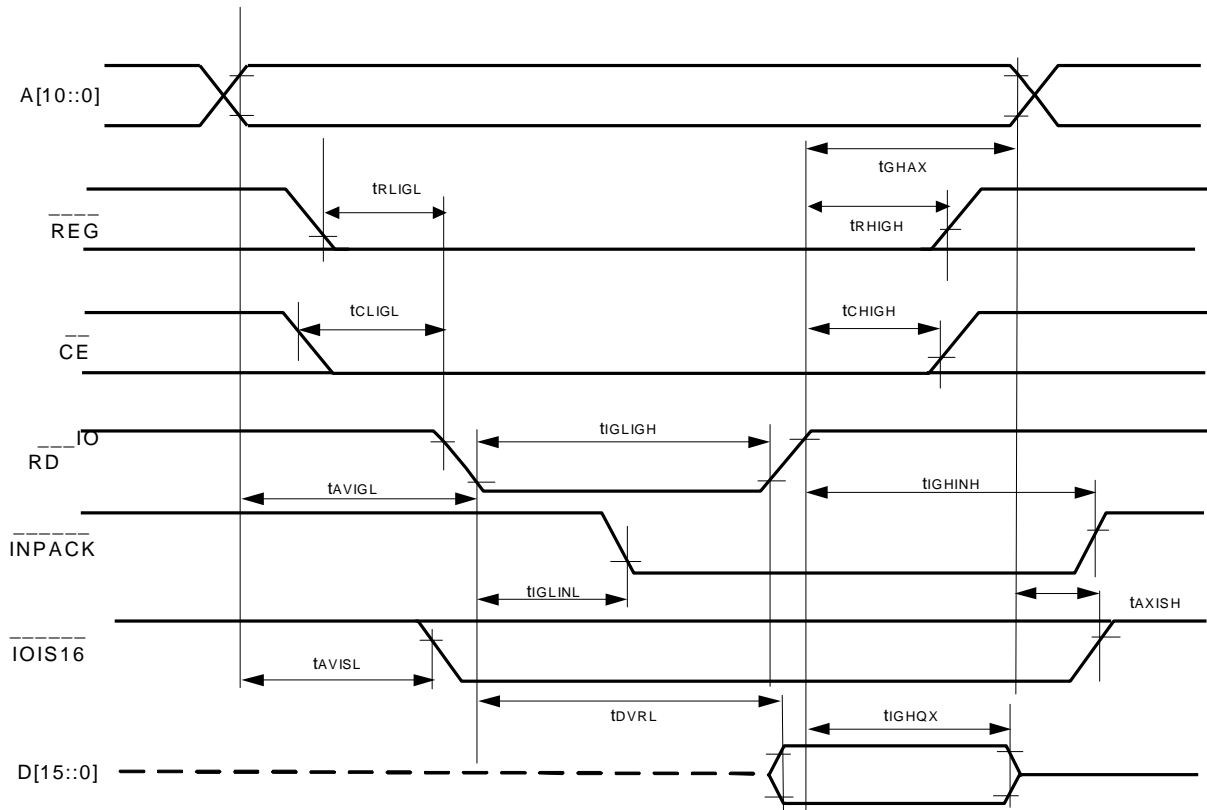
Symbol	Parameter	3.3 V \pm 10%		5V \pm 10%		Units
		Min.	Max.	Min.	Max.	
V _{CC}	Power Supply Voltage	3.0	3.6	4.5	5.5	V
I _{LI}	Input Leakage *(1) Current		5		5	μ A
I _{LO}	Output Leakage *(1) Current		5		5	μ A
V _{CCR}	V _{CC} Read Current		50	-	80	mA
V _{CCW}	V _{CC} Write Current		50	-	80	mA
V _{CCS}	V _{CC} Standby Current		.3	-	.5	mA
V _{IL}	Input LOW Voltage	-0.3	.3 x V _{CC}	-0.3	.3 x V _{CC}	V
V _{IH}	Input HIGH Voltage	.7 x V _{CC}	V _{CC} + .3	.7 x V _{CC}	V _{CC} + .3	V
V _{OL}	Output LOW Voltage	-	.4		.4	V
V _{OH}	Output HIGH Voltage	V _{CC} - 0.4		V _{CC} - 0.4		V

Note

*(1) Except pulled up/pulled down pin.

3.6. AC Characteristics

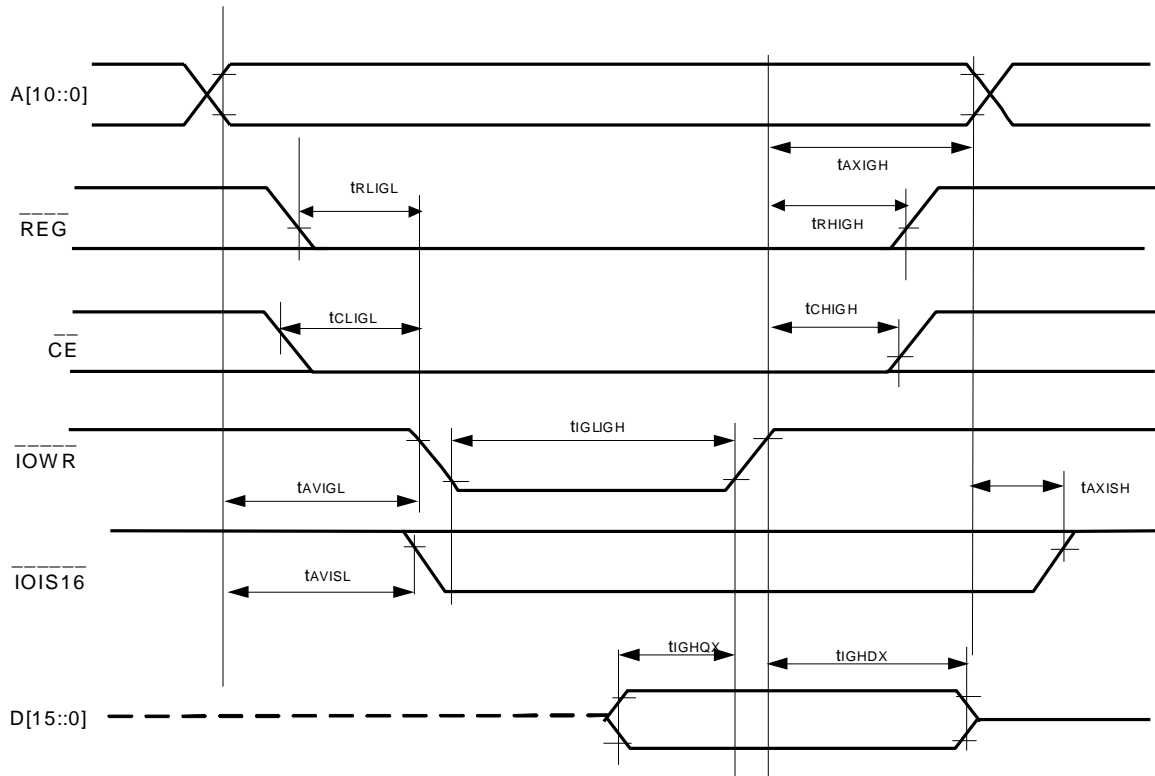
3.6.1. I/O Access Read Timing



Symbol	Parameter	Min	Max	Units
t _{DVRL}	Data Delay after IORD	-	50	nsec
t _{GHQX}	Data Hold following IORD	5	-	
t _{GLIGH}	IORD Pulse Width	65	-	
t _{AVIGL}	Address Setup before IORD	25	-	
t _{GHAX}	Address Hold following IORD	10	-	
t _{CLIGL}	CE Setup before IORD	5	-	
t _{CHIGH}	CE Hold following IORD	10	-	
t _{RLIGL}	REG Setup before IORD	5	-	
t _{RLIGH}	REG Hold following IORD	0	-	
t _{GLINL}	INPACK Delay falling from IORD	-	(1)	
t _{GLINH}	INPACK Delay Rising from IORD	-	(1)	
t _{AVISL}	IOIS16 Delay Falling from Address	-	(1)	
t _{AXISH}	IOIS16 Delay Rising from Address	-	(1)	

Note: 1) IOIS16 and INPACK is not supported.

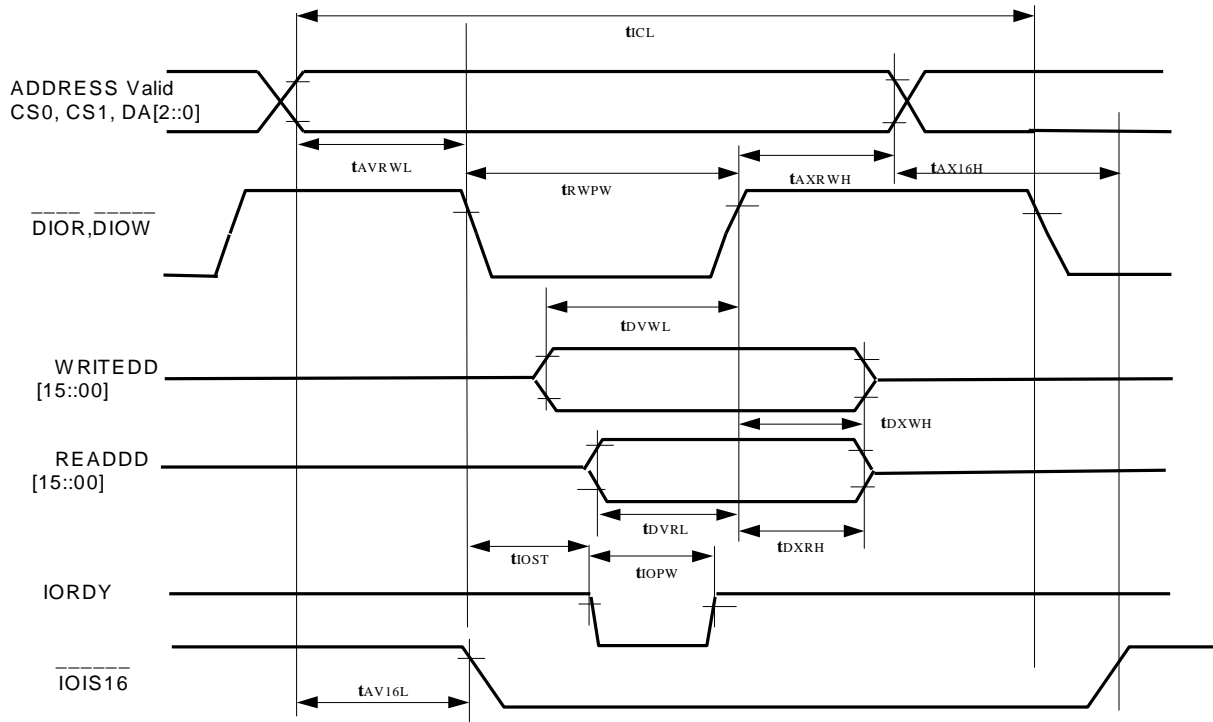
3.6.2. I/O Access Write Timing



Symbol	Parameter	Min	Max	Units
t_{IGHDX}	Data Hold following IOWR	5	-	nsec
t_{IGHQX}	Data Setup before IOWR	20	-	
t_{IGLIGH}	IOWR Pulse Width	65	-	
t_{AVIGL}	Address Setup before IOWR	25	-	
t_{AXIGH}	Address Hold following IOWR	10	-	
t_{CLIGL}	CE Setup before IOWR	5	-	
t_{CHIGH}	CE Hold following IOWR	10	-	
t_{RLIGL}	REG Setup before IOWR	5	-	
t_{RHIGH}	REG Hold following IOWR	0	-	
t_{AVISL}	IOIS16 Delay Falling from Address	-	(1)	
t_{AXISH}	IOIS16 Delay Rising from Address	-	(1)	

Note: 1) IOIS16 and INPACK is not supported.

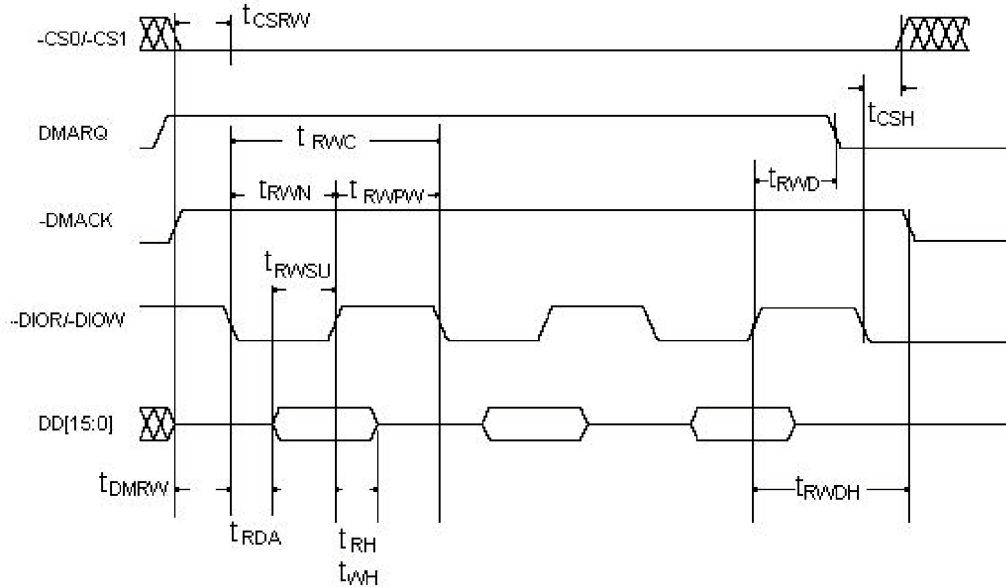
3.6.3. True IDE Read/Write Access Timing



Symbol	Parameter	Min	Max	Units
t _{ICL}	Cycle Time	100	-	nsec
t _{AVRWL}	Address Valid to DIOR,DIOW Setup Time	15	-	
t _{RWPW}	DIOR, DIOW Pulse Width	65	-	
t _{DVWL}	DIOW Data Setup Time	20	-	
t _{DXWH}	DIOW Data Hold Time	5	-	
t _{DVRL}	DIOR Data Setup Time	15	-	
t _{DXRH}	DIOR Data Hold Time	5	-	
t _{AV16L}	Address Valid to IOCS16 Assertion	-	(1)	
t _{AX16H}	Address Valid to IOCS16 Negation	-	(1)	
t _{AXRWH}	DIOW,DIOR to Address Valid Hold Time	10	-	
t _{IOST}	IORDY Setup Time	-	(1)	
t _{IOPW}	IORDY Pulse Width	-	(1)	

Note: 1) IOIS16 and INPACK is not supported.

3.6.4. True IDE Multiword DMA Read/Write Access Timing



Symbol	Parameter	Min	Max	Units
t_{RWC}	Cycle Time (Mode 2)	100	-	nsec
t_{RWPW}	DIOR/DIOW Pulse Width	65	-	
t_{RDA}	DIOR Data Access	-	50	
t_{RWSU}	DIOR/DIOW Data Setup Time	15	-	
t_{WH}	DIOW Data Hold Time	5	-	
t_{RH}	DIOR Data Hold Time	5	-	
t_{DMRW}	DMACK to DIOR/DIOW Setup Time	0	-	
t_{RWDH}	DIOR/DIOW to DMACK Hold Time	5	-	
t_{RWN}	DIOR/DIOW negated Pulse Width	25	-	
t_{RWD}	DIOR/DIOW to DMARQ Delay	-	25	
t_{CSRW}	CS(1:0) valid to DIOR/DIOW	10	-	
t_{CSH}	CS(1:0) Hold Time	10	-	

4. ATA & TRUE IDE REGISTER DECODING

SiliconDrives can be configured as either Memory Mapped or I/O Devices. As noted earlier communication to and from the card is accomplished using the ATA Command Block.

4.1. Memory Mapped Register Decoding

In Memory Mapped mode, the cards' registers are accessed via standard memory references (i.e., OE# and WE#). The ATA registers are mapped to common memory space in a 2K byte window starting at address 0.

Reg#	Offset	A10	A9:A4	A3	A2	A1	A0	OE# = L	WE# = L
1	0	0	X	0	0	0	0	Even Data Read	Even Data Write
1	1	0	X	0	0	0	1	Error	Feature
1	2	0	X	0	0	1	0	Sector Count	Sector Count
1	3	0	X	0	0	1	1	Sector Number	Sector Number
1	4	0	X	0	1	0	0	Cylinder Low	Cylinder Low
1	5	0	X	0	1	0	1	Cylinder High	Cylinder High
1	6	0	X	0	1	1	0	Drive/Head	Drive/Head
1	7	0	X	0	1	1	1	Status	Command
1	8	0	X	1	0	0	0	Duplicate Even Data Read	Duplicate Even Data Write
1	9	0	X	1	0	0	1	Duplicate Odd Data Read	Duplicate Odd Data Write
1	D	0	X	1	1	0	1	Duplicate Error	Duplicate Feature
1	E	0	X	1	1	1	0	Alternate Status	Device Control
1	F	0	X	1	1	1	1	Drive Address	Reserved
1	X	1	X	X	X	X	0	Even Data Read	Even Data Write
1	X	1	X	X	X	X	1	Odd Data Read	Odd Data Write

4.2. Independent I/O Mode Register Decoding

Independent I/O Mode, or Contiguous I/O mode requires the host to decode a contiguous block of 16 I/O registers to select the card.

REG#	Offset	A10	A9:A4	A3	A2	A1	A0	IORD# = L	IOWR# = L
0	0	X	X	0	0	0	0	Even Data Read	Even Data Write
0	1	X	X	0	0	0	1	Error	Feature
0	2	X	X	0	0	1	0	Sector Count	Sector Count
0	3	X	X	0	0	1	1	Sector Number	Sector Number
0	4	X	X	0	1	0	0	Cylinder Low	Cylinder Low
0	5	X	X	0	1	0	1	Cylinder High	Cylinder High
0	6	X	X	0	1	1	0	Drive/Head	Drive/Head
0	7	X	X	0	1	1	1	Status	Command
0	8	X	X	1	0	0	0	Duplicate Even Data Read	Duplicate Even Data Write
0	9	X	X	1	0	0	1	Duplicate Odd Data Read	Duplicate Odd Data Write
0	D	X	X	1	1	0	1	Duplicate Error	Duplicate Feature
0	E	X	X	1	1	1	0	Alternate Status	Device Control
0	F	X	X	1	1	1	1	Drive Address	Reserved

4.3. Primary and Secondary I/O Mapped Register Decoding

REG#	A10	A9:A4 Primary	A9:A4 Secondary	A3	A2	A1	A0	IORD# = L	IOWR# = L
0	X	1Fyh	17yh	0	0	0	0	Even Data Read	Even Data Write
0	X	1Fyh	17yh	0	0	0	1	Error	Feature
0	X	1Fyh	17yh	0	0	1	0	Sector Count	Sector Count
0	X	1Fyh	17yh	0	0	1	1	Sector Number	Sector Number
0	X	1Fyh	17yh	0	1	0	0	Cylinder Low	Cylinder Low
0	X	1Fyh	17yh	0	1	0	1	Cylinder High	Cylinder High
0	X	1Fyh	17yh	0	1	1	0	Drive/Head	Drive/Head
0	X	1Fyh	17yh	0	1	1	1	Status	Command
0	X	3Fyh	37yh	0	1	1	0	Alternate Status	Device Control
0	X	3Fyh	37yh	0	1	1	1	Drive Address	Reserved

4.4. Task File Register Specification

The Task File Registers are used for reading and writing the storage data in the SiliconDrive. The decoded addresses are as shown.

CS0#	CS1#	DA02	DA01	DA00	DIOR# = L	DIOW# = L
0	1	0	0	0	Data	Data
0	1	0	0	1	Error	Feature
0	1	0	1	0	Sector Count	Sector Count
0	1	0	1	1	Sector Number	Sector Number
0	1	0	1	1	Cylinder Low	Cylinder Low
0	1	1	0	1	Cylinder High	Cylinder High
0	1	1	1	0	Drive/Head	Drive/Head
0	1	1	1	1	Status	Command
0	0	X	X	X	Invalid	Invalid
1	1	X	X	X	High-Z	Not Used
1	0	0	X	X	High-Z	Not Used
1	0	1	0	X	High-Z	Not Used
1	0	1	1	0	Alternate Status	Device Control
1	0	1	1	1	Device Address	Not Used

5. ATA REGISTERS

5.1. Data Register

The Data Register is a 16-bit Register used to transfer data blocks between the Host and the Drive buffer. This register may set to 8-bit mode by using the Set Features Command defined in Section 9.1.15.

5.2. Error Register

The Error Register contains the error status, if any, generated from the last executed ATA Command. The contents are qualified by the ERR bit being set in the Status Register Section 8.9.

Operation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Read	BBK	UNC	MC	IDNF	MCR	ABRT	TKNOF	AMNF
Default Value	0	0	0	0	0	0	0	0

Notes

Bit 7: BBK (Bad Block Detected)	Set when a Bad Block is detected.
Bit 6: UNC (Uncorrectable Data Error)	Set when Uncorrectable Error is encountered.
Bit 5: MC (Media Changed)	Set to 0.
Bit 4: IDNF (ID Not Found)	Set when Sector ID not found.
Bit 3: MCR (Media Change Request)	Set to 0.
Bit 2: ABRT (Aborted Command)	Set when Command Aborted due to drive error.
Bit 1: TKNOF (Track 0 Not Found)	Set when Executive Drive Diagnostic Command. Bit
0: AMNF (Address mark Not Found)	Set in case of a general error.

5.3. Feature Register

The Feature Register is command specific and is used to enable and disable interface features. This register supports either odd or even byte data transfers only.

Operation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Read/Write	Feature Byte							

5.4. Sector Count Register

The Sector Count Register is used to read or write the sector count of the data for which an ATA transfer has been made.

Operation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Read/Write	Sector Count							
Default Value	0	0	0	0	0	0	0	1

5.5. Sector Number Register

The Sector Number Register is set by the host to specify the starting sector number associated with the next ATA command to be executed. Following a qualified ATA command sequence the device will set the register value to the last sector read or written as a result of the previous AT command.

When LBA mode is implemented and the host issues a command the contents of this register describe the Logical Block Number bits A[7:0]. Following an ATA Command the device will load this register with the LBA block number resulting from the last ATA command.

Operation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Read/Write	Sector Number (CHS Addressing)							
	Logical Block Number bits A07-A00 (LBA Addressing)							
Default Value	0	0	0	0	0	0	0	1

5.6. Cylinder Low Register

The Cylinder Low Register is set by the host to specify the cylinder number low byte. Following an ATA command, the contents of this register is written by the device, identifying the cylinder number low byte.

In LBA mode, this 8-bit register maintains the contents of the Logical Block number address bits A15:A08.

Operation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Read/Write	Cylinder Number Low Byte (CHS Addressing)							
	Logical Block Number bits A15-A08 (LBA Addressing)							
Default Value	0	0	0	0	0	0	0	0

5.7. Cylinder High Register

The Cylinder High Register is set by the host to specify the cylinder number high byte. Following an ATA command, the contents of this register is set internally by the device, identifying the cylinder number high byte.

In LBA mode, this 8-bit register maintains the contents of the Logical Block number address bits A23:A16.

Operation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Read/Write	Cylinder Number Low Byte (CHS Addressing)							
	Logical Block Number bits A23-A16 (LBA Addressing)							
Default Value	0	0	0	0	0	0	0	0

5.8. Drive/Head Register

The Drive/Head Register is used by the host and the device to select the type of addressing (CHS or LBA), the drive letter, and either bits 3 through 0 of the head number in CHS mode or in LBA mode bits D3:D0 reflect the logical block number bits LBA27:LBA24.

Operation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Read/Write	1	LBA	1	DRV	HS3 LBA27	HS2 LBA26	HS1 LBA25	HS0 LBA24
Default Value	1	0	1	0	0	0	0	0

The Drive/Head Register is used by the host, to specify one of a pair of ATA drives present in the platform.

Notes

Bit 6: LBA (Logical Block Addressing)

Selects between CHS (0) and LBA (1) addressing mode.

Bit 7: DRV (Drive Address)

Indicates the drive number selected by the host, either 0 or 1.

Bits 3 - 0: HS3 to 0 mode.

Indicates bits 3 to 0 of the head number in CHS addressing or LBA bits 27 thru 24 in LBA mode.

CHS to LBA conversion:

$$LBA = (C \times HpC + H) \times SpH + S - 1$$

LBA to CHS conversion:

$$C = LBA / (HpC \times SpH)$$

$$H = (LBA / SpH) \bmod (HpC)$$

$$S = (LBA \bmod (SpH)) + 1$$

Where:

'C' is the Cylinder Number.

'H' is the Head Number.

'S' is the Sector Count.

'HpC' is the Head count per Cylinder Count.

'SpH' is the Sector count per Head Count (Track).

5.9. Status Register

The Status Register provides the device's current status to the host. The status register is an 8-bit read only register. When the contents of this register are read by the host, the IREQ# bit is cleared.

Operation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Read/Write	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
Default Value	0	0	0	0	0	0	0	0

Notes

Bit 7: BSY (Busy)	Set when the drive is busy and unable to process any new ATA commands.
Bit 6: DRDY (Data Ready)	Set when the device is ready to accept ATA commands from the host.
Bit 5: DWF (Drive Write Fault)	Always set to 0.
Bit 4: DSC (Drive Seek Complete)	Set when the drive heads have been positioned over a specific track.
Bit 3: DRQ (Data Request)	Set when device is read to transfer a word or byte of data to or from the host and the device.
Bit 2: CORR (Corrected Data)	Always set to 0.
Bit 1: IDX (Index)	Always set to 0.
Bit 0: ERR (Error)	Set when an error occurred during the previous ATA command.

5.10. Command Register

The Command Register specifies the ATA Command code being issued to the drive by the host. Execution of the command begins immediately following the issuance of the command register code by the host.

Operation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Read/Write	ATA Command Code							

Refer to Section 6.1 ATA Command Set, for a listing of the supported ATA Commands.

5.11. Alternate Status Register

The Alternate Status Register is a read-only register indicating the status of the device, following the previous ATA command. Refer to Section 8.9, Status Register for specific details.

Operation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Read/Write	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
Default Value	0	0	0	0	0	0	0	0

5.12. Device Control Register

The Device Control Register is used to control the Interrupt Request and issue ATA Software Resets.

Operation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Write	-	-	-	-	1	SRST	nIEN	0

Notes

Bits 7-4:

Reserved bits.

Bit 3:

Always set to 1

Bit 2: SRST (Software Reset)

When set, resets the ATA software.

Bit 1: nIEN(Interrupt Enable)

When set, device interrupts are disabled. No function in Memory Mapped mode.

Bit 0:

Always set to 0.

5.13. Device Address Register

The Device Address Register is used to maintain compatibility with ATA disk drive interfaces.

Operation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Read/Write	-	nWTG	nHS3	nHS2	nHS1	nHS0	nDS1	nDS0
Default Value	0	0	1	1	1	1	1	0

Notes

Bit 7:	Reserved bit.
Bit 6: nWTG (Write Gate)	Low when a write to the device is in process.
Bits 5-2: nHS3 to nHS0	Negated binary address of the currently selected head.
Bit 1: nDS1	Low when Drive 1 is selected and active.
Bit 0: nDS0	Low when Drive 0 is selected and active.

6. ATA COMMAND BLOCK & SET DESCRIPTION

In accordance with the ANSI ATA Specification, the device implements seven registers which are used to transfer instructions to the device by the host. These commands follow the ANSI standard ATA protocol, a description of the ATA Command block is provided below.

Register	D7	D6	D5	D4	D3	D2	D1	D0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	1	LBA	1	Drive	X			
Command	X							

6.1. ATA Command Set

Class	Command Name	Command Code	Registers Used					
			FR	SC	SN	CY	DH	LBA
1	Check Power Mode	98h,E5h					D	
1	Execute Drive Diagnostics	90h					D	
1	Erase Sector	C0h		Y	Y	Y	Y	Y
2	Format Track	50h		Y		Y	Y	Y
1	Identify Drive	ECh					D	
1	Idle	97h,E3h		Y			D	
1	Idle Immediate	95h,E1h					D	
1	Initialize Drive Parameters	91h		Y			Y	
1	Read Buffer	E4h					D	
1	Read DMA	C8h		Y	Y	Y	Y	Y
1	Read Multiple	C4h		Y	Y	Y	Y	Y
1	Read Long Sector	22h,23h			Y	Y	Y	Y
1	Read Sector(s)	20h,21h			Y	Y	Y	Y
1	Read Verify Sector(s)	40h,41h		Y	Y	Y	Y	Y
1	Recalibrate	1Xh					Y	
1	Request Sense	03h					D	
1	Seek	7Xh			Y	Y	Y	Y
1	Set Features	EFh	Y				D	
1	Set Multiple Mode	C6h		Y			D	
1	Set Sleep Mode	99h,E6h					D	
1	Standby	96h,E2h					D	
1	Standby Immediate	94h,E0h					D	
1	Translate Sector	87h		Y	Y	Y	Y	Y
1	Wear Level	F5h					Y	
2	Write Buffer	E8h					D	
1	Write DMA	CAh		Y	Y	Y	Y	Y
2	Write Long Sector	32h,33h			Y	Y	Y	Y
3	Write Multiple	C5h		Y	Y	Y	Y	Y
3	Write Multiple w/o Erase	CDh		Y	Y	Y	Y	Y
2	Write Sector(s)	30h,31h		Y	Y	Y	Y	Y
2	Write Sector(s) w/o Erase	38h		Y	Y	Y	Y	Y
3	Write Verify	3Ch		Y	Y	Y	Y	Y
-	NOP	FFh						

Register Notes: CY - Cylinder; SC - Sector Count; DH – Drive/Head; SN – Sector Number; FR – Feature LBA – LBA bit of the Drive/Head Register ('D' denotes that only the drive bit is used)

6.1.1. Check Power Mode – 98h, E5h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive				
Command	98h or E5h							

The Check Power Mode command verifies the device's current power mode. When the device is configured for standby mode, or is entering or exiting Standby, the BSY bit will be set and the Sector Count register is set to 00h, then clears the BSY bit. In Idle mode, BSY is set and the Sector Count Register is set to FFh, then the BSY bit is cleared and an interrupt is issued.

6.1.2. Executive Drive Diagnostic – 90h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive				
Command	90h							

The Executive Drive Diagnostic performs an internal read write diagnostic test using (AA55h and 55AAh). If an error is detected in the read/write buffer, the Error Register will report the appropriate Diagnostic Code.

6.1.3. Format Track – 50h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7 – 0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	50h							

The Format Track command formats the common solid-state memory array.

6.1.4. Identify Drive – ECh

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	ECh							

Issued by the host, the Identify Drive command provides 256 bytes of Drive attribute data (i.e., Sector Size, Count, etc.) The Identify Drive data structure is detailed in the preceding table.

6.1.4.1. Identify Drive – Drive Attribute Data

6.1.4.1 Identify Drive – Drive Attribute Data			
Word Address	Data Default	Bytes	Data Description
0	045Ah	2	General Configuration Bit Information 15: Non-magnetic Disk 14: Formatting Speed Latency Permissible Gap needed 13: Track Offset Option supported 12: Data Strobe Offset Option supported 11: Over 0.5% Rotational Speed Difference 10: Disk Transfer Rate > 10Mbps 9: 10Mbps >= Disk Transfer Rate > 5Mbps 8: 5Mbps >= Disk Transfer Rate 7: Removable Cartridge Drive 6: Fixed Drive 5: Spindle Motor Control Option executed 4: Over 15µs Changing Head Time 3: Non-MFM Encoding 2: Soft Sector Allocation 1: Hard Sector Allocation 0: Reserved
1	XXXXh	2	Number of Cylinders
2	0000h	2	Reserved
3	00XXh	2	Number of Heads
4	0000h	2	Number of Unformatted Bytes per Track
5	XXXXh	2	Number of Unformatted Bytes per Sector
6	XXXXh	2	Number of Sectors per Track
7 - 8	XXXXh	4	Number of Sectors per Device
9	0000h	2	Reserved
10 – 19	XXXXh	20	Serial Number
20	0001h	2	Buffer Type 0000h: Not specified 0001h: A single ported single sector buffer 0002h: A dual ported multi-sector buffer 0003h: A dual ported multi-sector buffer with a read caching
21	0001h	2	Buffer Size in 512-byte increments
22	0004h	2	Number of ECC Bytes passed on Read/Write Long Cmds
23 - 26	XXXXh	8	Firmware Revision (8 ASCII Characters)
27 - 46	XXXXh	40	Model Number (40 ASCII Characters)
47	0001h	2	7 – 0: Max Number of Sectors that can be transferred with a Read/Write Multiple Command per Interrupt
48	0000h	2	Double Word (32 bit) not supported
49	0f00h	2	11: IORDY Supported 9: LBA supported 8: DMA supported
50	0000h	2	Reserved
51	0200h	2	15 – 8: PIO data transfer cycle timing
52	0000h	2	15 – 8: DMA data transfer cycle timing
53	0003h	2	1: Words 64 to 70 are valid

6.1.4.1 Identify Drive – Drive Attribute Data

Word Address	Data Default	Bytes	Data Description
			0: Words 54 to 58 are valid
54	XXXXh	2	Current Number of Cylinders
55	XXXXh	2	Current Number of Heads
56	XXXXh	2	Current Sectors per Track
57 – 58	XXXXh	4	Current Capacity in Sectors
59	010Xh	2	7 – 0: Current Sectors can be transferred with a Read/Write Multiple command per interrupt
60 - 61	XXXXh	4	Total Number of Sectors addressable in LBA Mode
62	0000h	2	Single-word DMA Modes supported
63	0407h	2	Multi-word DMA Modes supported
64	0003h	2	PIO Modes Supported
65	0078h	2	Minimum DMA transfer cycle time per word (ns)
66	0078h	2	Manufacturer's recommended DMA transfer cycle time (ns)
67	0078h	2	Minimum PIO transfer cycle time without flow control (ns)
68	0078h	2	Minimum PIO transfer cycle time with IORDY flow control (ns)
69-70	0000h	4	Reserved
71 –127	0000h	132	Reserved
128 – 159	0000h	64	Vendor Unique
160 - 255	0000h	192	Reserved

6.1.5. Idle – 97h, E3h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Timer Count (5ms increments)							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	97h or E3h							

When issued by the host, the device's internal controller sets the BSY bit, enters the Idle mode, clears the BSY bit, and generates an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power-down mode is enabled. If the sector count is zero, the automatic power-down mode is disabled.

6.1.6. Idle Immediate – 95h, E1h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	95h or E1h							

When issued by the host the device's internal controller sets the BSY bit, enters Idle Mode, clears the BSY bit, and issues an interrupt. The interrupt is issued whether or not the Idle mode is fully entered.

6.1.7. Initialize Drive Parameters – 91h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count (Number of Sectors)							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	0	X	Drive	Head Number (Number of Heads – 1)			
Command	91h							

Initialize Drive Parameters allows the host to set the sector counts per track and the head counts per cylinder to "1" fixed. Upon issuance of the command the device will set the BSY bit and associated parameters, clears the BSY bit and issues an interrupt.

6.1.8. Recalibrate – 1Xh

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	1	LBA	1	Drive	X			
Command	1Xh							

The Recalibrate command sets the Cylinder Low & High, and the Head Number to “0h”, and Sector Number to “1h” in CHS mode. In LBA mode (i.e., LBA = 1) the Sector Number is set to “0h”.

6.1.9. Read Buffer – E4h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	E4h							

This command allows the host to read the contents of the sector buffer. When issued the device sets the BSY bit and sets up the sector buffer data in preparation for the read operation. Once the data is ready, the DRQ bit is set and the BSY bit in the status register are set and cleared, respectively.

6.1.10. Read DMA – C8h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	C8h							

This command allows the host to read data using the DMA transfer protocol.

6.1.11. Read Multiple – C4h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	C4h							

This command executes similarly to the Read Sector command with the exception that, interrupts are issued only when a block containing the counts of sectors defined by the Set Multiple command is transferred.

6.1.12. Read Sector – 20h, 21h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	20h or 21h							

The Read Sector command allows the host to read sectors 1 to 256 as specified in the Sector Count Register. If the Sector count is set to "0h", all 256 Sectors of data will be made available. Once the command code is issued and the first sector of data has been transferred to the buffer the DRQ bit will be set. The Read Sector command is terminated by writing the cylinder, head, and sector number of the last sector read in the task file. On error, the read operation is aborted in the errant sector.

6.1.13. Read Long Sector(s) – 22h, 23h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	X							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	22h or 23h							

The Read Long Sector(s) command operates similarly to the Read Sector(s) command, with the exception that it transfers requested data sectors and ECC data. The long instruction ECC byte transfer for Long commands is a byte transfer at a fixed length of 4 bytes.

6.1.14. Read Verify Sector(s) – 40h, 41h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	40h or 41h							

The Read Verify Sector(s) command operates similarly to the Read Sector(s) command, with the exception that it does not set the DRQ bit and does not transfer data to the host. Once the requested sectors have been verified, the onboard controller clears the BSY bit and issues an interrupt.

6.1.15. Seek – 7Xh

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	X							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	7Xh							

The Seek command seeks and picks up the head to tracks specified in the task file. When the command is issued, the Solid-state memory chips need not be formatted. After an appropriate amount of time the DSC bit is set.

6.1.16. Set Features – EFh

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	Feature							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	EFh							

6.1.16. Set Features – EFh (*continued*)

This command allows the host to configure the Feature Set of the device according to the attributes listed below.

Feature	Operation
01h	Enable 8 bit Data Transfer
66h	Disable Reverting to Power On Defaults
81h	Disable 8 bit Data Transfer
BBh	4 Bytes of Data Apply on Read/Write Long Commands
CCh	Enable revert to Power on Defaults

On Power-up or following a Hardware Reset, the device will be set to the default mode “81h”.

6.1.17. Set Multiple Mode – C6h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	C6h							

The Set Multiple Mode command allows the host to access the drive via Read Multiple and Write Multiple ATA commands. Additionally, the command sets the block count (i.e., the number of sectors within the block) for the Read/Write Multiple command. The sector count per block is set in the Sector Count register.

6.1.18. Set Sleep Mode – 99h, E6h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	99h or E6h							

The Set Sleep Mode command allows the host to set the device in Sleep mode. When the onboard controller transitions to Sleep mode, it clears the BSY bit and issues an interrupt, and the device interface becomes inactive. Sleep mode can be exited by issuing either a hardware or software reset.

6.1.19. Standby – 96h, E2h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Timer Count(5msec x Timer Count)							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	96h or E2h							

The Standby command, when issued by the host will transition the device into the Standby mode. If the Sector Count Register is set to a value other than “0h”, the Auto Power Down function is enabled and the device will return to Idle mode.

6.1.20. Standby Immediate – 94h, E0h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	94h or E0h							

The Standby Immediate command, when issued by the host will transition the device into the Standby mode.

6.1.21. Write Buffer – E8h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	E8h							

The Write Buffer command allows the host to rewrite the contents of the 512 byte data buffer with the desired data.

6.1.22. Write DMA – CAh

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low(LBA15-8)							
Cylinder High	Cylinder High(LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number(LBA27-24)			
Command	CAh							

The Write DMA command allows the host to write data using the DMA transfer protocol.

6.1.23. Write Multiple – C5h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low(LBA15-8)							
Cylinder High	Cylinder High(LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number(LBA27-24)			
Command	C5h							

The Write Multiple command operates in the same manner as the Write Sector command, when issued the device will set the BSY bit within 400nsec, an interrupt is generated at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

6.1.24. Write Sector(s) – 30h, 31h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	30h or 31h							

The Write Sector(s) command writes from 1 to 256 sectors as specified in the Sector Count Register. A Sector count of 0 requests 256 Sectors. When issued the device will set the BSY bit within 400nsec, an interrupt is generated at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

6.1.25. Write Long Sector(s) – 32h, 33h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	32h or 33h							

The Write Long Sector(s) command operates in the same manner as the Write Sector command, when issued the device will set the BSY bit within 400nsec, an interrupt is generated at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

6.1.26. Erase Sector(s) – C0h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	C0h							

The Erase Sector(s) command is issued prior to the issuance of a Write Sector(s) or Write Multiple w/o Erase command.

6.1.27. Request Sense – 03h

Register	D7	D6	D5	D4	D3	D2	D1	D0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	1	X	1	Drive	X			
Command	03h							

The Request Sense command identifies the Extended Error Codes by generated by the preceding ATA command. The Request Sense command must be issues immediately following the detection of an error via the Error Register. Extended Error codes are defined as follows:

Extended Error Codes	Description
00h	No Error Detected
01h	Self Test OK (No Error)
09h	Miscellaneous Error
20h	Invalid Command
21h	Invalid Address (Requested Head or Sector Invalid)
2Fh	Address Overflow (Address Too Large)
35h, 36h	Supply or Generated Voltage Out of Tolerance
11h	Uncorrectable ECC Error
18h	Corrected ECC Error
05h, 30h-32h, 37h,3Eh	Self Test of Diagnostic Failed
10h, 14h	ID Not Found
3Ah	Spare Sectors Exhausted
1Fh	Data Transfer Error/ Aborted Command
0Ch, 38h, 3Bh, 3Ch, 3Fh	Computed Media Format
03h	Write/Erase Failed

6.1.28. Translate Sector – 87h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	87h							

The Translate Sector command is not currently supported by the SiliconSystems' SiliconDrive. If the host issues this command the device will respond with 0x00h in the data register.

6.1.29. Wear Level – F5h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Completion Status							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	Flag			
Command	F5h							

The Wear Level command is supported as a NOP command for the purposes of backward compatibility with the ANSI AT Attachment Standard. This command sets the Sector Count Register to 0x00h after processing this command.

6.1.30. Write Multiple w/o Erase – CDh

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	CDh							

The Write Multiple w/o Erase command functions identically to the Write Multiple command with the exception that the implied pre-erase (i.e., Erase Sector(s) Command) is not issued prior to writing the sectors.

6.1.31. Write Sector(s) w/o Erase – 38h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	38h							

The Write Sector(s) w/o Erase command functions similar to the Write Sector command, however the implied pre-erase (i.e., Erase Sector(s) Command) is not issued prior to writing the sectors.

6.1.32. Write Verify – 3Ch

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	3Ch							

The Write Verify command verifies each sector immediately after it is written. This command performs identically to the Write Sector(s) command with the added feature of verifying each sector written.

7. SALES AND SUPPORT

To order or to obtain information on pricing and delivery, please contact your SiliconSystems Sales Representative.

7.1. Part Numbering Nomenclature

The following table defines the SiliconDrive 2.5" Drive part numbering scheme:

Definition						
SSD-	D	YYY	T	-XXXX		
<i>SiliconSystems Proprietary</i>						
<i>Temp. Range: Blank=Commercial, I=Industrial</i>						
<i>Capacity: 08G=8GB / 12=128MB</i>						
<i>Form Factor: D = 2.5" Drive</i>						
<i>SiliconSystems SiliconDrive</i>						
<i>Operating Temperature Range: Commercial: 0°C to 70°C, Industrial: -40°C to +85°C</i>						
<i>Note: XXXX = 3012 for SiliconDrive 2.5" with DMA support; XXXX = 3021 for DMA disabled. Other configurations are available. Please contact your SiliconSystems Sales Representative for more details.</i>						

Part Number	Description
SSD-D08G-xxxx	8GB SiliconDrive 2.5" Drive, Commercial Temp
SSD-D06G-xxxx	6GB SiliconDrive 2.5" Drive, Commercial Temp
SSD-D04G-xxxx	4GB SiliconDrive 2.5" Drive, Commercial Temp
SSD-D02G-xxxx	2GB SiliconDrive 2.5" Drive, Commercial Temp
SSD-D01G-xxxx	1GB SiliconDrive 2.5" Drive, Commercial Temp
SSD-D51M-xxxx	512MB SiliconDrive 2.5" Drive, Commercial Temp
SSD-D25M-xxxx	256MB SiliconDrive 2.5" Drive, Commercial Temp
SSD-D12M-xxxx	128MB SiliconDrive 2.5" Drive, Commercial Temp

SiliconSystems' performance tests, ratings and product specifications are measured using specific computer systems and/or components and reflect the approximate performance of SiliconSystems' products as measured by those tests. Any difference in system hardware or software design or configuration, as well as system use, may affect actual test results, ratings and product specifications. SiliconSystems may change its product specifications or its products at any time and without notice.

SiliconSystems™, SiliconDrive™, PowerArmor™, and the SiliconSystems logo are trademarks or registered trademarks of SiliconSystems and may be used publicly only with permission from SiliconSystems and require proper acknowledgement. Other listed names and brands are trademarks or registered trademarks of their respective owners.