SiliconDrive™ PC – SSD-Pxxx(I)-3100

Overview

SiliconDrive™ PC is an optimal time-to-market replacement for hard drives and flash cards or in host systems that require low power and scalable storage solutions.

SiliconDrive technology is engineered exclusively for the high performance, high reliability and multi-year product lifecycle requirements of the Enterprise System OEM market. Typical end-market applications include broadband data and voice networks, military systems, flight system avionics, medical equipment, industrial control systems, video surveillance, storage networking, VoIP and wireless infrastructure and interactive kiosks.

Every SiliconDrive is integrated with SiliconSystems patented PowerArmor™ and patent-pending SiSMART™ technology to virtually eliminate storage systems failures.

PowerArmor technology prevents data corruption and loss from power disturbances by integrating proprietary voltage detection circuitry and logic into every SiliconDrive.

SiSMART acts as an early warning system to eliminate unscheduled downtime by constantly monitoring and reporting the exact amount of remaining storage system useful life.

Numerous SiliconSystems patented and patent-pending application-specific technology can be integrated into SiliconDrive to safeguard application data and software IP. Application notes detailing these performance-enhancing options are available under NDA.

Features

- Integrated PowerArmor™ and SiSMART™ Technology
- Capacity Range: 32MB to 16GB
- Supports Both 8 and 16 Bit Data Register Transfers
- Supports Dual Voltage 3.3V or 5V Interface
- Less than 1 Error in 10^{14} Bits Read
- MTBF > 4,000,000 Hours
- ATA-3 Compliant
- RoHS 5 of 6 Compliant
- Supports PIO Modes 0-4 and DMA Modes 0-2

TABLE OF CONTENTS

1. PHYSICAL SPECIFICATIONS 5
   1.1. PHYSICAL DIMENSIONS 5
2. PRODUCT SPECIFICATIONS 6
   2.1. SYSTEM PERFORMANCE 6
   2.2. SYSTEM POWER REQUIREMENTS 6
   2.3. SYSTEM RELIABILITY 6
   2.4. PRODUCT CAPACITY SPECIFICATIONS 7
   2.5. ENVIRONMENTAL SPECIFICATIONS 7
3. ELECTRICAL SPECIFICATIONS 8
   3.1. PIN ASSIGNMENTS 8
   3.2. SIGNAL DESCRIPTIONS 9
   3.3. ABSOLUTE MAXIMUM RATINGS 14
   3.4. CAPACITANCE 14
   3.5. DC CHARACTERISTICS 15
   3.6. AC CHARACTERISTICS 16
      3.6.1. ATTRIBUTE & COMMON MEMORY READ TIMING 16
      3.6.2. ATTRIBUTE & COMMON MEMORY WRITE TIMING 17
      3.6.3. I/O ACCESS READ TIMING 18
      3.6.4. I/O ACCESS WRITE TIMING 19
      3.6.5. TRUE IDE READ/WRITE ACCESS TIMING 21
      3.6.6. TRUE IDE DMA READ/WRITE ACCESS TIMING 22
4. ATTRIBUTE MEMORY DESCRIPTION & OPERATION 22
   4.1. ATTRIBUTE MEMORY READ OPERATIONS 22
   4.2. ATTRIBUTE MEMORY WRITE OPERATIONS 23
   4.3. ATTRIBUTE MEMORY MAP 23
   4.4. CARD INFORMATION STRUCTURE (CIS) 24
   4.5. CONFIGURATION OPTION REGISTER (200H) 36
   4.6. CONFIGURATION & STATUS REGISTER (202H) 37
   4.7. PIN PLACEMENT REGISTER (204H) 37
   4.8. SOCKET & COPY REGISTER (206H) 38
5. COMMON MEMORY DESCRIPTION & OPERATION 39
   5.1. COMMON MEMORY READ OPERATIONS 39
   5.2. COMMON MEMORY WRITE OPERATIONS 39
6. I/O SPACE DESCRIPTION & OPERATION 40
   6.1. I/O SPACE INPUT OPERATIONS 40
   6.2. I/O Space Output Operations 40

7. ATA & TRUE IDE REGISTER DECODING 41
7.1. MEMORY MAPPED REGISTER DECODING 41
7.2. INDEPENDENT I/O MODE REGISTER DECODING 42
7.3. PRIMARY AND SECONDARY I/O MAPPED REGISTER DECODING 43
7.4. TASK FILE REGISTER SPECIFICATION 43
8. ATA REGISTERS 44
8.1. DATA REGISTER 44
8.2. ERROR REGISTER 44
8.3. FEATURE REGISTER 45
8.4. SECTOR COUNT REGISTER 45
8.5. SECTOR NUMBER REGISTER 45
8.6. CYLINDER LOW REGISTER 46
8.7. CYLINDER HIGH REGISTER 46
8.8. DRIVE/HEAD REGISTER 47
8.9. STATUS REGISTER 48
8.10. COMMAND REGISTER 48
8.11. ALTERNATE STATUS REGISTER 49
8.12. DEVICE CONTROL REGISTER 49
8.13. DEVICE ADDRESS REGISTER 50
9. ATA COMMAND BLOCK & SET DESCRIPTION 51
9.1. ATA COMMAND SET 52
9.1.1. CHECK POWER MODE – 98H, E5H 53
9.1.2. EXECUTIVE DRIVE DIAGNOSTIC – 90H 53
9.1.3. FORMAT TRACK – 50H 54
9.1.4. IDENTIFY DRIVE – ECH 54
9.1.4.1. IDENTIFY DRIVE – DRIVE ATTRIBUTE DATA 55
9.1.5. IDLE – 97H, E3H 53
9.1.6. IDLE IMMEDIATE – 95H, E1H 57
9.1.7. INITIALIZE DRIVE PARAMETERS – 91H 57
9.1.8. RECALIBRATE – 1XH 58
9.1.9. READ BUFFER – E4H 58
9.1.10. READ DMA – C8H 58
9.1.11. READ MULTIPLE – C4H 59
9.1.12. READ SECTOR – 20H, 21H 60
9.1.13. LEAD LONG SECTOR(S) – 22H, 23H 60
9.1.14. READ VERIFY SECTOR(S) – 40H, 41H 61
9.1.15. SEEK – 7XH 62
9.1.16. SET FEATURES – EFH 62
9.1.17. SET MULTIPLE MODE – C6H 63
9.1.18. SET SLEEP MODE – 99H, E6H 64
9.1.19. STANDBY – 96H, E2H 64
9.1.20. STANDBY IMMEDIATE – 94H, E0H 65
9.1.21. WRITE BUFFER – E8H 65

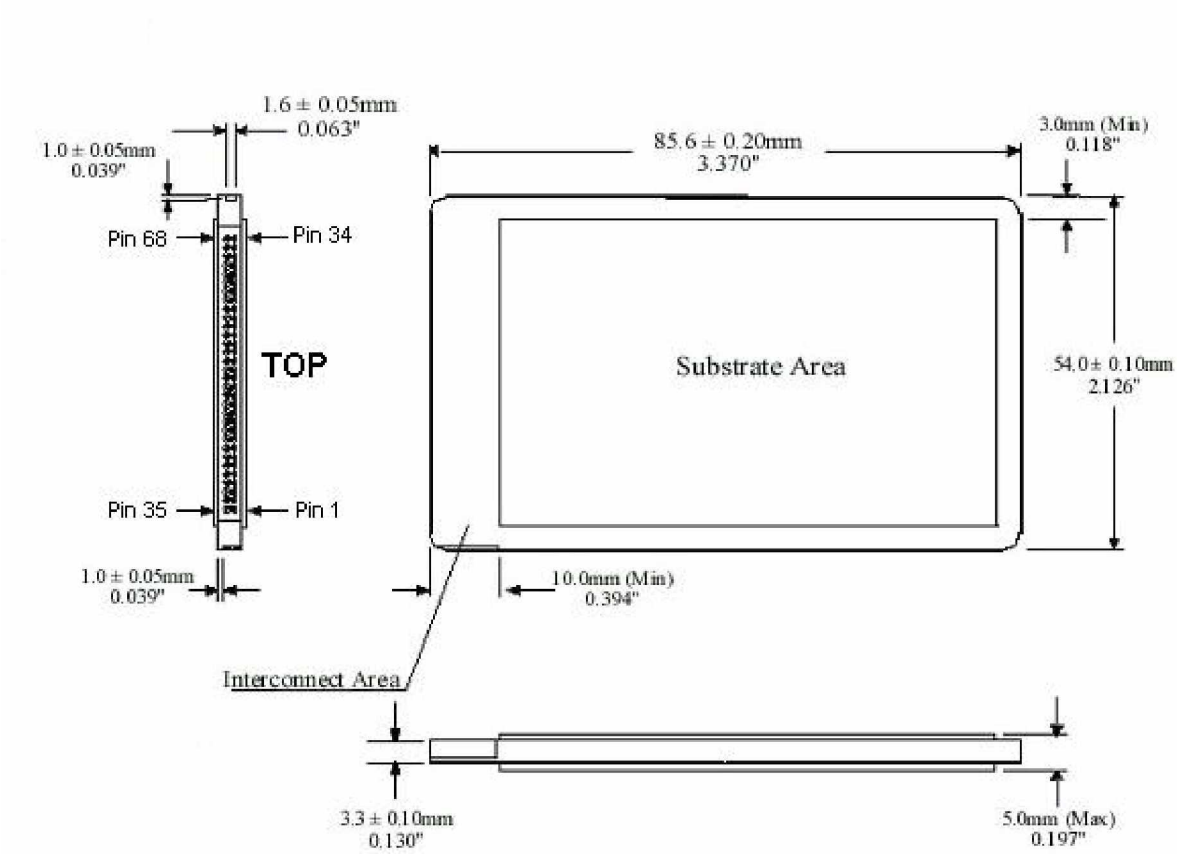
9.1.22. WRITE DMA – CAH 65
9.1.23. WRITE MULTIPLE – C5H 66
9.1.24. WRITE SECTOR(S) – 30H, 31H 67
9.1.25. WRITE LONG SECTOR(S) – 32H, 33H 67
9.1.26. ERASE SECTOR(S) – C0H 68
9.1.27. REQUEST SENSE – 03H 69
9.1.28. TRANSLATE SECTOR – 87H 70
9.1.29. WEAR LEVEL – F5H 70
9.1.30. WRITE MULTIPLE W/O ERASE – CDH 71
9.1.31. WRITE SECTOR(S) W/O ERASE – 38H 71
9.1.32. WRITE VERIFY – 3CH 72
10. SALES AND SUPPORT 74
10.1. PART NUMBERING NOMENCLATURE 74

1. PHYSICAL SPECIFICATIONS

SiliconDrive PC products are offered in an industry standard Type II form factor. Refer to Section 10.1 Part Ordering Nomenclature for details regarding PC capacities.

1.1. Physical Dimensions

The following diagram describes the PC Type II physical dimensions and pin orientation:



2. PRODUCT SPECIFICATIONS[1]

2.1. System Performance

Reset to Ready Startup Time (Typical/Max)	200ms/400ms
Read Transfer Rate (Typical)	8MB/s
Write Transfer Rate (Typical)	6MB/s
Burst Transfer Rate	16.7MB/s
Controller Overhead (Command to DRQ)	2ms (max)

2.2. System Power Requirements

DC Input Voltage	3.3 ± 10%	5.0 ± 10%
Sleep (Standby Current)	<0.5mA	<1.0mA
Read (Typical/Peak)	20mA/75mA	30mA/100mA
Write (Typical/Peak)	30mA/75mA	40mA/100mA

2.3. System Reliability

MTBF (@ 25°C)	> 4,000,000 Hours
Data Reliability	< 1 Non-Recoverable Error in 10^{14} Bits Read
Endurance	>2,000,000 write/erase cycles

[1] All SiliconDrive PC values quoted are typical at 25°C and nominal supply voltage.

2.4. Product Capacity Specifications

Product Density	Formatted Capacity (Bytes)	Number of Sectors	Number of Cylinders	Number of Heads	Number of Sectors/Track
32MB	32,702,464	63,872	499	4	32
64MB	65,601,536	128,128	1001	4	32
128MB	130,154,496	254,208	993	8	32
256MB	260,571,136	508,928	994	16	32
512 MB	521,773,056	1,019,088	1011	16	63
1GB	1,047,674,880	2,046,240	2030	16	63
2GB	2,098,446,336	4,098,528	4066	16	63
4GB	4,224,761,856	8,251,488	8186	16	63
6GB	6,309,789,696	12,323,808	12226	16	63
8GB	8,455,200,768	16,514,064	16383*	16	63
16GB	16,494,428,160	32,215,680	16383*	16	63

* All IDE Drives 8GB and larger use 16383 Cylinders, 16 Heads and 63 Sectors/Track due to interface restrictions.

2.5. Environmental Specifications

Temperature	0ºC to 70ºC (Standard)
	-40ºC to 85ºC (Industrial)
Humidity	8% to 95% non-condensing
Vibration	16.3gRMS, MIL-STD-810F, Method 514.5, Procedure I, Category 24
Shock	1000G, Half-sine, 0.5ms Duration 50g Pk, MIL-STD-810F, Method 516.5, Procedure I
Altitude	80,000ft, MIL-STD-810F, Method 500.4, Procedure II

3. ELECTRICAL SPECIFICATIONS

3.1. Pin Assignments

The following Table describes the SiliconDrive PC 68-Pin Connector Signals:

Pin	PC Card Memory Mode	PC Card I/O Mode	IDE-ATA Mode	Pin	PC Card Memory Mode	PC Card I/O Mode	IDE-ATA Mode
1	GND	GND	GND	35	GND	GND	GND
2	D3	D3	D3	36	CD1#	CD1#	CD1#
3	D4	D4	D4	37	D11[1]	D11[1]	D11[1]
4	D5	D5	D5	38	D12[1]	D12[1]	D12[1]
5	D6	D6	D6	39	D13[1]	D13[1]	D13[1]
6	D7	D7	D7	40	D14[1]	D14[1]	D14[1]
7	CE1#	CE1#	CS0#	41	D15[1]	D15[1]	D15[1]
8	A10	A10	A10[2]	42	CE2#	CE2#	CS1#
9	OE#	OE#	OE#[2]	43	VS1#	VS1#	VS1#
10	N.U.	N.U.	N.U.	44	IORD#	IORD#	IORD#
11	A9	A9	A9[2]	45	IOWR#	IOWR#	IOWR#
12	A8	A8	A8[2]	46	N.U.	N.U.	N.U.
13	N.U.	N.U.	N.U.	47	N.U.	N.U.	N.U.
14	N.U.	N.U.	N.U.	48	N.U.	N.U.	N.U.
15	WE#	WE#	WE#[3]	49	N.U.	N.U.	N.U.
16	RDY/BSY#	IREQ	INTRQ	50	N.U.	N.U.	N.U.
17	Vcc	Vcc	Vcc	51	Vcc	Vcc	Vcc
18	N.U.	N.U.	N.U.	52	N.U.	N.U.	N.U.
19	N.U.	N.U.	N.U.	53	N.U.	N.U.	N.U.
20	N.U.	N.U.	N.U.	54	N.U.	N.U.	N.U.
21	N.U.	N.U.	N.U.	55	N.U.	N.U.	N.U.
22	A7	A7	A7[2]	56	N.U.	N.U.	CSEL#
23	A6	A6	A6[2]	57	VS2#	VS2#	VS2#
24	A5	A5	A5[2]	58	RESET	RESET	RESET#
25	A4	A4	A4[2]	59	WAIT#	WAIT#	IORDY
26	A3	A3	A3[2]	60	INPACK#	INPACK#	DMARQ
27	A2	A2	A2	61	REG#	REG#	DMACK#
28	A1	A1	A1	62	BVD2[3]	SPKR#[3]	DASP#
29	A0	A0	A0	63	BVD1	STSCHG#	PDIAG#
30	D0	D0	D0	64	D8[1]	D8[1]	D8[1]
31	D1	D1	D1	65	D9[1]	D9[1]	D9[1]
32	D2	D2	D2	66	D10[1]	D10[1]	D10[1]
33	WP	IOIS16#	IOCS16#	67	CD2#	CD2#	CD2#
34	GND	GND	GND	68	GND	GND	GND

N.U. = Not Used.

Notes

1. These signals are required only for 16-bit access and not required when installed in 8-bit systems.
2. Should be grounded by the host.

3.2. Signal Descriptions

Signal Name	Pin	Type	Description
A10 - A0 A10 - A0 (PC Card I/O Mode) A2 - A0 (True IDE Mode)	8,11,12,22, 23,24,25,26, 27,28,29 27,28,29	I	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the PC Card, the memory mapped port address registers within the PC Card, a byte in the card's information structure and its configuration control and status registers. This signal is the same as the PC Card Memory Mode signal. In True IDE Mode only A[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode) -STSCHG (PC Card I/O Mode) -PDIAG (True IDE Mode)	63	I/O	This signal is asserted high, as BVD1 is not supported. This signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Configuration and Status Register. In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.
BVD2 (PC Card Memory Mode) -SPKR (PC Card I/O Mode) -DASP (True IDE Mode)	62	I/O	This signal is asserted high, as BVD2 is not supported. This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated. In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card Memory Mode) -CD1, -CD2 (PC Card I/O Mode) . -CD1, -CD2 (True IDE Mode)	36,37	O	These Card Detect pins are connected to ground on the PC Card. They are used by the host to determine that the PC Card is fully inserted into its socket. This signal is the same for all modes. This signal is the same for all modes.

3.2. Signal Descriptions

Signal Name	Pin	Type	Description
-CE1, -CE2 (PC Card Memory Mode) -CE1, -CE2 (PC Card I/O Mode) -CS0, -CS1 (True IDE Mode)	7,42	I	The Card Enable signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. –CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7. See Sections 4.1, 4.2, 5.1, and 5.2. This signal is the same as the PC Card Memory Mode signal. Refer to Sections 6.1 and 6.2. In the True IDE Mode CS0 –CS1 is the chip select for the task file registers while CS2 is used to select the Alternate Status Register and the Device Control Register.
-CSEL (PC Card Memory Mode) -CSEL (PC Card I/O Mode) -CSEL (True IDE Mode)	56	I	This signal is not used for this mode. This signal is not used for this mode. Cable Select is an internally pulled up signal used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
D15 - D00 (PC Card Memory Mode) D15 - D00 (PC Card I/O Mode) D15 - D00 (True IDE Mode)	41,40,39,38, 37,66,65,64, 6,5,4,3,2, 32, 31, 30	I/O	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word. This signal is the same as the PC Card Memory Mode signal. In True IDE Mode, all Task File operations occur in byte mode on the low order bus D00-D07 while all data transfers are 16 bit using D00-D15.
GND (PC Card Memory Mode) GND (PC Card I/O Mode) GND (True IDE Mode)	1,34,35,68	---	Ground. This signal is the same for all modes. This signal is the same for all modes.

3.2. Signal Descriptions

Signal Name	Pin	Type	Description
-INPACK (PC Card Memory Mode) -INPACK (PC Card I/O Mode) DMARQ (True IDE Mode)	60	O	This signal is not used in this mode. The Input Acknowledge signal is asserted by the PC Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the PC Card and the CPU. In True IDE Mode this signal is used for DMA transfers between the host and device. DMARQ shall be asserted by the device when the device is ready to transfer data to/from the host. The direction of data transfer is controlled by –IORD and –IOWR. This signal is used in a handshake manner with –DMACK, i.e. the device shall wait until the host asserts -DMACK before negating DMARQ, and re-assert DMARQ if there is more data to transfer. The DMARQ/-DMACK handshake is used to provide flow control during the transfer.
-IORD (PC Card Memory Mode) -IORD (PC Card I/O Mode) -IORD (True IDE Mode)	44	I	This signal is not used in this mode. This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the PC Card when the card is configured to use the I/O interface. In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
-IOWR (PC Card Memory Mode) -IOWR (PC Card I/O Mode) -IOWR (True IDE Mode)	45	I	This signal is not used in this mode. The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the PC Card controller registers when the PC Card is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge). In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
-OE (PC Card Memory Mode) -OE (PC Card I/O Mode) -ATA SEL (True IDE Mode)	9	I	This is an Output Enable strobe generated by the host interface. It is used to read data from the PC Card in Memory Mode and to read the CIS and configuration registers. In PC Card I/O Mode, this signal is used to read the CIS and configuration registers. To enable True IDE Mode this input should be grounded by the host.

3.2. Signal Descriptions

Signal Name	Pin	Type	Description
-RDY/-BSY (PC Card Memory Mode) -IREQ (PC Card I/O Mode) -IREQ (True IDE Mode)	16	O	In Memory Mode this signal is set high when the PC Card is ready to accept a new data transfer operation and held low when the card is busy. The Host memory card socket must provide a pull-up resistor. At power up and at Reset, the RDY/-BSY signal is held low (busy) until the PC Card has completed its power up or reset function. No access of any type should be made to the PC Card during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true: The PC Card has been powered up with --RESET continuously disconnected or asserted. I/O Operation – After the PC Card has been configured for I/O operation, this signal is used as the Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt. In True IDE Mode signal is the active high Interrupt Request to the host.
-REG (PC Card Memory Mode) -REG (PC Card I/O Mode) -DMACK (True IDE Mode)	61	I	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory. The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus. In True IDE Mode this signal is used by the host in response to DMARQ to initiate DMA transfers. The DMARQ/-DMACK handshake is used to provide flow control during the transfer. When –DMACK is asserted, -CS0 and –CS1 shall not be asserted and transfers shall be 16-bits wide.
-RESET (PC Card Memory Mode) -RESET (PC Card I/O Mode) -RESET (True IDE Mode)	58	I	When the pin is high, this signal Resets the PC Card. The PC Card is Reset only at power up if this pin is left high or open from power-up. The PC Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set. This signal is the same as the PC Card Memory Mode signal. In the True IDE Mode this input pin is the active low hardware reset from the host.

3.2. Signal Descriptions

Signal Name	Pin	Type	Description
VCC (PC Card Memory Mode) VCC (PC Card I/O Mode) VCC (True IDE Mode)	17,51	-	+5 V, +3.3 V power. This signal is the same for all modes. This signal is the same for all modes.
-VS1, -VS2 -VS1, -VS2 (PC Card I/O Mode) -VS1, -VS2 (True IDE Mode)	43,57	O	Voltage Sense Signals. -VS1 is grounded so that the PC Card CIS can be read at 3.3 volts and -VS2 is reserved by PC Card for a secondary voltage. This signal is the same for all modes. This signal is the same for all modes.
-WAIT (PC Card Memory Mode) -WAIT (PC Card I/O Mode) -IORDY (True IDE Mode)	59	O	The -WAIT signal is driven low by the PC Card to signal the host to delay completion of a memory or I/O cycle that is in progress. This signal is the same as the PC Card Memory Mode signal. In True IDE Mode this output signal may be used as IORDY.
-WE (PC Card Memory Mode) -WE (PC Card I/O Mode) -WE (True IDE Mode)	15	I	This is a signal driven by the host and used for strobing memory write data to the registers of the PC Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers. In PC Card I/O Mode, this signal is used for writing the configuration registers. In True IDE Mode this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode) -IOIS16 (PC Card I/O Mode) -IOIS16 (True IDE Mode)	33	O	Write Protect Memory Mode – The PC Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence. I/O Operation – When the PC Card is configured for I/O Operation, Pin 33 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port. In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

3.3. Absolute Maximum Ratings

Vcc = 3.3 ± 10%

Symbol	Parameter	Min	Max	Units
Ts	Storage Temperature	-55	125	°C
T_A	Operating Temperature	-40	85	°C
Vcc	Vcc with Respect to GND	-0.3	6.7	V
Vin	Input Voltage	-0.5	3.8	V
Vout	Output Voltage	-0.3	3.6	V

Vcc = 5.0 ± 10%

Symbol	Parameter	Min	Max	Units
Ts	Storage Temperature	-55	125	°C
T_A	Operating Temperature	-40	85	°C
Vcc	Vcc with Respect to GND	-0.3	6.7	V
Vin	Input Voltage	-0.5	6.0	V
Vout	Output Voltage	-0.3	5.8	V

3.4. Capacitance

Symbol	Parameter	Max	Units
Cin	Input Capacitance	35	pF
Cout	Output Capacitance	35	
CI/O	Bi-directional Capacitance	35	

3.5. DC Characteristics

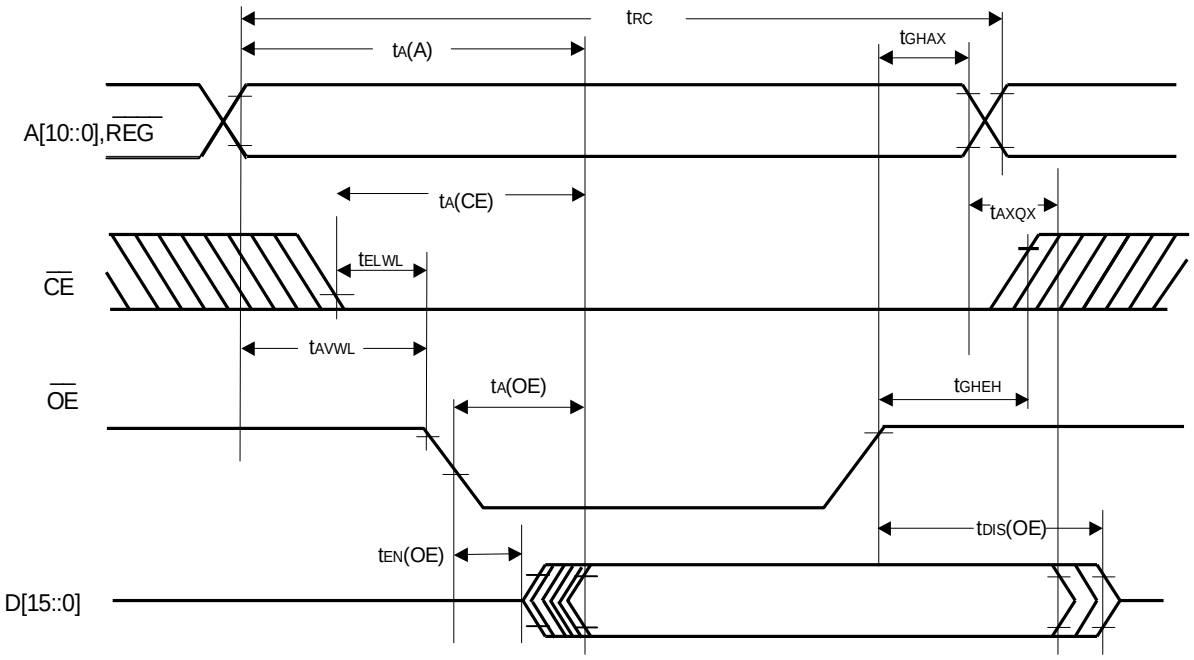
Symbol	Parameter	3.3 V ±10%		5V ±10%		Units
		Min.	Max.	Min.	Max.	
Vcc	Power Supply Voltage	3.0	3.6	4.5	5.5	V
I_{LI}	Input Leakage *(1) Current		5		5	µA
I_{LO}	Output Leakage *(1) Current		5		5	µA
V_{CCR}	Vcc Read Current		50	-	80	mA
V_{CCW}	Vcc Write Current		50	-	80	mA
V_{CCS}	Vcc Standby Current		.3	-	.5	mA
V_{IL}	Input LOW Voltage	-0.3	.3 x Vcc	-0.3	.3 x Vcc	V
V_{IH}	Input HIGH Voltage	.7 x Vcc	Vcc + .3	.7 x Vcc	Vcc + .3	V
V_{OL}	Output LOW Voltage	-	.4		.4	V
V_{OH}	Output HIGH Voltage	Vcc – 0.4		Vcc – 0.4		V

Note

*(1) Except pulled up/pulled down pin.

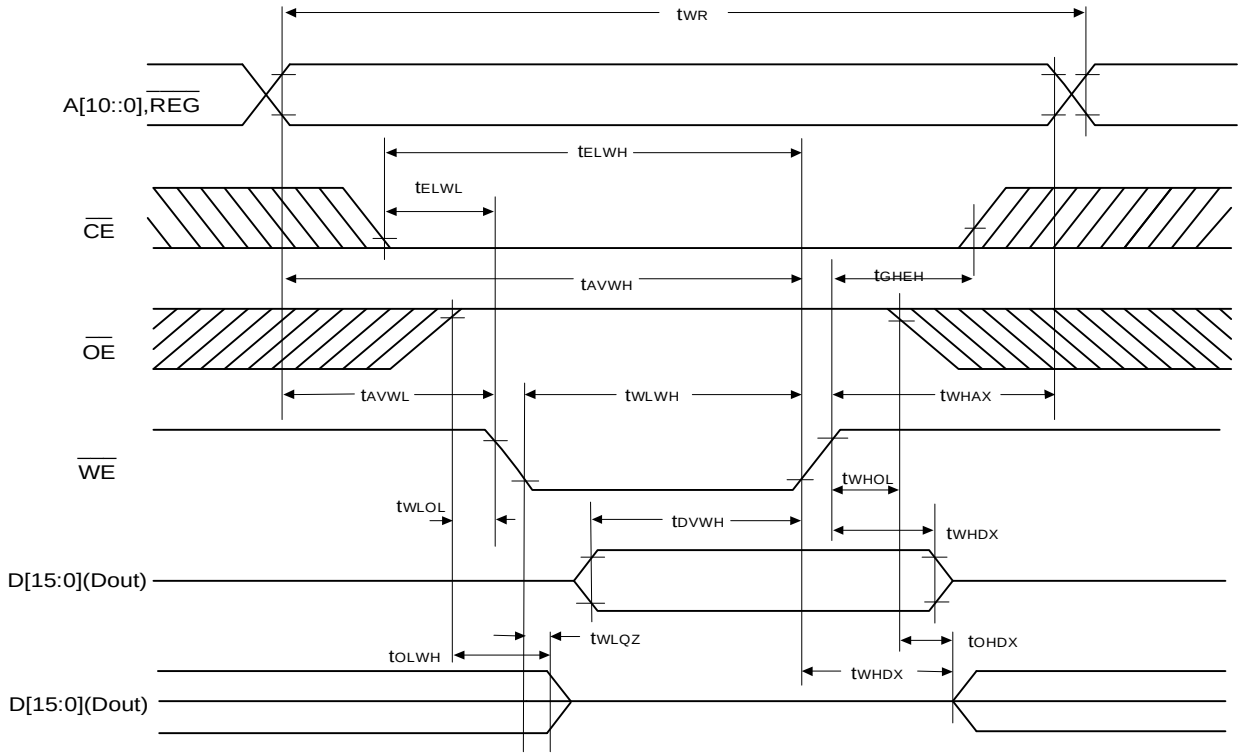
3.6. AC Characteristics

3.6.1. Attribute & Common Memory Read Timing



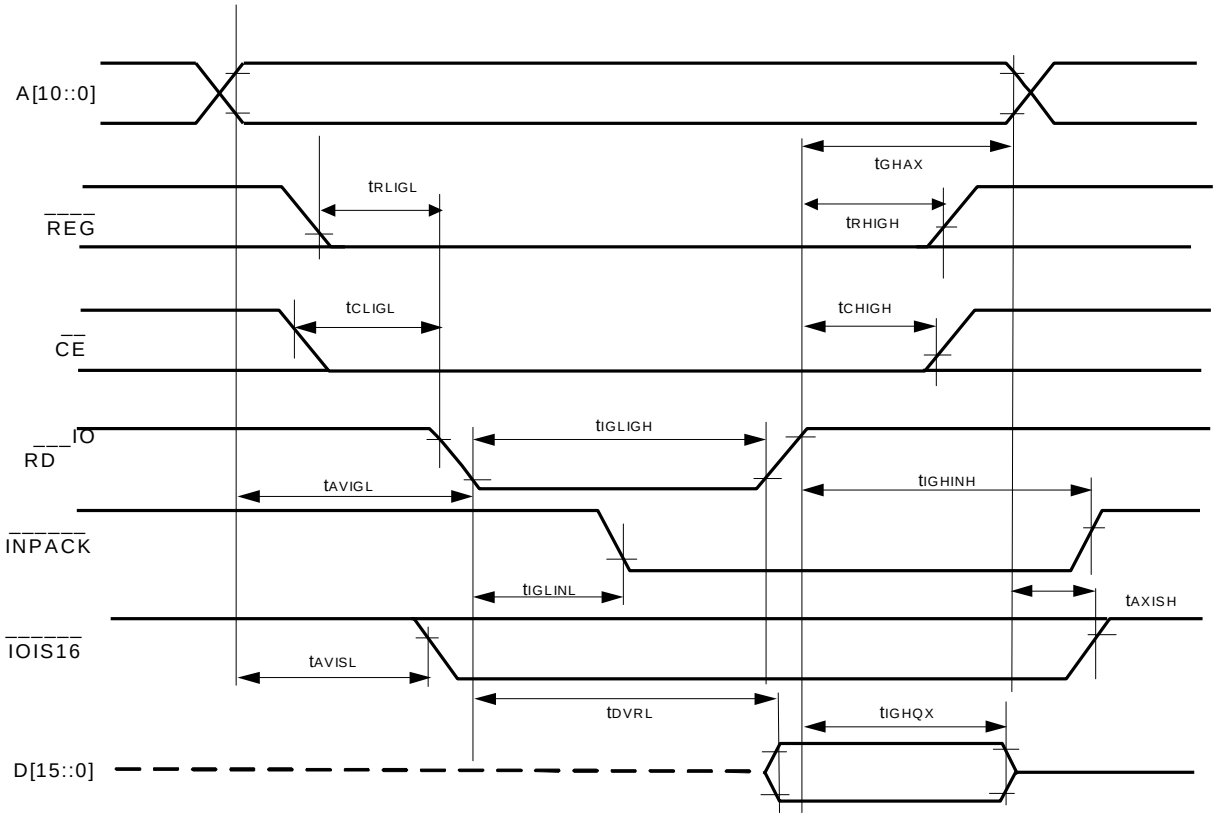
Symbol	Parameter	Min	Max	Units
t_{RC}	Read Cycle Time	100		nsec
$t_{A}(A)$	Address Access Time	-	100	
$t_{A}(CE)$	Card Enable Access Time	-	100	
$t_{A}(OE)$	Output Enable Access Time	-	50	
$t_{DIS}(OE)$	Output Disable Time from OE	-	50	
$t_{EN}(OE)$	Output Enable Time from OE	5	-	
t_{AXQX}	Data Valid from Address Change	0	-	
t_{AVWL}	Address Setup Time	10	-	
t_{AXQX}	Address Hold Time	15	-	
t_{ELWL}	Card Enable Setup Time before OE	0	-	
t_{GHEH}	Card Enable Hold Time following OE	15	-	

3.6.2. Attribute & Common Memory Write Timing



Symbol	Parameter	Min	Max	Units
t_{WR}	Write Cycle Time	100	-	nsec
t_{WLWH}	Write Pulse Width	60	-	
t_{AVWL}	Address Setup Time	10	-	
t_{AVWH}	Address Setup Time for WE	70	-	
t_{ELWH}	Card Enable Setup Time for WE	70	-	
t_{WHDX}	Data Hold Time	10	-	
t_{WHAX}	Write Recover Time	15	-	
t_{WLQZ}	Output Disable Time from WE	-	75	
t_{OLWH}	Output Disable Time from OE	-	100	
t_{WHOX}	Output Enable Time from WE	5	-	
t_{OHDX}	Output Enable Time from OE	5	-	
t_{WLOL}	Output Enable Setup for WE	10	-	
t_{WHOL}	Output Enable Hold from WE	10	-	
t_{ELWL}	Card Enable Setup Time before WE	0	-	
t_{GHEH}	Card Enable Hold Time from WE	15	-	
t_{DVWH}	Data Setup Time	40	-	

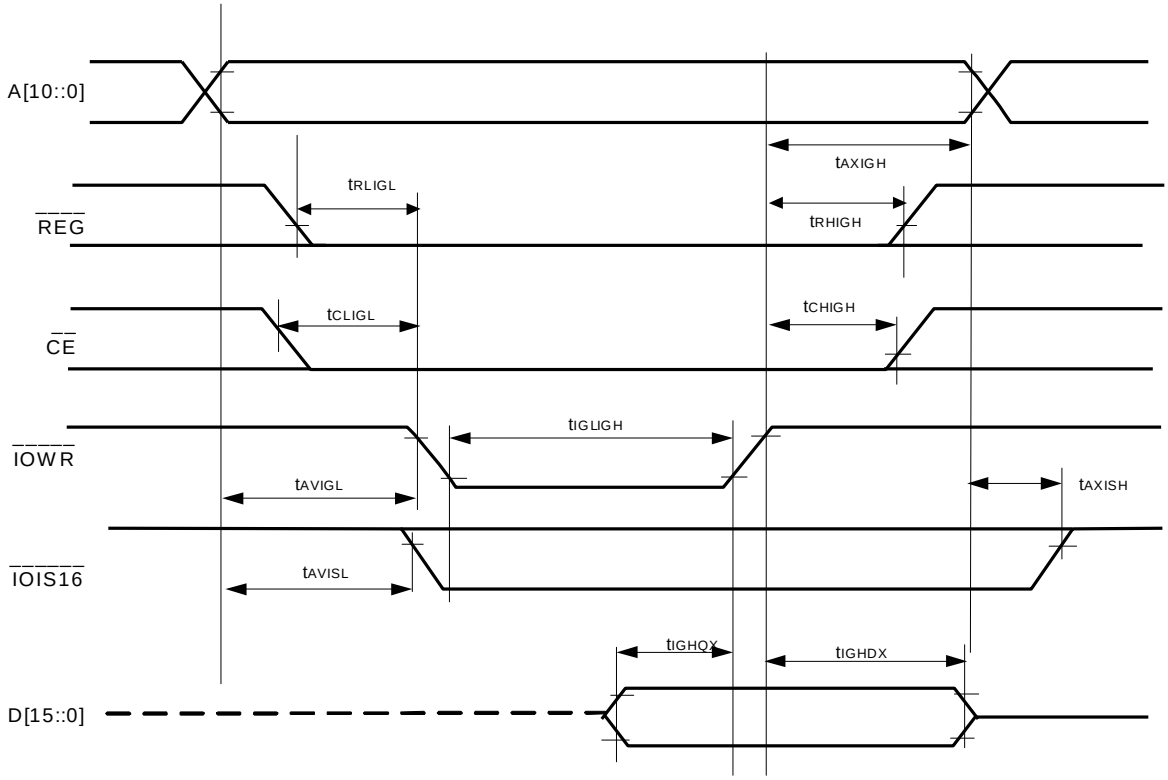
3.6.3. I/O Access Read Timing



Symbol	Parameter	Min	Max	Units
t_{DVRL}	Data Delay after IORD	-	50	nsec
t_{IGHQX}	Data Hold following IORD	5	-	
t_{IGLIGH}	IORD Pulse Width	65	-	
t_{AVIGL}	Address Setup before IORD	25	-	
t_{GHAX}	Address Hold following IORD	10	-	
t_{CLIGL}	CE Setup before IORD	5	-	
t_{CHIGH}	CE Hold following IORD	10	-	
t_{RLIGL}	REG Setup before IORD	5	-	
t_{RHIGH}	REG Hold following IORD	0	-	
t_{IGLINL}	INPACK Delay falling from IORD	-	(1)	
t_{IGHINH}	INPACK Delay Rising from IORD	-	(1)	
t_{AVISL}	IOIS16 Delay Falling from Address	-	(1)	
t_{AXISH}	IOIS16 Delay Rising from Address	-	(1)	

Note: 1) IOIS16 and INPACK is not supported.

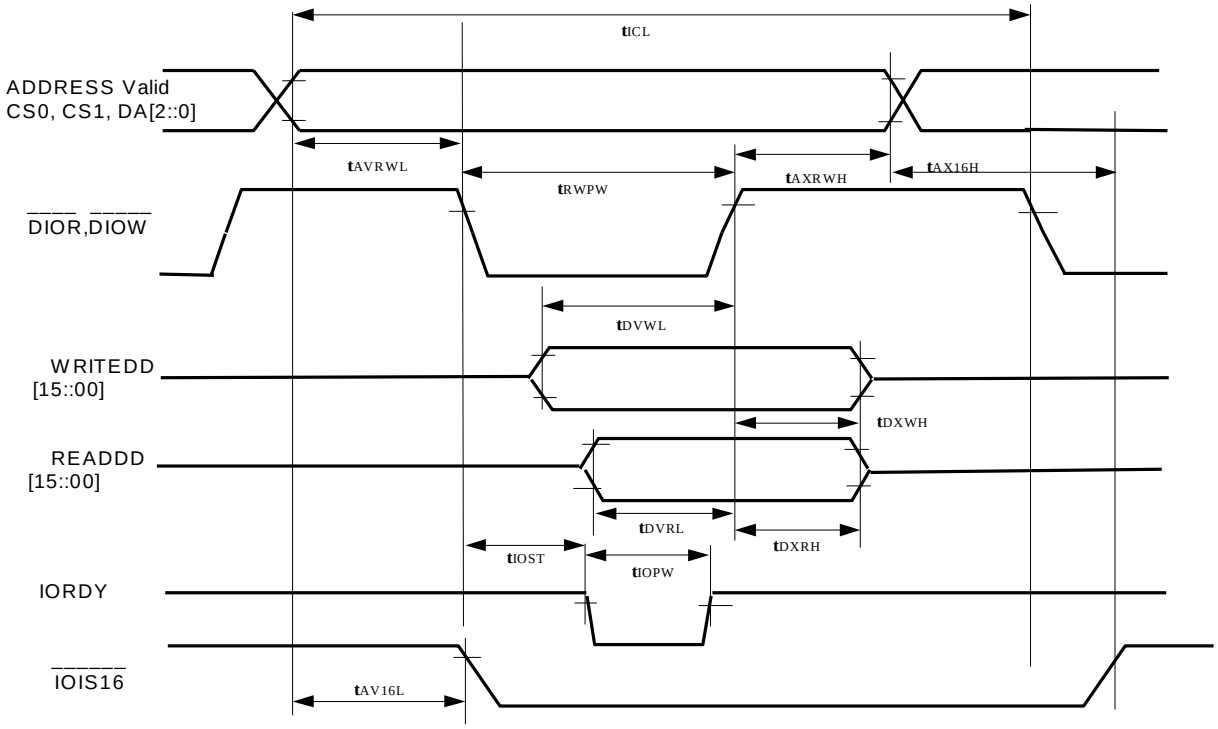
3.6.4. I/O Access Write Timing



Symbol	Parameter	Min	Max	Units
t_{IGHDX}	Data Hold following IOWR	5	-	nsec
t_{IGHQX}	Data Setup before IOWR	20	-	
t_{IGLIGH}	IOWR Pulse Width	65	-	
t_{AVIGL}	Address Setup before IOWR	25	-	
t_{AXIGH}	Address Hold following IOWR	10	-	
t_{CLIGL}	CE Setup before IOWR	5	-	
t_{CHIGH}	CE Hold following IOWR	10	-	
t_{RLIGL}	REG Setup before IOWR	5	-	
t_{RHIGH}	REG Hold following IOWR	0	-	
t_{AVISL}	IOIS16 Delay Falling from Address	-	(1)	
t_{AXISH}	IOIS16 Delay Rising from Address	-	(1)	

Note: 1) IOIS16 and INPACK is not supported.

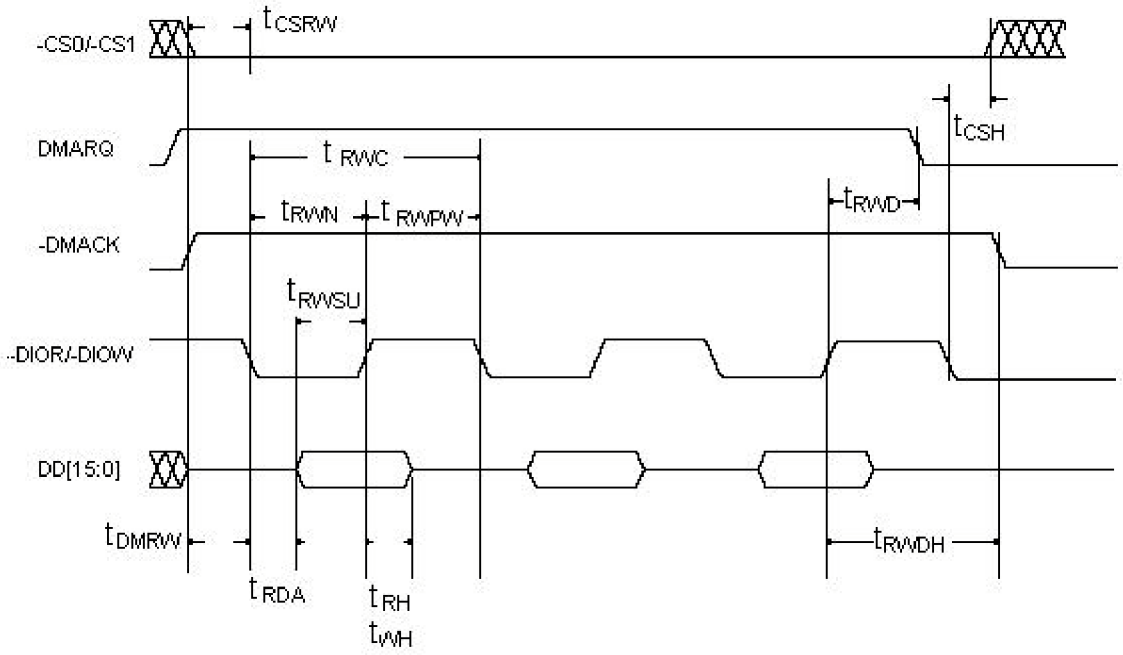
3.6.5. True IDE Read/Write Access Timing



Symbol	Parameter	Min	Max	Units
t_{ICL}	Cycle Time	100	-	nsec
t_{AVRWL}	Address Valid to DIOR,DIOW Setup Time	15	-	
t_{RWPW}	DIOR, DIOW Pulse Width	65	-	
t_{DVWL}	DIOW Data Setup Time	20	-	
t_{DXWH}	DIOW Data Hold Time	5	-	
t_{DVRL}	DIOR Data Setup Time	15	-	
t_{DXRH}	DIOR Data Hold Time	5	-	
t_{AV16L}	Address Valid to IOCS16 Assertion	-	(1)	
t_{AX16H}	Address Valid to IOCS16 Negation	-	(1)	
t_{AXRWH}	DIOW,DIOR to Address Valid Hold Time	10	-	
t_{IOST}	IORDY Setup Time	-	(1)	
t_{IOPW}	IORDY Pulse Width	-	(1)	

Note: 1) IOIS16 and INPACK is not supported.

3.6.6. True IDE DMA Read/Write Access Timing*



Symbol	Parameter	Min	Max	Units
t_{RWC}	Cycle Time (Mode 2)	100	-	nsec
t_{RWPW}	DIOR/DIOW Pulse Width	65	-	
t_{RDA}	DIOR Data Access	-	50	
t_{RWSU}	DIOR/DIOW Data Setup Time	15	-	
t_{WH}	DIOW Data Hold Time	5	-	
t_{RH}	DIOR Data Hold Time	5	-	
t_{DMRW}	DMACK to DIOR/DIOW Setup Time	0	-	
t_{RWDH}	DIOR/DIOW to DMACK Hold Time	5	-	
t_{RWN}	DIOR/DIOW negated Pulse Width	25	-	
t_{RWD}	DIOR/DIOW to DMARQ Delay	-	35	
t_{CSRW}	CS(1:0) valid to DIOR/DIOW	10	-	
t_{CSH}	CS(1:0) Hold Time	10	-	

* Does not apply to SiliconDrives that have DMA disabled.

4. ATTRIBUTE MEMORY DESCRIPTION & OPERATION

The Attribute Memory plane can be read or written to by asserting the REG# signal, qualified by the appropriate combination of CE1#, OE# and WE#. An Attribute memory map describing the type and location of the information maintained in the Attribute memory plane is provided in Section 4.3. Attribute Memory Map.

With respect to SiliconDrive PC, Attribute memory consists of two sections, the Card Information Structure (CIS) and the Function Configuration Registers (FCR). The CIS contains a description of the card's capabilities and specifications. The FCR consists of four registers, which can be read or written to by a host to configure the SiliconDrive PC for specific purposes.

4.1. Attribute Memory Read Operations

Attribute memory read operations are enabled by asserting REG# , OE#, and CE1# low. Odd byte read operations from the attribute memory plane are not valid.

Function Mode	REG#	CE1#	CE2#	A0	OE#	WE#	D[15:8]	D[7:0]
Standby	L	H	H	X	X	X	High-Z	High-Z
Byte Access	L	L	H	L	L	H	High-Z	Even
	L	H	L	H	L	H	High-Z	Not Valid
Word Access	L	L	L	X	L	H	Not Valid	Even
Odd Byte Only Access	L	L	H	X	H	H	Not Valid	High-Z

4.2. Attribute Memory Write Operations

Attribute memory write operations are enabled by asserting REG#, WE# and CE1# low. Odd byte write operations from the attribute memory plane are not valid.

Function Mode	REG#	CE1#	CE2#	A0	OE#	WE#	D[15:8]	D[7:0]
Standby	L	H	H	X	X	X	High-Z	High-Z
Byte Access	L	L	H	L	H	L	High-Z	Even
	L	H	L	H	H	L	High-Z	Not Valid
Word Access	L	L	L	X	H	L	Not Valid	Even
Odd Byte Only Access	L	L	H	X	H	H	Not Valid	High-Z

4.3. Attribute Memory Map

As stated earlier, the Attribute Memory plane is comprised to two components the Card Information Structure (CIS) and the Function Configuration Registers (FCR). The following tables detail the type, location and read/write requirements for each of the four FCR's maintained in the Attribute Memory plane.

Register	Operation	Addr	CE1#	REG#	WE#	OE#
Card Information Structure	READ	X	0	0	1	0
	WRITE	X	0	0	0	1
Configuration Option Register	READ	200h	0	0	1	0
	WRITE	200h	0	0	0	1
Card Configuration & Status Register	READ	202h	0	0	1	0
	WRITE	202h	0	0	0	1
Pin Replacement Register	READ	204h	0	0	1	0
	WRITE	204h	0	0	0	1
Socket and Copy Register	READ	206h	0	0	1	0
	WRITE	206h	0	0	0	1

4.4. Card Information Structure (CIS)

The CIS is data, which describes the SiliconDrive PC and is described by the PC Card standard. This information can be used by the Host system to determine a number of things about the SiliconDrive PC that has been inserted. For information regarding the exact nature of this data, and how to design Host software to interpret it, refer to the PC Card standard Metaformat Specification.

4.4. Card Information Structure (CIS)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
00h	01h	CISTPL_DEVICE								Device Info Tuple	Tuple Code
02h	03h									Link length is 3 byte	Link to Next Tuple
04h	D9h	Device Type Code Dh= I/O				W 1	Device Speed		1	I/O device No WP Speed = 100ns	Device ID WPS Device Speed
06h	01h	1X					2k			2k byte of Address Space	Device Size
08h	FFh	List end Marker								End of device	END marker
0Ah	1Ch	CISTPL_DEVICE_OC								Other conditions device in Tuple code	Tuple code
0Ch	04h	TPL_LINK								Link Length is 4 Bytes	Link to Next Tuple
0Eh	02h	EXT Reserved		VCC				MWAIT		3V, wait is Not Used	Other Conditions Info Field
10h	D9h	Device type		W P S		Device speed				Device type = DH: I/O device WPS = 1: No WP Device speed = 1: 250 ns	
12h	01h	1x					2k units			2k byte of address space	Device size
14h	FFh	List end marker								End of device	END marker
16h	18h	CISTPL_JEDEC_C								JEDEC ID common memory	Tuple code
18h	02h	TPL_LINK								Link length is 2 bytes	Link to next tuple
1Ah	DFh	PCMCIA Manufacturer's JEDEC								Manufacturer's ID code	JEDEC ID
1Ch	01h	PCMCIA JEDEC Device Code								2nd byte of JEDEC ID	
1Eh	20h	CISTPL_MANFID								Manufacturer's ID code	Tuple Code
20h	04h	TPL_LINK									
22h	00h	Low byte of PCMCIA manufacturer's code								JEDEC manufacturer's ID	Low byte of manufacturer's code
24h	00h	High byte of PCMCIA manufacturer's code								Code of 0 because other byte is JEDEC 1 byte manufacturer's ID	High byte of manufacturer's code
26h	00h	Low byte of product code								Manufacturer's code for SiliconDrive CF	Low byte of product code
28h	00h	High byte of product code								Manufacturer's code for SiliconDrive CF	High byte of product code
2Ah	21h	CISTPL_FUNCID								Function ID tuple	Tuple code

4.4. Card Information Structure (CIS)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
2Ch	02h	TPL_LINK								Link length is 2bytes	Link to next tuple
2Eh	04h	TPLFID_FUNCTION = 04H								Disk function, may be silicon, may be removable	PC card function code
30h	01h	Reserved						R	P	R = 0: No BIOS ROM P = 1: Configure card at power on	System initialization byte
32h	22h	CISTPL_FUNCE								Function extension tuple	Tuple code
34h	02h	TPL_LINK								Link length is 2 bytes	Link to next tuple
36h	01h	Disk function extension tuple type								Disk interface type	Extension tuple type for disk
38h	01h	Disk interface type								PC card interface type	Interface type
3Ah	22h	CISTPL_FUNCE								Function extension tuple	Tuple code
3Ch	03h	TPL_LINK								Link length is 3 bytes	Link to next tuple
3Eh	02h	Disk function extension Tuple type								Basic PCMCIA-ATA extension Tuple	Extension Tuple type for disk
40h	04h	Reserved			D	U	S	V		No Vpp, silicon,single drive V = 0: No Vpp required S = 0: Silicon U = 1: Unique serial # D = 0: Single drive on card	Basic ATA option parameters byte 1
42h	07h	R	I	E	N	P3	P2	P1	P0	P0: Sleep mode supported P1: Standby mode supp. P2: Idle mode supported P3: Drive auto power ctl N: Some config excludes 3X7 E: Index bit is emulated I: Twin IOIS16# data reg only R: Reserved	Basic ATA option parameters byte 2
44h	1Ah	CISTPL_CONFIG								Configuration tuple	Tuple code
46h	05h	TPL_LINK								Link length is 5 bytes	Link to next tuple
48h	01h	RFS		RMS			RAS			RFS: Reserved RMS: TPCC RMSK size-1 = 0 RAS: TPCC_RADR size-1 = 1 1 byte register mask 2 byte config base address	Size of fields byte TPCC_SZ
4Ah	07h	TPCC_LAST								Entry with config index of 7 is final entry in table	Last entry of config registers
4Ch	00h	TPCC_RADR (LSB)								Config. Reg. are located at 200H in REG space	Location of configuration registers
4Eh	02h	TPCC_RADR (MSB)									
50h	0Fh	Reserved			S	P	C	I		I: Configuration index C: Configuration and status P: Pin replacement S: Socket and copy	Configuration registers present mask TPCC_RMSK

4.4. Card Information Structure (CIS)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
52h	1Bh	CISTPL_TABLE_ENTRY								Configuration table entry tuple	Tuple code
54h	0Bh	TPL_LINK								Link length is 11 bytes	Link to next tuple
56h	C0h	I	D	Configuration index						Memory mapped I/O configuration I = 1: Interface byte follows D = 1: Default entry Configuration index = 0	Configuration table index byte TPCE_INDX
58h	C0h	W	R	P	B	Interface type				W = 0: Wait not used R = 1: Ready active P = 0: WP used B = 0: BVD1 and BVD2 not used IF type = 0: Memory interface	Interface description field TPCE_IF
5Ah	A1h	M	MS	IR	IO	T	P			M = 1: Misc info present MS = 01: Memory space info single 2-byte length IR = 0: No interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: VCC only info	Feature selection byte TPCE_FS
5Ch	27h	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for VCC
5Eh	55h	X	Mantissa			Exponent				Nominal voltage = 5 V	VCC nominal value
60h	4Dh	X	Mantissa			Exponent				VCC nominal 4.5V	VCC min value
62h	5Dh	X	Mantissa			Exponent				VCC nominal 5.5V	VCC max value
64h	75h	X	Mantissa			Exponent				Max average current over10msec is 80mA	Max average current
66h	08h	Length in 256 bytes pages (LSB)								Length of memory space is 2kB	Memory space description structures (TPCE_MS)
68h	00h	Length in 256 bytes pages (MSB)									
6Ah	21h	X	R	P		RO		A	T	X = 0: No more misc fields R: Reserved P = 1: Power down supported RO = 0: Not read only mode	Miscellaneous features field TPCE_MI

4.4. Card Information Structure (CIS)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
										A = 0: Audio not supported T = 0: Single drive	
6Ch	1Bh	CISTPL_TABLE_ENTRY								Configuration table entry tuple	Tuple Code
6Eh	06h	TPL_LINK								Link length is 6 bytes	Link to next tuple
70h	00h	I	D	Configuration index						Memory mapped I/O configuration I = 0: No Interface byte D = 0: No Default entry Configuration index = 0	Configuration table index byte TPCE_INDX
72h	01h	M	MS		IR	IO	T		P	M = 0: No Misc info MS = 00: No Memory space info IR = 0: No interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: VCC only info	Feature selection byte TPCE_FS
74h	21h	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for VCC
76h	B5h	X	Mantissa			Exponent				Nominal voltage = 3.0 V	VCC nominal value
78h	1Eh	Extension								+0.3 V	Extension byte
7Ah	4Dh	X	Mantissa			Exponent				Max average current over 10msec is 45 mA	Max. average current
7Ch	1Bh	CISTPL_TABLE_ENTRY								Configuration table entry Tuple	Tuple code
7Eh	0Dh	TPL_LINK								Link length is 10 bytes	Link to next tuple
80h	C1h	I	D	Configuration	INDEX					Contiguous I/O mapped ATA registers configuration I = 1: Interface byte follows D = 1: Default entry Configuration index = 1	Configuration table index byte TPCE_INDX
82h	41h	W	R	P	B	Interface type				W = 0: Wait not used R = 1: Ready active P = 0: WP not used B = 0: BVS1 and BVD2 not used IF type = 1: I/O interface	Interface description field TPCE_IF

4.4. Card Information Structure (CIS)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
84h	99h	M	MS	IR	IO	T			P	M = 1: Misc info present MS = 00: No memory space info IR = 1: Interrupt info present IO = 1: I/O port info present T = 0: No timing info present P = 1: VCC only info	Feature selection byte TPCE_FS
86h	27h	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down Curr. info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for VCC
88h	55h	X	Mantissa			Exponent				Nominal voltage = 5 V	VCC nominal value
8Ah	4Dh	X	Mantissa			Exponent				VCC nominal 4.5V	VCC min value
8Ch	5Dh	X	Mantissa			Exponent				VCC nominal 5.5V	VCC max value
8Eh	75h	X	Mantissa			Exponent				Max average current over10msec is 80mA	Max average current
90h	64h	R	S	E	I	O	AddrLine			S = 1: 16-bit hosts supported E = 1: 8-bit hosts supported IO AddrLine: 4 lines decoded	I/O space description field TPCE_IO
92h	F0h	S	P	L	M	V	B	I	N	S = 1: Share logic active P = 1: Pulse mode IRQ supported L = 1: Level mode IRQ supported M = 1: Bit mask of IRQs present V = 0: No vender unique IRQ B = 0: No bus error IRQ I = 0: No IO check IRQ N = 0: No NMI	Interrupt request description structure TPCE_IR
94h	FFh	IRQ 7	IRQ 6	IRQ 5	IRQ 4	IRQ 3	IRQ 2	IRQ 1	IRQ 0	IRQ level to be routed 0 to 15 recommended	Mask extension byte 1 TPCE_IR
96h	FFh	IRQ 15	IRQ 14	IRQ 13	IRQ 12	IRQ 11	IRQ 10	IRQ 9	IRQ 8	Recommended routing to any “normal, maskable” IRQ.	Mask extension byte 2 TPCE_IR
98h	21h	X	R	P	R	O	A	T		X = 0: No more misc fields R: reserved P = 1: Power down supp.	Miscellaneous features field TPCE_MI

4.4. Card Information Structure (CIS)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
										RO = 0: Not read only mode A = 0: Audio not supported T = 0: Single drive	
9Ah	1Bh	CISTPL__TABLE_ENTRY								Configuration table entry tuple	Tuple code
9Ch	06h	TPL_LINK								Link length is 6 bytes	Link to next tuple
9Eh	01h	I	D	Configuration index						Contiguous I/O mapped ATA registers configuration I = 0: No Interface byte D = 0: No Default entry Configuration index = 1	Configuration table index Byte TPCE_INDX
A0h	01h	M	MS	IR	IO	T	P			M = 0: No Misc info MS = 00: No Memory space info IR = 0: No interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: VCC only info	Feature selection byte TPCE_FS
A2h	21h	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for VCC
A4h	B5h	X	Mantissa			Exponent				Nominal voltage = 3.0 V	VCC nominal value
A6h	1Eh	X	Mantissa			Exponent				+0.3 V	Extension byte
A8h	4Dh	X	Mantissa			Exponent				Max average current over 10msec is 45 mA	Max. average current
AAh	1Bh	CISTPL_TABLE_ENTRY								Configuration table entry Tuple	Extension Byte
ACh	12h	TPL_LINK								Link length is 18 bytes	Link to next tuple
AEh	C2h	I	D	Configuration INDEX						ATA primary I/O mapped configuration I = 1: Interface byte follows D = 1: default entry follows Configuration index = 2	Configuration table index byte TPCE_INDX
B0h	41h	W	R	P	B	Interface type				W = 0: Wait not used R = 1: Ready active P = 0: WP not used B = 0: BVS1 and BVD2 not used IF type = 1: I/O interface	Interface description field TPCE_IF

4.4. Card Information Structure (CIS)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
B2h	99h	M	MS	IR	IO		T		P	M = 1: misc info present MS = 00: No memory space info IR = 1: Interrupt info present IO = 1: I/O port info present T = 0: No timing info present P = 1: VCC only info	Feature selection byte TPCE_FS
B4h	27h	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down Curr. info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for VCC
B6h	55h	X		Mantissa			Exponent			Nominal voltage = 5 V	VCC nominal value
B8h	4Dh	X		Mantissa			Exponent			VCC nominal 4.5V	VCC min value
BAh	5Dh	X		Mantissa			Exponent			VCC nominal 5.5V	VCC max value
BCh	75h	X		Mantissa			Exponent			Max average current over10msec is 80mA	Max average current
BEh	EAh	R	S	E	IO		AddrLine			R = 1: Range follows S = 1: 16-bit hosts supported E = 1: 8-bit hosts supported IO AddrLines: 10 lines decoded	I/O space description field TPCE_IO
C0h	61h	LS		AS			N range			LS = 1: Size of lengths is 1 byte AS = 2: Size of address is 2 bytes N Range = 1: Address Range-1	I/O range format description
C2h	F0h	1st I/0 base address								1st I/O base address (LSB)	1st I/O range address
C4h	01h	1st I/0 base address								1st I/O base address (MSB)	
C6h	07h	1st I/0 base address								1st I/O length - 1	1st I/O range length
C8h	F6h	2nd I/O base address								2nd I/O base address (LSB)	2nd I/O range address
CAh	03h	2nd I/O base address								2nd I/O base address(MSB)	
CCh	01h	2nd I/O range length								2nd I/O length – 1	2nd I/O range length

4.4. Card Information Structure (CIS)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
CEh	EEh	S	P	L	M	IRQ		level		S = 1: Share logic active P = 1: Pulse mode IRQ supported L = 1: Level mode IRQ supported M = 0: Bit mask of IRQs present IRQ level is IRQ14	Interrupt request description structure TPCE_IR
D0h	21h	X	R	P	RO	A		T		X = 0: No more misc fields R: reserved P = 1: Power down supp. RO = 0: Not read only mode A = 0: Audio not supported T = 0: Single drive	Miscellaneous features field TPCE_MI
D2h	1Bh	CISTPL_TABLE_ENTRY								Configuration table entry Tuple	Tuple code
D4h	06h	TPL_LINK								Link length is 6 bytes	Link to next tuple
D6h	02h	I	D	Configuration index						ATA primary I/O mapped configuration I = 0: No Interface byte D = 0: No Default entry Configuration index = 2	Configuration table index Byte TPCE_INDX
D8h	01h	I	D	Configuration index						Contiguous I/O mapped ATA registers configuration I = 0: No Interface byte D = 0: No Default entry Configuration index = 1	Configuration table index Byte TPCE_INDX
DAh	21h	M	MS	IR	IO	T		P		M = 0: No Misc info MS = 00: No Memory space info IR = 0: No interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: VCC only info	Feature selection byte TPCE_FS

4.4. Card Information Structure (CIS)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
DCh	B5h	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for VCC
DEh	1Eh	X	Mantissa			Exponent				Nominal voltage = 3.0 V	VCC nominal value
E0h	4Dh	Extension								+0.3 V	Extension byte
E2h	1Bh	CISTPL_TABLE_ENTRY								Config. table entry Tuple	Tuple code
E4h	12h	TPL_LINK								Link length is 18 bytes	Link to next tuple
E6h	C3h	M	MS	IR	IO	T	P			M = 0: No Misc info MS = 00: No Memory space info IR = 0: No interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: VCC only info	Feature selection byte TPCE_FS
E8h	41h	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for VCC
EAh	99h	M	MS	IR	IO	T	P			M = 1: No Misc info MS = 00: No Memory space info IR = 1: No interrupt info present IO = 1: No I/O port info present T = 0: No timing info present P = 01: VCC only info	Feature selection byte TPCE_FS

4.4. Card Information Structure (CIS)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
ECh	27h	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down Curr. info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for VCC
EEh	55h	X	Mantissa			Exponent				Nominal voltage = 5 V	VCC nominal value
F0h	4Dh	X	Mantissa			Exponent				VCC nominal 4.5V	VCC min value
F2h	5Dh	X	Mantissa			Exponent				VCC nominal 5.5V	VCC max value
F4h	75h	X	Mantissa			Exponent				Max average current over10msec is 80mA	Max average current
F6h	EAh	R	S	E	IO	AddrLine				R = 1: Range follows S = 1: 16-bit hosts supported E = 1: 8-bit hosts supported IO AddrLines: 10 lines Decoded	I/O space description field TPCE_IO
F8h	61h	LS	AS			N range				LS = 1: Size of lengths is 1 Byte AS = 2: Size of address is 2 bytes N Range = 1: Address range - 1	I/O range format description
FAh	70h									1st I/O base address (LSB)	1st I/O range address
FCh	01h									1st I/O base address (MSB)	
FEh	07h									1st I/O length - 1	1st I/O range length
100h	76h									2nd I/O base address (LSB)	2nd I/O range address
102h	03h									2nd I/O base address (MSB)	
104h	01h									2nd I/O length	2st I/O range length
106h	EEh	S	P	L	M	IRQ	level			S = 1: Share logic active P = 1: Pulse mode IRQ supported L = 1: Level mode IRQ supported M = 0: Bit mask of IRQs present IRQ level is IRQ14	Interrupt request description structure TPCE_IR Miscellaneous features field TPCE_MI

4.4. Card Information Structure (CIS)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
108h	21h	X	R	P	RO	A		T		X = 0: No more misc fields R: reserved P = 1: Power down supported RO = 0: Not read only mode A = 0: Audio not supported T = 0: Single drive	
10Ah	1Bh	CISTPL_TABLE_ENTRY								Configuration table entry Tuple	Tuple code
10Ch	06h	TPL_LINK								Link length is 6 bytes	Link to next tuple
10Eh	03h	I	D	Configuration index						ATA primary I/O mapped configuration I = 0: No Interface byte D = 0: No Default entry Configuration index = 2	Configuration table index Byte TPCE_INDX
110h	01h	M	MS		IR	IO	T		P	M = 0: No Misc info MS = 00: No Memory space info IR = 0: No interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: VCC only info	Feature selection byte TPCE_FS
112h	21h	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for VCC
114h	B5h	X	Mantissa			Exponent				Nominal voltage = 3.0 V	VCC nominal value
116h	1Eh	Extension								+0.3 V	Extension byte
118h	4Dh	X	Mantissa			Exponent				Max average current over 10msec is 45 mA	Max. average current
11Ah	1Bh	CISTPL_MANFID								Manufacturer's ID code	Tuple Code
11Ch	04h	TPL_LINK								Link length is 4 bytes	Link to next tuple
11Eh	07h	I	D	Configuration Index						AT Fixed Disk Secondary I/O 3.3V configuration	TPCE_INDX
120h	00h	M	MS		IR	IO	T		P	P: Power info type	TPCL_FS
122h	28h									Manufacturer code for SiliconDrive CF	Reserved

4.4. Card Information Structure (CIS)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
124h	D3h									Manufacturer code for SiliconDrive CF	Reserved
126h	14h	CISTPL_NO_LINK								No link control tuple	Tuple code
128h	00h									Link is 0 bytes	Link to next tuple
12Ah	15h	CISTPL_VERS_1								Level 1 version	Tuple code
12Ch	1Ah	TPL_LINK								Link length is 26h bytes	Link to Next Tuple
12Eh	04h	TPPLV1_MAJOR								PC Card 2.0/JEIDA4.1	END marker
130h	01h	TPPLV1_MINOR								PC Card 2.0/JEIDA4.1	Tuple code
132h	53h									S	Info String
134h	49h									I	
136h	4Ch									L	
138h	49h									I	
13Ah	43h									C	
13Ch	4Fh									O	
13Eh	4Eh									N	
140h	53h									S	
142h	59h									Y	
144h	53h									S	
146h	54h									T	
148h	45h									E	
14Ah	4Dh									M	
14Ch	53h									S	
14Eh	00h									“Space”	
150h	56h									V	
152h	45h									E	
154h	52h									R	
156h	32h									2	
158h	2Eh									.	
15Ah	30h									0	
15Ch	30h									0	
15Eh	00h										
160h	FFh										

4.5. Configuration Option Register (200h)

The Configuration Option Register is used to configure the SiliconDrive PC, define the address decoding, and initiate the software RESET sequence.

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	SRESET	LevIREQ	Configuration Index					
Default Value	0	0	0	0	0	0	0	0

Notes

SRESET: When set this bit initiates a software reset sequence, which is equivalent to a Power-On Reset or Hardware Reset.

LevlREQ: IREQ# interrupt signal level mode select:
Logic '0' = Pulse mode, logic '1' = Level mode.

Configuration Index: Memory Mapped Mode 000000B
Independent I/O Mode 000001B
Primary Mode 000010B
Secondary Mode 000011B

4.6. Configuration & Status Register (202h)

The Configuration and Status Register (CSR) informs the host of any status changes with regard to power-down.

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read	Changed	SigChg	IOis8	0	0	PwrDn	Int	0
Write	0	SigChg	IOis8	0	0	PwrDn	0	0
Default Value	0	0	0	0	0	0	0	0

Notes

Changed: Indicates that either CREADY (D5) or CWPort (D4) of the Pin Replacement Register is set. Additionally, this bit changes state as the Power Down (D2) bit changes.

SigChg: Outputs the inverse state of the Changed bit to the hardware interface signal STSCHG# at the card interface.

IOis8: Informs the host of the valid data bus width for the operations in progress, “0” indicates a 16-bit data transfer, “1” indicates an 8-bit data transfer.

PwrDwn: Indicates the state of the card: Operating – “0”, or Power Down mode “1”. During power-down mode, no commands are accepted. Additionally, the host may not initiate a Power-Down request when the card is BUSY via the Status Register or the Hardware RDY/BSY pin.

Int: Indicates the inverse of the IREQ# status signal.

4.7. Pin Placement Register (204h)

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	CBVD1	CBVD2	CRDY	CWProt	RBVD1	RBVD2	RRDY	RWProt
Default Value	0	0	0	0	1	1	0	0

Notes

CRDY: Indicates a bit change in the RRDY (D1) bit.

CWProt Indicates a bit change in the RWProt (D0) bit.

RRDY: When set high “1” informs the host that the card is ready, low “0” state indicates the card is busy.

RWProt: Indicates Write Protect is enabled when set to “1”, and disabled when “0”.

4.8. Socket & Copy Register (206h)

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	RFU	Copy Number			Socket Number			
Default Value	0	0	0	0	0	0	0	0

Notes

RFU: Reserved for future use.

Copy Number: Indicates the card number. Allows the host to differentiate between identical card by writing to this bit which card is being accessed. This value will be compared to the DRV bit in the ATA Drive/Head Register.

Card 0: 000B = (D6,D5,D4). (Default).
Card 1: 001B = (D6,D5,D4). (Alternate).

Socket Number: The host writes the socket number identifying the inserted card.

5. COMMON MEMORY DESCRIPTION & OPERATION

Common memory space can be accessed when the card is configured in Memory Mapped mode.

5.1. Common Memory Read Operations

Common memory read operations are issued by asserting either CE1# or CE2# or both, and OE# low. REG# and WE# must be inactive.

Function Mode	REG#	CE1#	CE2#	A0	OE#	WE#	D[15:8]	D[7:0]
Standby	H	H	H	X	X	X	High-Z	High-Z
Byte Access	H	L	H	L	L	H	High-Z	Even
	H	H	L	H	L	H	High-Z	Odd
Word Access	H	L	L	X	L	H	Odd	Even
Odd Byte OnlyAccess	H	L	H	X	H	H	Odd	High-Z

5.2. Common Memory Write Operations

Common memory write operations are issued by asserting either CE1# or CE2# or both, and WE# low. REG# and OE# must be inactive.

Function Mode	REG#	CE1#	CE2#	A0	OE#	WE#	D[15:8]	D[7:0]
Standby	H	H	H	X	X	X	High-Z	High-Z
Byte Access	H	L	H	L	H	L	High-Z	Even
	H	H	L	H	H	L	High-Z	Odd
Word Access	H	L	L	X	H	L	Odd	Even
Odd Byte Only Access	H	L	H	X	H	H	Odd	High-Z

6. I/O SPACE DESCRIPTION & OPERATION

6.1. I/O Space Read Operations

Function Mode	REG#	CE1#	CE2#	A0	IOR#	IOW#	D[15:8]	D[7:0]
Standby	X	H	H	X	X	X	High-Z	High-Z
Byte Access	L	L	H	L	L	H	High-Z	Even
	L	L	H	H	L	H	High-Z	Odd
Word Access	L	L	L	L	L	H	Odd	Even
I/O Inhibit	H	X	X	X	L	H	High-Z	High-Z
Odd Byte Only Access	L	H	L	X	L	H	Odd	High-Z

6.2. I/O Space Write Operations

Function Mode	REG#	CE1#	CE2#	A0	IORD#	IOWR#	D[15:8]	D[7:0]
Standby	X	H	H	X	X	X	X	X
Byte Access	L	L	H	L	H	L	X	Even
	L	L	H	H	H	L	X	Odd
Word Access	L	L	L	L	H	L	Odd	Even
I/O Inhibit	H	X	X	X	H	L	X	X
Odd Byte Only Access	L	H	L	X	H	L	Odd	X