

## SiliconDrive™ PC Card: 128MB to 8GB of Solid-State Storage

### Overview

SiliconDrive™ PC Card products replace the functionality of rotating hard disk drives while providing enhanced levels of performance and reliability for Enterprise System OEMs targeting the netcom, military, industrial, interactive kiosk and medical markets. Typical end-market applications include broadband data and voice networks, military systems, flight system avionics, medical equipment, industrial control systems, and interactive kiosks.

SiliconDrives are designed to meet the growing OEM demands for high performance, high reliability, multi-year product lifecycles, low power consumption, compact size, and reliable operation in extreme environments. SiliconDrive PC Card Type II form factor products are available in capacities ranging from 128MB to 8GB.

SiliconSystems patented PowerArmor™ technology provides enhanced levels of drive integrity in the event of unexpected power disturbances and is integrated as a standard feature on all SiliconDrives. In addition, patent-pending technology advances of data sanitization and purge, write protection, and application-specific performance enhancements are available as options on all SiliconDrive products. Separate application notes covering these topics are available under NDA.



### Features

- ATA-3 Compliant
- Capacity Range: 128MB to 8GB
- Supports Both 8 and 16 Bit Data Register Transfers
- Supports Dual Voltage 3.3V or 5V Interface
- Less than 1 Error in  $10^{14}$  Bits Read
- MTBF > 4,000,000 Hours
- Industry Standard Type II PC Card Form Factor
- Solid-State, No Moving Parts
- Supports PIO Modes 0-4 and DMA Modes 0-2
- High Shock & Vibration Tolerance

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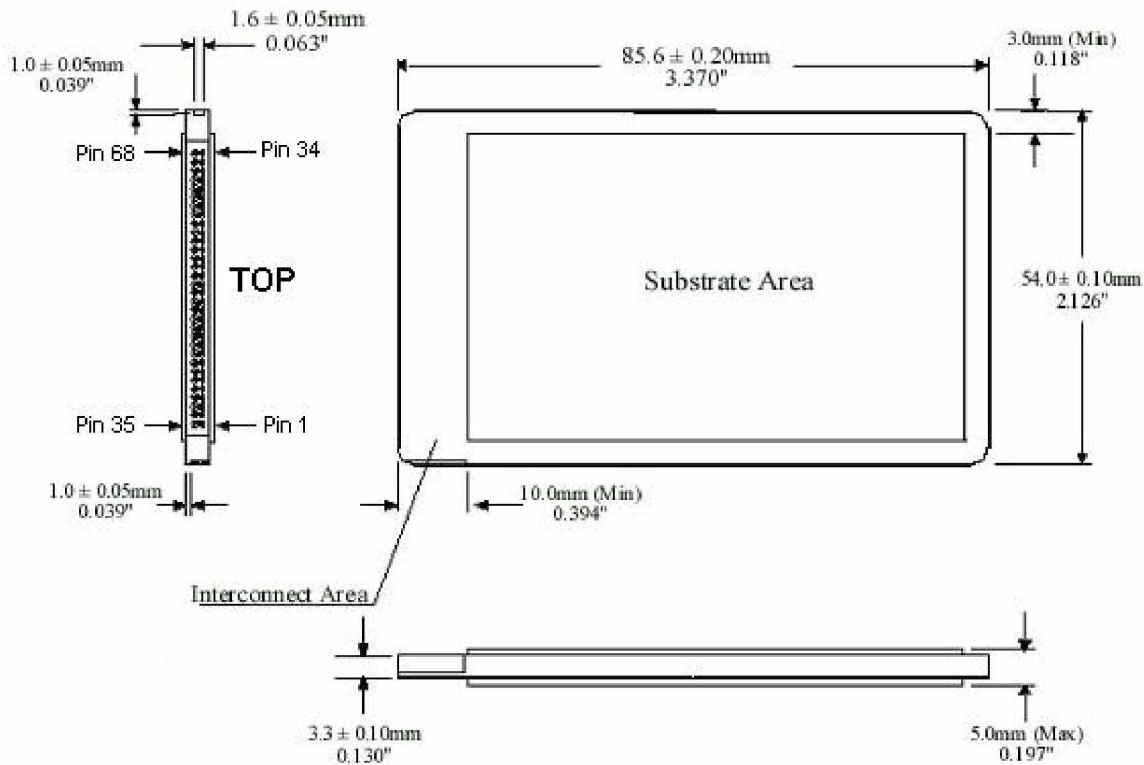
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# 1. PHYSICAL SPECIFICATIONS

SiliconDrive PC Card products are offered in an industry standard PC Card Type II form factor. Refer to Section 10.1 Part Ordering Nomenclature for details regarding PC Card capacities.

## 1.1. Physical Dimensions

The following diagram describes the PC Card Type II physical dimensions and pin orientation:



## 2. PRODUCT SPECIFICATIONS<sup>1</sup>

### 2.1. System Performance

|   |             |
|---|-------------|
| Reset to Ready Startup Time (Typical/Max) | 200ms/400ms |
| Read Transfer Rate (Typical)              | 8MB/s       |
| Write Transfer Rate (Typical)             | 6MB/s       |
| Burst Transfer Rate                       | 16.7MB/s    |
| Controller Overhead (Command to DRQ)      | 2ms (max)   |

### 2.2. System Power Requirements

|                         |           |            |
|-------------------------|-----------|------------|
| DC Input Voltage        | 3.3 ± 10% | 5.0 ± 10%  |
| Sleep (Standby Current) | <0.5mA    | <1.0mA     |
| Read (Typical/Peak)     | 20mA/75mA | 30mA/100mA |
| Write (Typical/Peak)    | 30mA/75mA | 40mA/100mA |

### 2.3. System Reliability

|                  |   |
|------------------|---|
| MTBF (@ 25°C)    | > 4,000,000 Hours                                       |
| Data Reliability | < 1 Non-Recoverable Error in 10 <sup>14</sup> Bits Read |
| Endurance        | >2,000,000 write/erase cycles                           |

<sup>1</sup> All SiliconDrive PC Card values quoted are typical at 25°C and nominal supply voltage.

**2.4. Product Capacity Specifications**

| Product Density | Formatted Capacity (Bytes) | Number of Sectors | Number of Cylinders | Number of Heads | Number of Sectors/Track |
|-----------------|----------------------------|-------------------|---------------------|-----------------|-------------------------|
| 128MB           | 130,154,496                | 254,208           | 993                 | 8               | 32                      |
| 256MB           | 260,571,136                | 508,928           | 994                 | 16              | 32                      |
| 512 MB          | 521,773,056                | 1,019,088         | 1011                | 16              | 63                      |
| 1GB             | 1,047,674,880              | 2,046,240         | 2030                | 16              | 63                      |
| 2GB             | 2,098,446,336              | 4,098,528         | 4066                | 16              | 63                      |
| 4GB             | 4,224,761,856              | 8,251,488         | 8186                | 16              | 63                      |
| 6GB             | 6,309,789,696              | 12,323,808        | 12226               | 16              | 63                      |
| 8GB             | 8,456,749,056              | 16,517,088        | 16386               | 16              | 63                      |

**2.5. Environmental Specifications**

|                    |   |
|--------------------|---|
| <b>Temperature</b> | 0°C to 70°C (Standard)  |
|                    | -40°C to 85°C (Industrial)  |
| <b>Humidity</b>    | 8% to 95% non-condensing  |
| <b>Vibration</b>   | 16.3gRMS, MIL-STD-810F, Method 514.5, Procedure I, Category 24                      |
| <b>Shock</b>       | 1000G, Half-sine, 0.5ms Duration<br>50g Pk, MIL-STD-810F, Method 516.5, Procedure I |
| <b>Altitude</b>    | 80,000ft, MIL-STD-810F, Method 500.4, Procedure II                                  |

### 3. ELECTRICAL SPECIFICATIONS

#### 3.1. Pin Assignments

The following Table describes the SiliconDrive PC Card 68-Pin Connector Signals:

| Pin | PC Card Memory Mode | PC Card I/O Mode | IDE-ATA Mode     | Pin | PC Card Memory Mode | PC Card I/O Mode   | IDE-ATA Mode     |
|-----|---------------------|------------------|------------------|-----|---------------------|--------------------|------------------|
| 1   | GND                 | GND              | GND              | 35  | GND                 | GND                | GND              |
| 2   | D3                  | D3               | D3               | 36  | CD1#                | CD1#               | CD1#             |
| 3   | D4                  | D4               | D4               | 37  | D11                 | D11                | D11 <sup>1</sup> |
| 4   | D5                  | D5               | D5               | 38  | D12                 | D12                | D12 <sup>1</sup> |
| 5   | D6                  | D6               | D6               | 39  | D13                 | D13                | D13 <sup>1</sup> |
| 6   | D7                  | D7               | D7               | 40  | D14                 | D14                | D14 <sup>1</sup> |
| 7   | CE1#                | CE1#             | CS0#             | 41  | D15                 | D15                | D15 <sup>1</sup> |
| 8   | A10                 | A10              | A10 <sup>2</sup> | 42  | CE2#                | CE2#               | CS1#             |
| 9   | OE#                 | OE#              | OE# <sup>2</sup> | 43  | VS1#                | VS1#               | VS1#             |
| 10  | N.U.                | N.U.             | N.U.             | 44  | IORD#               | IORD#              | IORD#            |
| 11  | A9                  | A9               | A9 <sup>2</sup>  | 45  | IOWR#               | IOWR#              | IOWR#            |
| 12  | A8                  | A8               | A8 <sup>2</sup>  | 46  | N.U.                | N.U.               | N.U.             |
| 13  | N.U.                | N.U.             | N.U.             | 47  | N.U.                | N.U.               | N.U.             |
| 14  | N.U.                | N.U.             | N.U.             | 48  | N.U.                | N.U.               | N.U.             |
| 15  | WE#                 | WE#              | WE# <sup>3</sup> | 49  | N.U.                | N.U.               | N.U.             |
| 16  | RDY/BSY#            | IREQ             | INTRQ            | 50  | N.U.                | N.U.               | N.U.             |
| 17  | Vcc                 | Vcc              | Vcc              | 51  | Vcc                 | Vcc                | Vcc              |
| 18  | N.U.                | N.U.             | N.U.             | 52  | N.U.                | N.U.               | N.U.             |
| 19  | N.U.                | N.U.             | N.U.             | 53  | N.U.                | N.U.               | N.U.             |
| 20  | N.U.                | N.U.             | N.U.             | 54  | N.U.                | N.U.               | N.U.             |
| 21  | N.U.                | N.U.             | N.U.             | 55  | N.U.                | N.U.               | N.U.             |
| 22  | A7                  | A7               | A7 <sup>2</sup>  | 56  | N.U.                | N.U.               | CSEL#            |
| 23  | A6                  | A6               | A6 <sup>2</sup>  | 57  | VS2#                | VS2#               | VS2#             |
| 24  | A5                  | A5               | A5 <sup>2</sup>  | 58  | RESET               | RESET              | RESET#           |
| 25  | A4                  | A4               | A4 <sup>2</sup>  | 59  | WAIT#               | WAIT#              | IORDY            |
| 26  | A3                  | A3               | A3 <sup>2</sup>  | 60  | INPACK#             | INPACK#            | DMARQ            |
| 27  | A2                  | A2               | A2               | 61  | REG#                | REG#               | DMACK#           |
| 28  | A1                  | A1               | A1               | 62  | BVD2 <sup>3</sup>   | SPKR# <sup>3</sup> | DASP#            |
| 29  | A0                  | A0               | A0               | 63  | BVD1                | STSCHG#            | PDIAG#           |
| 30  | D0                  | D0               | D0               | 64  | D8                  | D8                 | D8 <sup>1</sup>  |
| 31  | D1                  | D1               | D1               | 65  | D9                  | D9                 | D9 <sup>1</sup>  |
| 32  | D2                  | D2               | D2               | 66  | D10                 | D10                | D10 <sup>1</sup> |
| 33  | WP                  | IOIS16#          | IOCS16#          | 67  | CD2#                | CD2#               | CD2#             |
| 34  | GND                 | GND              | GND              | 68  | GND                 | GND                | GND              |

N.U. = Not Used.

#### Notes

1. These signals are required only for 16-bit access and not required when installed in 8-bit systems.
2. Should be grounded by the host.

## 3.2. Signal Descriptions

| 3.2. Signal Descriptions            |   |      |   |
|-------------------------------------|---|------|---|
| Signal Name                         | Pin                                     | Type | Description   |
| A10 - A0                            | 8,11,12,22,<br>23,24,25,26,<br>27,28,29 | I    | These address lines along with the -REG signal are used to select the following: The I/O port address registers within the PC Card, the memory mapped port address registers within the PC Card, a byte in the card's information structure and its configuration control and status registers. |
| A10 - A0<br>(PC Card I/O Mode)      |   |      | This signal is the same as the PC Card Memory Mode signal.  |
| A2 - A0<br>(True IDE Mode)          | 27,28,29                                |      | In True IDE Mode only A[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.  |
| BVD1<br>(PC Card Memory Mode)       | 63                                      | I/O  | This signal is asserted high, as BVD1 is not supported.   |
| -STSCHG<br>(PC Card I/O Mode)       |   |      | This signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Configuration and Status Register.  |
| -PDIAG<br>(True IDE Mode)           |   |      | In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.   |
| BVD2<br>(PC Card Memory Mode)       | 62                                      | I/O  | This signal is asserted high, as BVD2 is not supported.   |
| -SPKR<br>(PC Card I/O Mode)         |   |      | This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated.   |
| -DASP<br>(True IDE Mode)            |   |      | In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.   |
| -CD1, -CD2<br>(PC Card Memory Mode) | 36,37                                   | O    | These Card Detect pins are connected to ground on the PC Card. They are used by the host to determine that the PC Card is fully inserted into its socket.   |
| -CD1, -CD2<br>(PC Card I/O Mode)    |   |      | This signal is the same for all modes.  |
| -CD1, -CD2<br>(True IDE Mode)       |   |      | This signal is the same for all modes.  |

### 3.2. Signal Descriptions

| Signal Name                         | Pin  | Type | Description  |
|-------------------------------------|--|------|--|
| -CE1, -CE2<br>(PC Card Memory Mode) | 7,42   | I    | The Card Enable signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7. See Sections 4, 5, and 6. |
| -CE1, -CE2<br>(PC Card I/O Mode)    |  |      | This signal is the same as the PC Card Memory Mode signal.   |
| -CS0, -CS1<br>(True IDE Mode)       |  |      | In the True IDE Mode CS0 is the chip select for the task file registers while CS2 is used to select the Alternate Status Register and the Device Control Register.   |
| -CSEL<br>(PC Card Memory Mode)      | 56   | I    | This signal is not used for this mode.   |
| -CSEL<br>(PC Card I/O Mode)         |  |      | This signal is not used for this mode.   |
| -CSEL<br>(True IDE Mode)            |  |      | Cable Select is an internally pulled up signal used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.  |
| D15 - D00<br>(PC Card Memory Mode)  | 41,40,39,38,<br>37,66,65,64,<br>6,5,4,3,2,<br>32, 31, 30 | I/O  | These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.  |
| D15 - D00<br>(PC Card I/O Mode)     |  |      | This signal is the same as the PC Card Memory Mode signal.   |
| D15 - D00<br>(True IDE Mode)        |  |      | In True IDE Mode, all Task File operations occur in byte mode on the low order bus D00-D07 while all data transfers are 16 bit using D00-D15.  |
| GND<br>(PC Card Memory Mode)        | 1,34,35,68   | ---  | Ground.  |
| GND<br>(PC Card I/O Mode)           |  |      | This signal is the same for all modes.   |
| GND<br>(True IDE Mode)              |  |      | This signal is the same for all modes.   |

## 3.2. Signal Descriptions

| Signal Name                      | Pin | Type | Description  |
|----------------------------------|-----|------|--|
| -INPACK<br>(PC Card Memory Mode) | 60  | O    | This signal is not used in this mode.  |
| -INPACK<br>(PC Card I/O Mode)    |     |      | The Input Acknowledge signal is asserted by the PC Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the PC Card and the CPU.  |
| DMARQ<br>(True IDE Mode)         |     |      | In True IDE Mode this signal is used for DMA transfers between the host and device. DMARQ shall be asserted by the device when the device is ready to transfer data to/from the host. The direction of data transfer is controlled by -IORD and -IOWR. This signal is used in a handshake manner with -DMACK, i.e. the device shall wait until the host asserts -DMACK before negating DMARQ, and re-assert DMARQ if there is more data to transfer. The DMARQ/-DMACK handshake is used to provide flow control during the transfer. |
| -IORD<br>(PC Card Memory Mode)   | 44  | I    | This signal is not used in this mode.  |
| -IORD<br>(PC Card I/O Mode)      |     |      | This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the PC Card when the card is configured to use the I/O interface.   |
| -IORD<br>(True IDE Mode)         |     |      | In True IDE Mode, this signal has the same function as in PC Card I/O Mode.  |
| -IOWR<br>(PC Card Memory Mode)   | 45  | I    | This signal is not used in this mode.  |
| -IOWR<br>(PC Card I/O Mode)      |     |      | The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the PC Card controller registers when the PC Card is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge).   |
| -IOWR<br>(True IDE Mode)         |     |      | In True IDE Mode, this signal has the same function as in PC Card I/O Mode.  |
| -OE<br>(PC Card Memory Mode)     | 9   | I    | This is an Output Enable strobe generated by the host interface. It is used to read data from the PC Card in Memory Mode and to read the CIS and configuration registers.  |
| -OE<br>(PC Card I/O Mode)        |     |      | In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.  |
| -ATA SEL<br>(True IDE Mode)      |     |      | To enable True IDE Mode this input should be grounded by the host.   |

### 3.2. Signal Descriptions

| Signal Name                        | Pin | Type | Description  |
|------------------------------------|-----|------|--|
| -RDY/-BSY<br>(PC Card Memory Mode) | 16  | O    | In Memory Mode this signal is set high when the PC Card is ready to accept a new data transfer operation and held low when the card is busy. The Host memory card socket must provide a pull-up resistor.  |
| -IREQ<br>(PC Card I/O Mode)        |     |      | At power up and at Reset, the RDY/-BSY signal is held low (busy) until the PC Card has completed its power up or reset function. No access of any type should be made to the PC Card during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true: The PC Card has been powered up with --RESET continuously disconnected or asserted. |
| -IREQ<br>(True IDE Mode)           |     |      | I/O Operation – After the PC Card has been configured for I/O operation, this signal is used as the Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.   |
| -REG<br>(PC Card Memory Mode)      | 61  | I    | In True IDE Mode signal is the active high Interrupt Request to the host.  |
| -REG<br>(PC Card I/O Mode)         |     |      | This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.  |
| -DMACK<br>(True IDE Mode)          |     |      | The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.   |
| -RESET<br>(PC Card Memory Mode)    | 58  | I    | In True IDE Mode this signal is used by the host in response to DMARQ to initiate DMA transfers. The DMARQ/-DMACK handshake is used to provide flow control during the transfer. When –DMACK is asserted, -CS0 and –CS1 shall not be asserted and transfers shall be 16-bits wide.   |
| -RESET<br>(PC Card I/O Mode)       |     |      | When the pin is high, this signal Resets the PC Card. The PC Card is Reset only at power up if this pin is left high or open from power-up. The PC Card is also Reset when the Soft Reset bit in the Card Configuration  |
| -RESET                             |     |      | Option Register is set.  |
|                                    |     |      | This signal is the same as the PC Card Memory Mode signal.   |

### 3.2. Signal Descriptions

| Signal Name  | Pin   | Type | Description  |
|--|-------|------|--|
| (True IDE Mode)  |       |      | In the True IDE Mode this input pin is the active low hardware reset from the host.  |
| VCC<br>(PC Card Memory Mode)<br><br>VCC<br>(PC Card I/O Mode)<br><br>VCC<br>(True IDE Mode)        | 17,51 | -    | +5 V, +3.3 V power.<br><br>This signal is the same for all modes.<br><br>This signal is the same for all modes.  |
| -VS1, -VS2<br><br>-VS1, -VS2<br>(PC Card I/O Mode)<br><br>-VS1, -VS2<br>(True IDE Mode)            | 43,57 | O    | Voltage Sense Signals. -VS1 is grounded so that the PC Card CIS can be read at 3.3 volts and -VS2 is reserved by PC Card for a secondary voltage.<br><br>This signal is the same for all modes.<br><br>This signal is the same for all modes.  |
| -WAIT<br>(PC Card Memory Mode)<br><br>-WAIT<br>(PC Card I/O Mode)<br><br>-IORDY<br>(True IDE Mode) | 59    | O    | The -WAIT signal is driven low by the PC Card to signal the host to delay completion of a memory or I/O cycle that is in progress.<br><br>This signal is the same as the PC Card Memory Mode signal.<br><br>In True IDE Mode this output signal may be used as IORDY.  |
| -WE<br>(PC Card Memory Mode)<br><br>-WE<br>(PC Card I/O Mode)<br><br>-WE<br>(True IDE Mode)        | 15    | I    | This is a signal driven by the host and used for strobing memory write data to the registers of the PC Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.<br><br>In PC Card I/O Mode, this signal is used for writing the configuration registers.<br><br>In True IDE Mode this input signal is not used and should be connected to VCC by the host.  |
| WP<br>(PC Card Memory Mode)<br><br>-IOIS16<br>(PC Card I/O Mode)<br><br>-IOIS16<br>(True IDE Mode) | 33    | O    | Write Protect Memory Mode – The PC Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.<br><br>I/O Operation – When the PC Card is configured for I/O Operation, Pin 33 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.<br><br>In True IDE Mode this output signal is asserted low |

### 3.2. Signal Descriptions

| Signal Name | Pin | Type | Description   |
|-------------|-----|------|---|
|             |     |      | when this device is expecting a word data transfer cycle. |

### 3.3. Absolute Maximum Ratings

**Vcc = 3.3 ± 10%**

| Symbol         | Parameter               | Min  | Max | Units |
|----------------|-------------------------|------|-----|-------|
| Ts             | Storage Temperature     | -55  | 125 | °C    |
| T <sub>A</sub> | Operating Temperature   | -40  | 85  | °C    |
| Vcc            | Vcc with Respect to GND | -0.3 | 6.7 | V     |
| Vin            | Input Voltage           | -0.5 | 3.8 | V     |
| Vout           | Output Voltage          | -0.3 | 3.6 | V     |

**Vcc = 5.0 ± 10%**

| Symbol         | Parameter               | Min  | Max | Units |
|----------------|-------------------------|------|-----|-------|
| Ts             | Storage Temperature     | -55  | 125 | °C    |
| T <sub>A</sub> | Operating Temperature   | -40  | 85  | °C    |
| Vcc            | Vcc with Respect to GND | -0.3 | 6.7 | V     |
| Vin            | Input Voltage           | -0.5 | 6.0 | V     |
| Vout           | Output Voltage          | -0.3 | 5.8 | V     |

### 3.4. Capacitance

| Symbol           | Parameter                  | Max | Units |
|------------------|----------------------------|-----|-------|
| Cin              | Input Capacitance          | 35  | pF    |
| Cout             | Output Capacitance         | 35  |       |
| C <sub>I/O</sub> | Bi-directional Capacitance | 35  |       |

### 3.5. DC Characteristics

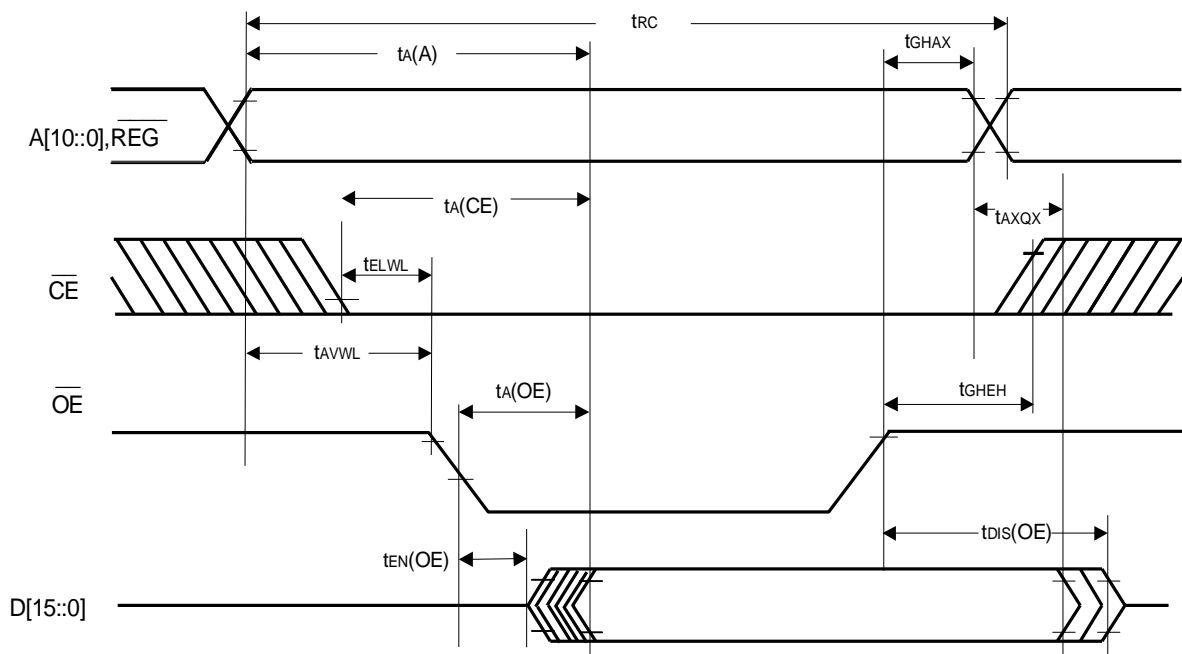
| Symbol           | Parameter                       | 3.3 V $\pm$ 10%       |                      | 5V $\pm$ 10%          |                      | Units   |
|------------------|---------------------------------|-----------------------|----------------------|-----------------------|----------------------|---------|
|                  |                                 | Min.                  | Max.                 | Min.                  | Max.                 |         |
| V <sub>CC</sub>  | Power Supply Voltage            | 3.0                   | 3.6                  | 4.5                   | 5.5                  | V       |
| I <sub>LI</sub>  | Input Leakage<br>*(1) Current   |                       | 5                    |                       | 5                    | $\mu$ A |
| I <sub>LO</sub>  | Output Leakage<br>*(1) Current  |                       | 5                    |                       | 5                    | $\mu$ A |
| V <sub>CCR</sub> | V <sub>CC</sub> Read Current    |                       | 50                   | -                     | 80                   | mA      |
| V <sub>CCW</sub> | V <sub>CC</sub> Write Current   |                       | 50                   | -                     | 80                   | mA      |
| V <sub>CCS</sub> | V <sub>CC</sub> Standby Current |                       | .3                   | -                     | .5                   | mA      |
| V <sub>IL</sub>  | Input LOW Voltage               | -0.3                  | .3 x V <sub>CC</sub> | -0.3                  | .3 x V <sub>CC</sub> | V       |
| V <sub>IH</sub>  | Input HIGH Voltage              | .7 x V <sub>CC</sub>  | V <sub>CC</sub> + .3 | .7 x V <sub>CC</sub>  | V <sub>CC</sub> + .3 | V       |
| V <sub>OL</sub>  | Output LOW Voltage              | -                     | .4                   |                       | .4                   | V       |
| V <sub>OH</sub>  | Output HIGH Voltage             | V <sub>CC</sub> - 0.4 |                      | V <sub>CC</sub> - 0.4 |                      | V       |

**Note**

\*(1) Except pulled up/pulled down pin.

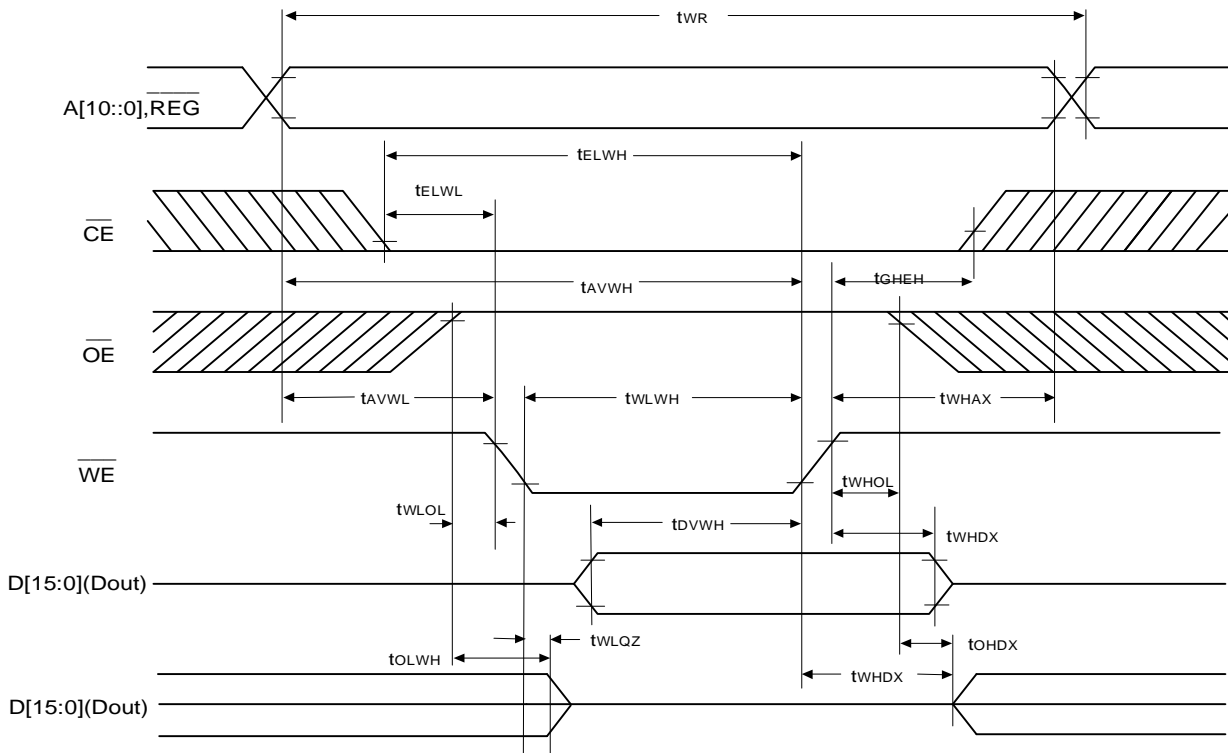
### 3.6. AC Characteristics

#### 3.6.1. Attribute & Common Memory Read Timing



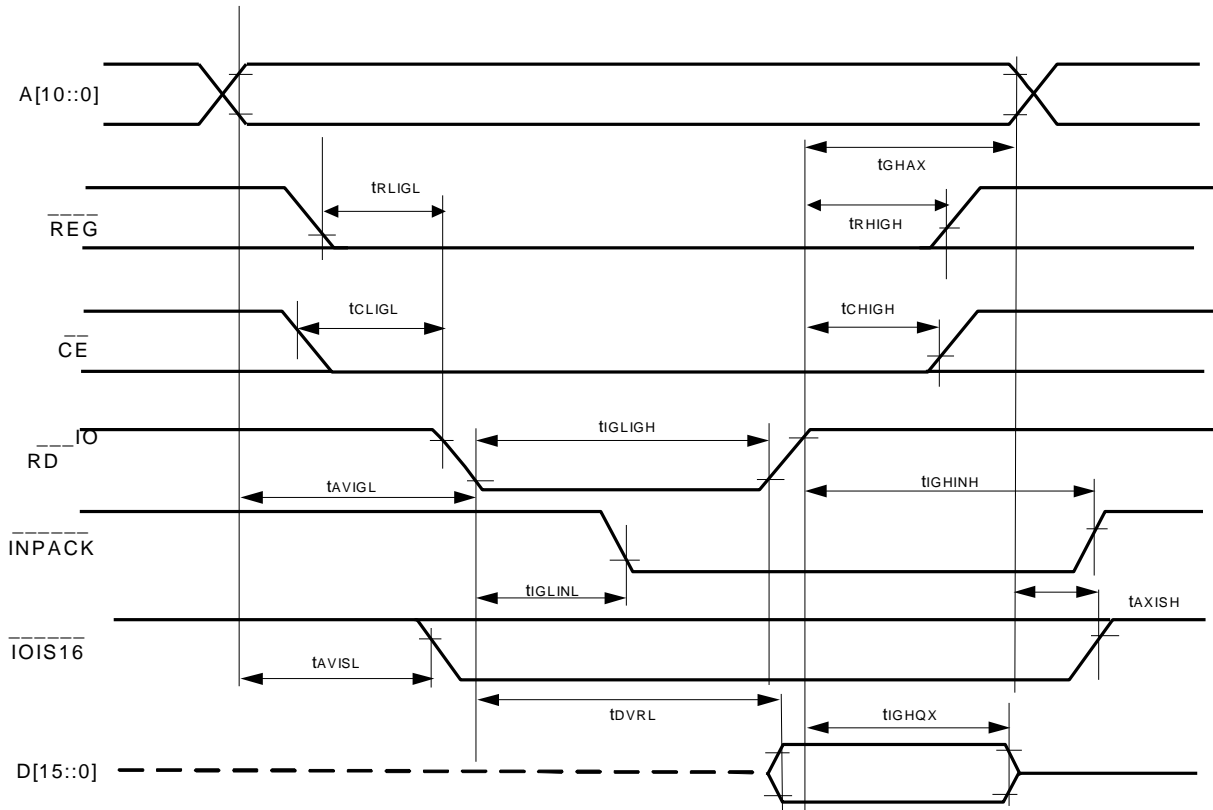
| Symbol               | Parameter                          | Min | Max | Unit |
|----------------------|------------------------------------|-----|-----|------|
| t <sub>RC</sub>      | Read Cycle Time                    | 100 |     | nsec |
| t <sub>A(A)</sub>    | Address Access Time                | -   | 100 |      |
| t <sub>A(CE)</sub>   | Card Enable Access Time            | -   | 100 |      |
| t <sub>A(OE)</sub>   | Output Enable Access Time          | -   | 50  |      |
| t <sub>DIS(OE)</sub> | Output Disable Time from OE        | -   | 50  |      |
| t <sub>EN(OE)</sub>  | Output Enable Time from OE         | 5   | -   |      |
| t <sub>AXQX</sub>    | Data Valid from Address Change     | 0   | -   |      |
| t <sub>AVWL</sub>    | Address Setup Time                 | 10  | -   |      |
| t <sub>AXQX</sub>    | Address Hold Time                  | 15  | -   |      |
| t <sub>ELWL</sub>    | Card Enable Setup Time before OE   | 0   | -   |      |
| t <sub>GHEH</sub>    | Card Enable Hold Time following OE | 15  | -   |      |

### 3.6.2. Attribute & Common Memory Write Timing



| Symbol      | Parameter                        | Min | Max | Unit |
|-------------|----------------------------------|-----|-----|------|
| $t_{WR}$    | Write Cycle Time                 | 100 | -   | nsec |
| $t_{LWHL}$  | Write Pulse Width                | 60  | -   |      |
| $t_{AVWL}$  | Address Setup Time               | 10  | -   |      |
| $t_{AVWH}$  | Address Setup Time for WE        | 70  | -   |      |
| $t_{ELWH}$  | Card Enable Setup Time for WE    | 70  | -   |      |
| $t_{WHDX}$  | Data Hold Time                   | 10  | -   |      |
| $t_{WHAX}$  | Write Recover Time               | 15  | -   |      |
| $t_{LWLOZ}$ | Output Disable Time from WE      | -   | 75  |      |
| $t_{LWLOH}$ | Output Disable Time from OE      | -   | 100 |      |
| $t_{LWHOX}$ | Output Enable Time from WE       | 5   | -   |      |
| $t_{LWHOX}$ | Output Enable Time from OE       | 5   | -   |      |
| $t_{LWLOL}$ | Output Enable Setup for WE       | 10  | -   |      |
| $t_{LWHOL}$ | Output Enable Hold from WE       | 10  | -   |      |
| $t_{ELWL}$  | Card Enable Setup Time before WE | 0   | -   |      |
| $t_{GHEH}$  | Card Enable Hold Time from WE    | 15  | -   |      |
| $t_{DVWH}$  | Data Setup Time                  | 40  | -   |      |

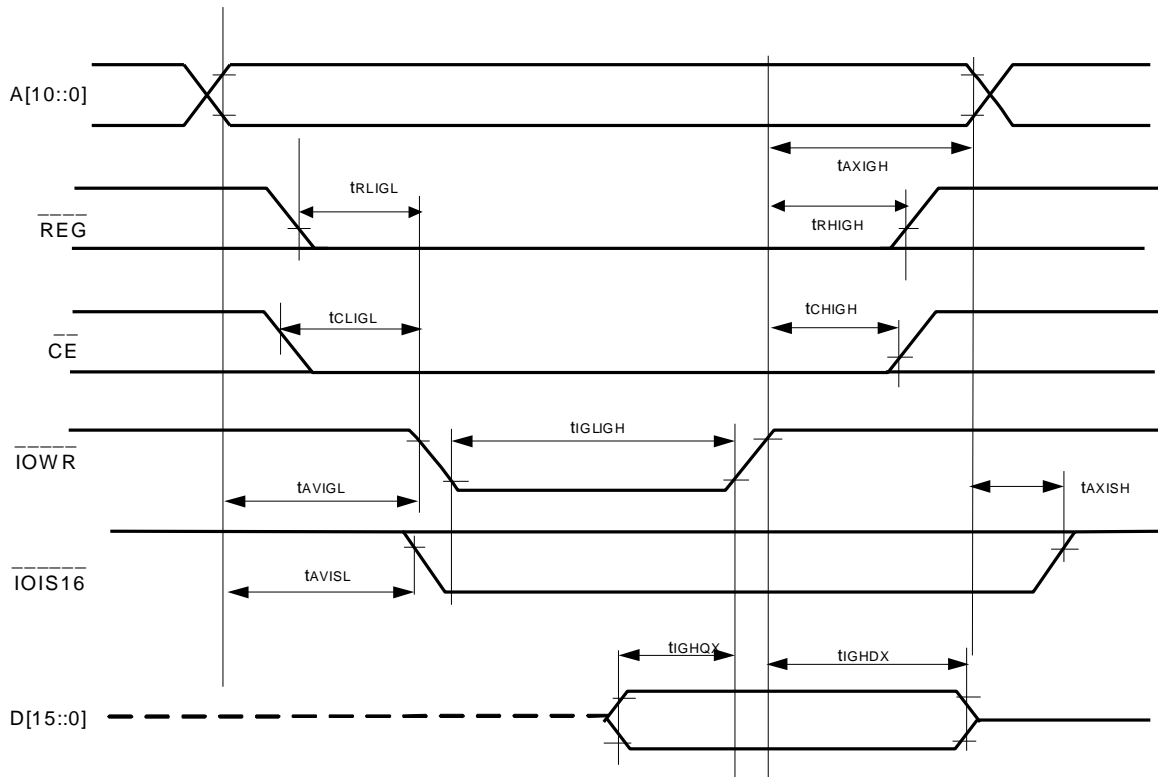
### 3.6.3. I/O Access Read Timing



| Symbol       | Parameter                         | Min | Max | Units |
|--------------|-----------------------------------|-----|-----|-------|
| $t_{DVRL}$   | Data Delay after IORD             | -   | 50  | nsec  |
| $t_{IGHQX}$  | Data Hold following IORD          | 5   | -   |       |
| $t_{IGLIGH}$ | IORD Pulse Width                  | 65  | -   |       |
| $t_{AVIGL}$  | Address Setup before IORD         | 25  | -   |       |
| $t_{GHAX}$   | Address Hold following IORD       | 10  | -   |       |
| $t_{CLIGL}$  | CE Setup before IORD              | 5   | -   |       |
| $t_{CHIGH}$  | CE Hold following IORD            | 10  | -   |       |
| $t_{RLIGL}$  | REG Setup before IORD             | 5   | -   |       |
| $t_{RHIGH}$  | REG Hold following IORD           | 0   | -   |       |
| $t_{IGLINL}$ | INPACK Delay falling from IORD    | -   | (1) |       |
| $t_{IGHINH}$ | INPACK Delay Rising from IORD     | -   | (1) |       |
| $t_{AVISL}$  | IOIS16 Delay Falling from Address | -   | (1) |       |
| $t_{AXISH}$  | IOIS16 Delay Rising from Address  | -   | (1) |       |

Note: 1) IOIS16 and INPACK is not supported.

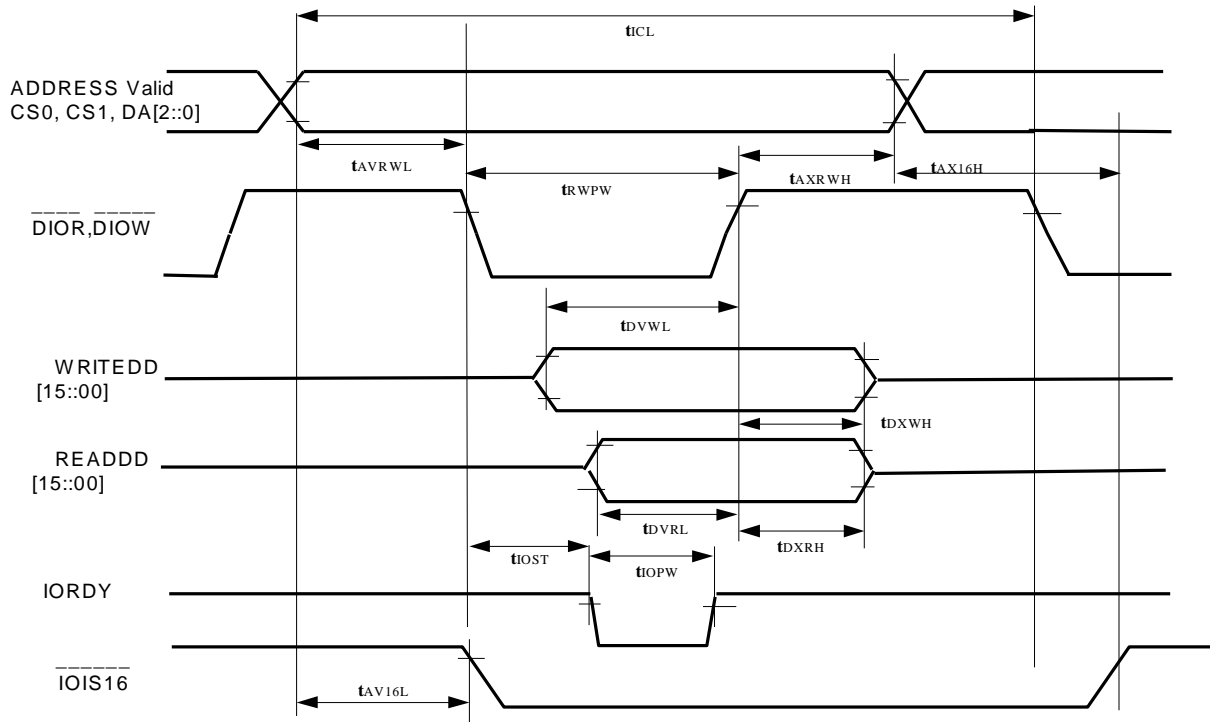
### 3.6.4. I/O Access Write Timing



| Symbol      | Parameter                         | Min | Max | Units |
|-------------|-----------------------------------|-----|-----|-------|
| $t_{GLHDX}$ | Data Hold following IOWR          | 5   | -   | nsec  |
| $t_{GLHGX}$ | Data Setup before IOWR            | 20  | -   |       |
| $t_{GLIGH}$ | IOWR Pulse Width                  | 65  | -   |       |
| $t_{AVIGL}$ | Address Setup before IOWR         | 25  | -   |       |
| $t_{AXIGH}$ | Address Hold following IOWR       | 10  | -   |       |
| $t_{CLIGL}$ | CE Setup before IOWR              | 5   | -   |       |
| $t_{CHIGH}$ | CE Hold following IOWR            | 10  | -   |       |
| $t_{RLIGL}$ | REG Setup before IOWR             | 5   | -   |       |
| $t_{RHIGH}$ | REG Hold following IOWR           | 0   | -   |       |
| $t_{AVISL}$ | IOIS16 Delay Falling from Address | -   | (1) |       |
| $t_{AXISH}$ | IOIS16 Delay Rising from Address  | -   | (1) |       |

Note: 1) IOIS16 and INPACK is not supported.

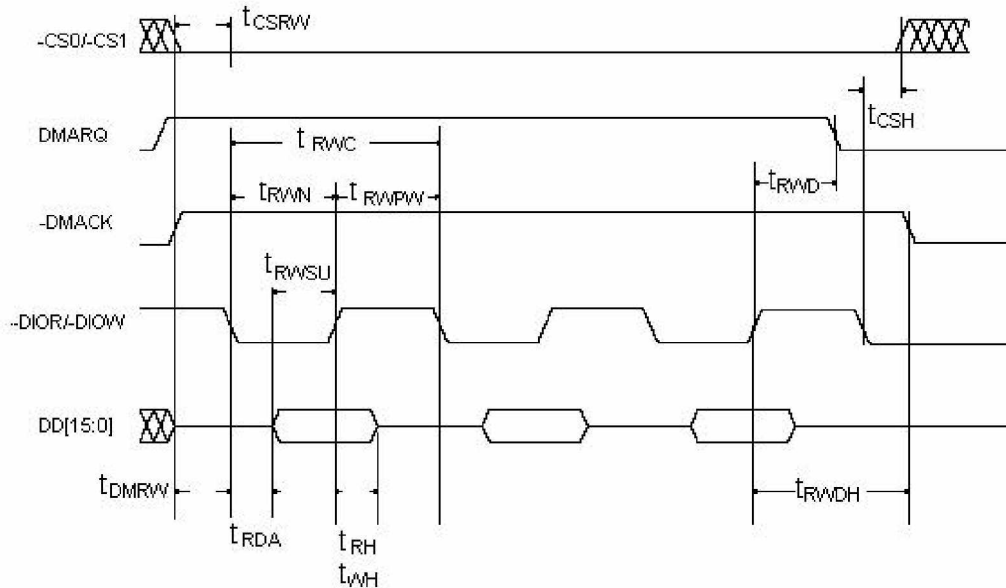
### 3.6.5. True IDE Read/Write Access Timing



| Symbol             | Parameter                             | Min | Max | Units |
|--------------------|---------------------------------------|-----|-----|-------|
| t <sub>ICL</sub>   | Cycle Time                            | 100 | -   | nsec  |
| t <sub>AVRWL</sub> | Address Valid to DIOR,DIOW Setup Time | 15  | -   |       |
| t <sub>RWPW</sub>  | DIOR, DIOW Pulse Width                | 65  | -   |       |
| t <sub>DVWL</sub>  | DIOW Data Setup Time                  | 20  | -   |       |
| t <sub>DXWH</sub>  | DIOW Data Hold Time                   | 5   | -   |       |
| t <sub>DVRL</sub>  | DIOR Data Setup Time                  | 15  | -   |       |
| t <sub>DXRH</sub>  | DIOR Data Hold Time                   | 5   | -   |       |
| t <sub>AV16L</sub> | Address Valid to IOCS16 Assertion     | -   | (1) |       |
| t <sub>AX16H</sub> | Address Valid to IOCS16 Negation      | -   | (1) |       |
| t <sub>AXRWH</sub> | DIOW,DIOR to Address Valid Hold Time  | 10  | -   |       |
| t <sub>IOST</sub>  | IORDY Setup Time                      | -   | (1) |       |
| t <sub>IOPW</sub>  | IORDY Pulse Width                     | -   | (1) |       |

Note: 1) IOIS16 and INPACK is not supported.

### 3.6.6. True IDE DMA Read/Write Access Timing\*



| Symbol     | Parameter                     | Min | Max | Units |
|------------|-------------------------------|-----|-----|-------|
| $t_{RWC}$  | Cycle Time (Mode 2)           | 100 | -   | nsec  |
| $t_{RWPW}$ | DIOR/DIOW Pulse Width         | 65  | -   |       |
| $t_{RDA}$  | DIOR Data Access              | -   | 50  |       |
| $t_{RWSU}$ | DIOR/DIOW Data Setup Time     | 15  | -   |       |
| $t_{RVH}$  | DIOW Data Hold Time           | 5   | -   |       |
| $t_{RH}$   | DIOR Data Hold Time           | 5   | -   |       |
| $t_{DMRW}$ | DMACK to DIOR/DIOW Setup Time | 0   | -   |       |
| $t_{RWDH}$ | DIOR/DIOW to DMACK Hold Time  | 5   | -   |       |
| $t_{RWN}$  | DIOR/DIOW negated Pulse Width | 25  | -   |       |
| $t_{RWD}$  | DIOR/DIOW to DMARQ Delay      | -   | 35  |       |
| $t_{CSRW}$ | CS(1:0) valid to DIOR/DIOW    | 10  | -   |       |
| $t_{CSH}$  | CS(1:0) Hold Time             | 10  | -   |       |

\* Does not apply to SiliconDrives that have DMA disabled.

## 4. ATTRIBUTE MEMORY DESCRIPTION & OPERATION

The Attribute Memory plane can be read or written to by asserting the REG# signal, qualified by the appropriate combination of CE1#, OE# and WE#. An Attribute memory map describing the type and location of the information maintained in the Attribute memory plane is provided in Section 4.3. Attribute Memory Map.

With respect to SiliconDrive PC Cards, Attribute memory consists of two sections, the Card Information Structure (CIS) and the Function Configuration Registers (FCR). The CIS contains a description of the card's capabilities and specifications. The FCR consists of four registers, which can be read or written to by a host to configure the card for specific purposes.

### 4.1. Attribute Memory Read Operations

Attribute memory read operations are enabled by asserting REG# , OE#, and CE1# low. Odd byte read operations from the attribute memory plane are not valid.

| Function Mode        | REG# | CE1# | CE2# | A0 | OE# | WE# | D[15:8]   | D[7:0]    |
|----------------------|------|------|------|----|-----|-----|-----------|-----------|
| Standby              | L    | H    | H    | X  | X   | X   | High-Z    | High-Z    |
| Byte Access          | L    | L    | H    | L  | L   | H   | High-Z    | Even      |
|                      | L    | H    | L    | H  | L   | H   | High-Z    | Not Valid |
| Word Access          | L    | L    | L    | X  | L   | H   | Not Valid | Even      |
| Odd Byte Only Access | L    | L    | H    | X  | H   | H   | Not Valid | High-Z    |

## 4.2. Attribute Memory Write Operations

Attribute memory write operations are enabled by asserting REG#, WE# and CE1# low. Odd byte write operations from the attribute memory plane are not valid.

| Function Mode        | REG# | CE1# | CE2# | A0 | OE# | WE# | D[15:8]   | D[7:0]    |
|----------------------|------|------|------|----|-----|-----|-----------|-----------|
| Standby              | L    | H    | H    | X  | X   | X   | High-Z    | High-Z    |
| Byte Access          | L    | L    | H    | L  | H   | L   | High-Z    | Even      |
|                      | L    | H    | L    | H  | H   | L   | High-Z    | Not Valid |
| Word Access          | L    | L    | L    | X  | H   | L   | Not Valid | Even      |
| Odd Byte Only Access | L    | L    | H    | X  | H   | H   | Not Valid | High-Z    |

## 4.3. Attribute Memory Map

As stated earlier, the Attribute Memory plane is comprised to two components the Card Information Structure (CIS) and the Function Configuration Registers (FCR). The following tables detail the type, location and read/write requirements for each of the four FCR's maintained in the Attribute Memory plane.

| Register                             | Operation | Addr | CE1# | REG# | WE# | OE# |
|--------------------------------------|-----------|------|------|------|-----|-----|
| Card Information Structure           | READ      | X    | 0    | 0    | 1   | 0   |
|                                      | WRITE     | X    | 0    | 0    | 0   | 1   |
| Configuration Option Register        | READ      | 200h | 0    | 0    | 1   | 0   |
|                                      | WRITE     | 200h | 0    | 0    | 0   | 1   |
| Card Configuration & Status Register | READ      | 202h | 0    | 0    | 1   | 0   |
|                                      | WRITE     | 202h | 0    | 0    | 0   | 1   |
| Pin Replacement Register             | READ      | 204h | 0    | 0    | 1   | 0   |
|                                      | WRITE     | 204h | 0    | 0    | 0   | 1   |
| Socket and Copy Register             | READ      | 206h | 0    | 0    | 1   | 0   |
|                                      | WRITE     | 206h | 0    | 0    | 0   | 1   |

## 4.4. Card Information Structure (CIS)

The CIS is data, which describes the SiliconDrive PC Card and is described by the PC Card standard. This information can be used by the Host system to determine a number of things about the card that has been inserted. For information regarding the exact nature of this data, and how to design Host software to interpret it, refer to the PC Card standard Metaformat Specification.

### 4.4. Card Information Structure (CIS)

| Attribute Offset | Data | 7                                       | 6 | 5           | 4            | 3                 | 2 | 1  | 0                                    | Description of Contents  | CIS Function                     |
|------------------|------|---|---|-------------|--------------|-------------------|---|--|--------------------------------------|--|----------------------------------|
| 00h              | 01h  | CISTPL_DEVICE                           |   |             |              |                   |   |  |                                      | Device Info Tuple  | Tuple Code                       |
| 02h              | 03h  |   |   |             |              |                   |   |  |                                      | Link length is 3 byte  | Link to Next Tuple               |
| 04h              | D9h  | Device Type Code<br>Dh= I/O             |   |             | W<br>1       | Device Speed<br>1 |   |  | I/O device<br>No WP<br>Speed = 100ns | Device ID<br>WPS<br>Device Speed                               |                                  |
| 06h              | 01h  | 1X                                      |   |             |              | 2k                |   |  |                                      | 2k byte of Address Space                                       | Device Size                      |
| 08h              | FFh  | List end Marker                         |   |             |              |                   |   |  |                                      | End of device  | END marker                       |
| 0Ah              | 1Ch  | CISTPL_DEVICE_OC                        |   |             |              |                   |   |  |                                      | Other conditions device in Tuple code                          | Tuple code                       |
| 0Ch              | 04h  | TPL_LINK                                |   |             |              |                   |   |  |                                      | Link Length is 4 Bytes   | Link to Next Tuple               |
| 0Eh              | 02h  | EXT Reserved VCC                        |   |             |              | MWAIT             |   |  |                                      | 3V, wait is Not Used   | Other Conditions Info Field      |
| 10h              | D9h  | Device type                             |   | W<br>P<br>S | Device speed |                   |   | Device type = DH: I/O device<br>WPS = 1: No WP<br>Device speed = 1: 250 ns |                                      |  |                                  |
| 12h              | 01h  | 1x                                      |   |             |              | 2k units          |   |  |                                      | 2k byte of address space                                       | Device size                      |
| 14h              | FFh  | List end marker                         |   |             |              |                   |   |  |                                      | End of device  | END marker                       |
| 16h              | 18h  | CISTPL_JEDEC_C                          |   |             |              |                   |   |  |                                      | JEDEC ID common memory   | Tuple code                       |
| 18h              | 02h  | TPL_LINK                                |   |             |              |                   |   |  |                                      | Link length is 2 bytes   | Link to next tuple               |
| 1Ah              | DFh  | PCMCIA Manufacturer's JEDEC             |   |             |              |                   |   |  |                                      | Manufacturer's ID code   | JEDEC ID                         |
| 1Ch              | 01h  | PCMCIA JEDEC Device Code                |   |             |              |                   |   |  |                                      | 2nd byte of JEDEC ID   |                                  |
| 1Eh              | 20h  | CISTPL_MANFID                           |   |             |              |                   |   |  |                                      | Manufacturer's ID code   | Tuple Code                       |
| 20h              | 04h  | TPL_LINK                                |   |             |              |                   |   |  |                                      |  |                                  |
| 22h              | 00h  | Low byte of PCMCIA manufacturer's code  |   |             |              |                   |   |  |                                      | JEDEC manufacturer's ID  | Low byte of manufacturer's code  |
| 24h              | 00h  | High byte of PCMCIA manufacturer's code |   |             |              |                   |   |  |                                      | Code of 0 because other byte is JEDEC 1 byte manufacturer's ID | High byte of manufacturer's code |
| 26h              | 00h  | Low byte of product code                |   |             |              |                   |   |  |                                      | Manufacturer's code for SiliconDrive CF                        | Low byte of product code         |

## 4.4. Card Information Structure (CIS)

| Attribute Offset | Data | 7                                  | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description of Contents  | CIS Function                        |
|------------------|------|------------------------------------|---|---|---|---|---|---|---|--|-------------------------------------|
| 28h              | 00h  | High byte of product code          |   |   |   |   |   |   |   | Manufacturer's code for SiliconDrive CF  | High byte of product code           |
| 2Ah              | 21h  | CISTPL_FUNCID                      |   |   |   |   |   |   |   | Function ID tuple  | Tuple code                          |
| 2Ch              | 02h  | TPL_LINK                           |   |   |   |   |   |   |   | Link length is 2bytes  | Link to next tuple                  |
| 2Eh              | 04h  | TPLFID_FUNCTION = 04H              |   |   |   |   |   |   |   | Disk function, may be silicon, may be removable  | PC card function code               |
| 30h              | 01h  | Reserved R P                       |   |   |   |   |   |   |   | R = 0: No BIOS ROM<br>P = 1: Configure card at power on  | System initialization byte          |
| 32h              | 22h  | CISTPL_FUNCE                       |   |   |   |   |   |   |   | Function extension tuple   | Tuple code                          |
| 34h              | 02h  | TPL_LINK                           |   |   |   |   |   |   |   | Link length is 2 bytes   | Link to next tuple                  |
| 36h              | 01h  | Disk function extension tuple type |   |   |   |   |   |   |   | Disk interface type  | Extension tuple type for disk       |
| 38h              | 01h  | Disk interface type                |   |   |   |   |   |   |   | PC card interface type   | Interface type                      |
| 3Ah              | 22h  | CISTPL_FUNCE                       |   |   |   |   |   |   |   | Function extension tuple   | Tuple code                          |
| 3Ch              | 03h  | TPL_LINK                           |   |   |   |   |   |   |   | Link length is 3 bytes   | Link to next tuple                  |
| 3Eh              | 02h  | Disk function extension Tuple type |   |   |   |   |   |   |   | Basic PCMCIA-ATA extension Tuple   | Extension Tuple type for disk       |
| 40h              | 04h  | Reserved D U S V                   |   |   |   |   |   |   |   | No Vpp, silicon, single drive<br>V = 0: No Vpp required<br>S = 0: Silicon<br>U = 1: Unique serial #<br>D = 0: Single drive on card   | Basic ATA option parameters byte 1  |
| 42h              | 07h  | R I E N P3 P2 P1 P0                |   |   |   |   |   |   |   | P0: Sleep mode supported<br>P1: Standby mode supp.<br>P2: Idle mode supported<br>P3: Drive auto power ctl<br>N: Some config excludes 3X7<br>E: Index bit is emulated<br>I: Twin IOIS16# data reg only<br>R: Reserved | Basic ATA option parameters byte 2  |
| 44h              | 1Ah  | CISTPL_CONFIG                      |   |   |   |   |   |   |   | Configuration tuple  | Tuple code                          |
| 46h              | 05h  | TPL_LINK                           |   |   |   |   |   |   |   | Link length is 5 bytes   | Link to next tuple                  |
| 48h              | 01h  | RFS RMS RAS                        |   |   |   |   |   |   |   | RFS: Reserved<br>RMS: TPCC_RMSK size-1 = 0<br>RAS: TPCC_RADR size-1 = 1<br>1 byte register mask<br>2 byte config base address  | Size of fields byte TPCC_SZ         |
| 4Ah              | 07h  | TPCC_LAST                          |   |   |   |   |   |   |   | Entry with config index of 7 is final entry in table   | Last entry of config registers      |
| 4Ch              | 00h  | TPCC_RADR (LSB)                    |   |   |   |   |   |   |   | Config. Reg. are located at 200H in REG space  | Location of configuration registers |
| 4Eh              | 02h  | TPCC_RADR (MSB)                    |   |   |   |   |   |   |   |  |                                     |

## 4.4. Card Information Structure (CIS)

| Attribute Offset | Data | 7                               | 6        | 5                   | 4  | 3              | 2  | 1  | 0                                       | Description of Contents  | CIS Function   |   |
|------------------|------|---------------------------------|----------|---------------------|----|----------------|----|----|---|--|--|---|
| 50h              | 0Fh  | Reserved                        | S        | P                   | C  | I              |    |    |   | I: Configuration index<br>C: Configuration and status<br>P: Pin replacement<br>S: Socket and copy  | Configuration registers present mask<br>TPCC_RMSK  |   |
| 52h              | 1Bh  | CISTPL_TABLE_ENTRY              |          |                     |    |                |    |    |   | Configuration table entry tuple  | Tuple code   |   |
| 54h              | 0Bh  | TPL_LINK                        |          |                     |    |                |    |    |   | Link length is 11 bytes  | Link to next tuple   |   |
| 56h              | C0h  | I                               | D        | Configuration index |    |                |    |    |   |  | Memory mapped I/O configuration<br>I = 1: Interface byte follows<br>D = 1: Default entry<br>Configuration index = 0  | Configuration table index byte<br>TPCE_INDX |
| 58h              | C0h  | W                               | R        | P                   | B  | Interface type |    |    |   | W = 0: Wait not used<br>R = 1: Ready active<br>P = 0: WP used<br>B = 0: BVD1 and BVD2 not used<br>IF type = 0: Memory interface  | Interface description field<br>TPCE_IF   |   |
| 5Ah              | A1h  | M                               | MS       | IR                  | IO | T              | P  |    |   |  | M = 1: Misc info present<br>MS = 01: Memory space info<br>single 2-byte length<br>IR = 0: No interrupt info present<br>IO = 0: No I/O port info present<br>T = 0: No timing info present<br>P = 1: VCC only info | Feature selection byte<br>TPCE_FS           |
| 5Ch              | 27h  | R                               | DI       | PI                  | AI | SI             | HV | LV | NV                                      | Nominal voltage only follows<br>R: Reserved<br>DI: Power down current info<br>PI: Peak current info<br>AI: Average current info<br>SI: Static current info<br>HV: Max voltage info<br>LV: Min voltage info<br>NV: Nominal voltage info | Power parameters for VCC   |   |
| 5Eh              | 55h  | X                               | Mantissa |                     |    | Exponent       |    |    | Nominal voltage = 5 V                   |  |  | VCC nominal value                           |
| 60h              | 4Dh  | X                               | Mantissa |                     |    | Exponent       |    |    | VCC nominal 4.5V                        |  |  | VCC min value                               |
| 62h              | 5Dh  | X                               | Mantissa |                     |    | Exponent       |    |    | VCC nominal 5.5V                        |  |  | VCC max value                               |
| 64h              | 75h  | X                               | Mantissa |                     |    | Exponent       |    |    | Max average current over 10msec is 80mA |  |  | Max average current                         |
| 66h              | 08h  | Length in 256 bytes pages (LSB) |          |                     |    |                |    |    |   | Length of memory space is 2kB  | Memory space description structures (TPCE_MS)  |   |
| 68h              | 00h  | Length in 256 bytes pages (MSB) |          |                     |    |                |    |    |   |  |  |   |

## 4.4. Card Information Structure (CIS)

| Attribute Offset | Data | 7                  | 6        | 5                   | 4  | 3  | 2        | 1  | 0     | Description of Contents  | CIS Function   |   |
|------------------|------|--------------------|----------|---------------------|----|----|----------|----|-------|--|--|---|
| 6Ah              | 21h  | X                  | R        | P                   | RO | A  | T        |    |       | X = 0: No more misc fields<br>R: Reserved<br>P = 1: Power down supported<br>RO = 0: Not read only mode<br>A = 0: Audio not supported<br>T = 0: Single drive  | Miscellaneous features field TPCE_MI   |   |
| 6Ch              | 1Bh  | CISTPL_TABLE_ENTRY |          |                     |    |    |          |    |       | Configuration table entry tuple  | Tuple Code   |   |
| 6Eh              | 06h  | TPL_LINK           |          |                     |    |    |          |    |       | Link length is 6 bytes   | Link to next tuple   |   |
| 70h              | 00h  | I                  | D        | Configuration index |    |    |          |    |       |  | Memory mapped I/O configuration<br>I = 0: No Interface byte<br>D = 0: No Default entry<br>Configuration index = 0  | Configuration table index byte<br>TPCE_INDX |
| 72h              | 01h  | M                  | MS       | IR                  | IO | T  | P        |    |       |  | M = 0: No Misc info<br>MS = 00: No Memory space info<br>IR = 0: No interrupt info present<br>IO = 0: No I/O port info present<br>T = 0: No timing info present<br>P = 1: VCC only info | Feature selection byte<br>TPCE_FS           |
| 74h              | 21h  | R                  | DI       | PI                  | AI | SI | HV       | LV | NV    | Nominal voltage only follows<br>R: Reserved<br>DI: Power down current info<br>PI: Peak current info<br>AI: Average current info<br>SI: Static current info<br>HV: Max voltage info<br>LV: Min voltage info<br>NV: Nominal voltage info | Power parameters for VCC   |   |
| 76h              | B5h  | X                  | Mantissa |                     |    |    | Exponent |    |       | Nominal voltage = 3.0 V  | VCC nominal value  |   |
| 78h              | 1Eh  | Extension          |          |                     |    |    |          |    |       | +0.3 V   | Extension byte   |   |
| 7Ah              | 4Dh  | X                  | Mantissa |                     |    |    | Exponent |    |       | Max average current over 10msec is 45 mA   | Max. average current   |   |
| 7Ch              | 1Bh  | CISTPL_TABLE_ENTRY |          |                     |    |    |          |    |       | Configuration table entry Tuple  | Tuple code   |   |
| 7Eh              | 0Dh  | TPL_LINK           |          |                     |    |    |          |    |       | Link length is 10 bytes  | Link to next tuple   |   |
| 80h              | C1h  | I                  | D        | Configuration       |    |    |          |    | INDEX |  | Contiguous I/O mapped ATA registers configuration<br>I = 1: Interface byte follows<br>D = 1: Default entry<br>Configuration index = 1  | Configuration table index byte TPCE_INDX    |

## 4.4. Card Information Structure (CIS)

| Attribute Offset | Data | 7  | 6        | 5  | 4        | 3              | 2        | 1  | 0  | Description of Contents   | CIS Function  |  |
|------------------|------|----|----------|----|----------|----------------|----------|----|----|---|---|--|
| 82h              | 41h  | W  | R        | P  | B        | Interface type |          |    |    | W = 0: Wait not used<br>R = 1: Ready active<br>P = 0: WP not used<br>B = 0: BVS1 and BVD2 not used<br>IF type = 1: I/O interface  | Interface description field<br>TPCE_IF  |  |
| 84h              | 99h  | M  | MS       | IR | IO       | T              | P        |    |    |   | M = 1: Misc info present<br>MS = 00: No memory space info<br>IR = 1: Interrupt info present<br>IO = 1: I/O port info present<br>T = 0: No timing info present<br>P = 1: VCC only info | Feature selection byte<br>TPCE_FS      |
| 86h              | 27h  | R  | DI       | PI | AI       | SI             | HV       | LV | NV | Nominal voltage only follows<br>R: Reserved<br>DI: Power down Curr. info<br>PI: Peak current info<br>AI: Average current info<br>SI: Static current info<br>HV: Max voltage info<br>LV: Min voltage info<br>NV: Nominal voltage info    | Power parameters for VCC  |  |
| 88h              | 55h  | X  | Mantissa |    | Exponent |                |          |    |    |   | Nominal voltage = 5 V   | VCC nominal value                      |
| 8Ah              | 4Dh  | X  | Mantissa |    | Exponent |                |          |    |    |   | VCC nominal 4.5V  | VCC min value                          |
| 8Ch              | 5Dh  | X  | Mantissa |    | Exponent |                |          |    |    |   | VCC nominal 5.5V  | VCC max value                          |
| 8Eh              | 75h  | X  | Mantissa |    | Exponent |                |          |    |    |   | Max average current over 10msec is 80mA   | Max average current                    |
| 90h              | 64h  | R  | S        | E  | I        | O              | AddrLine |    |    |   | S = 1: 16-bit hosts supported<br>E = 1: 8-bit hosts supported<br>IO AddrLine: 4 lines decoded   | I/O space description field<br>TPCE_IO |
| 92h              | F0h  | S  | P        | L  | M        | V              | B        | I  | N  | S = 1: Share logic active<br>P = 1: Pulse mode IRQ supported<br>L = 1: Level mode IRQ supported<br>M = 1: Bit mask of IRQs present<br>V = 0: No vender unique IRQ<br>B = 0: No bus error IRQ<br>I = 0: No IO check IRQ<br>N = 0: No NMI | Interrupt request description structure<br>TPCE_IR  |  |
| 94h              | FFh  | IR | IR       | IR | IR       | IR             | IR       | IR | IR | IRQ level to be routed 0 to 15 recommended  | Mask extension byte 1<br>TPCE_IR  |  |
|                  |      | Q  | Q        | Q  | Q        | Q              | Q        | Q  | Q  |   |   |  |
|                  |      | 7  | 6        | 5  | 4        | 3              | 2        | 1  | 0  |   |   |  |

## 4.4. Card Information Structure (CIS)

| Attribute Offset | Data | 7                  | 6        | 5                   | 4  | 3        | 2  | 1  | 0  | Description of Contents  | CIS Function  |   |
|------------------|------|--------------------|----------|---------------------|----|----------|----|----|----|--|---|---|
| 96h              | FFh  | IR                 | IR       | IR                  | IR | IR       | IR | IR | IR | Recommended routing to any "normal, maskable" IRQ.   | Mask extension byte 2<br>TPCE_IR  |   |
| 98h              | 21h  | X                  | R        | P                   | R  | O        | A  | T  |    | X = 0: No more misc fields<br>R: reserved<br>P = 1: Power down supp.<br>RO = 0: Not read only mode<br>A = 0: Audio not supported<br>T = 0: Single drive  | Miscellaneous features field<br>TPCE_MI   |   |
| 9Ah              | 1Bh  | CISTPL_TABLE_ENTRY |          |                     |    |          |    |    |    | Configuration table entry tuple  | Tuple code  |   |
| 9Ch              | 06h  | TPL_LINK           |          |                     |    |          |    |    |    | Link length is 6 bytes   | Link to next tuple  |   |
| 9Eh              | 01h  | I                  | D        | Configuration index |    |          |    |    |    |  | Contiguous I/O mapped ATA registers configuration<br>I = 0: No Interface byte<br>D = 0: No Default entry<br>Configuration index = 1 | Configuration table index<br>Byte TPCE_INDX |
| A0h              | 01h  | M                  | MS       | IR                  | IO | T        | P  |    |    | M = 0: No Misc info<br>MS = 00: No Memory space info<br>IR = 0: No interrupt info present<br>IO = 0: No I/O port info present<br>T = 0: No timing info present<br>P = 1: VCC only info   | Feature selection byte<br>TPCE_FS   |   |
| A2h              | 21h  | R                  | DI       | PI                  | AI | SI       | HV | LV | NV | Nominal voltage only follows<br>R: Reserved<br>DI: Power down current info<br>PI: Peak current info<br>AI: Average current info<br>SI: Static current info<br>HV: Max voltage info<br>LV: Min voltage info<br>NV: Nominal voltage info | Power parameters for VCC  |   |
| A4h              | B5h  | X                  | Mantissa |                     |    | Exponent |    |    |    |  | Nominal voltage = 3.0 V   | VCC nominal value                           |
| A6h              | 1Eh  | X                  | Mantissa |                     |    | Exponent |    |    |    |  | +0.3 V  | Extension byte                              |
| A8h              | 4Dh  | X                  | Mantissa |                     |    | Exponent |    |    |    |  | Max average current over 10msec is 45 mA  | Max. average current                        |
| AAh              | 1Bh  | CISTPL_TABLE_ENTRY |          |                     |    |          |    |    |    | Configuration table entry Tuple  | Extension Byte  |   |
| ACh              | 12h  | TPL_LINK           |          |                     |    |          |    |    |    | Link length is 18 bytes  | Link to next tuple  |   |
| AEh              | C2h  | I                  | D        | Configuration INDEX |    |          |    |    |    |  | ATA primary I/O mapped configuration<br>I = 1: Interface byte follows<br>D = 1: default entry follows<br>Configuration index = 2    | Configuration table index<br>byte TPCE_INDX |

## 4.4. Card Information Structure (CIS)

| Attribute Offset | Data | 7                                | 6        | 5  | 4        | 3              | 2  | 1  | 0   | Description of Contents  | CIS Function  |                                   |
|------------------|------|----------------------------------|----------|----|----------|----------------|----|----|---|--|---|-----------------------------------|
| B0h              | 41h  | W                                | R        | P  | B        | Interface type |    |    |   | W = 0: Wait not used<br>R = 1: Ready active<br>P = 0: WP not used<br>B = 0: BVS1 and BVD2 not used<br>IF type = 1: I/O interface   | Interface description field<br>TPCE_IF  |                                   |
| B2h              | 99h  | M                                | MS       | IR | IO       | T              | P  |    |   |  | M = 1: misc info present<br>MS = 00: No memory space info<br>IR = 1: Interrupt info present<br>IO = 1: I/O port info present<br>T = 0: No timing info present<br>P = 1: VCC only info | Feature selection byte<br>TPCE_FS |
| B4h              | 27h  | R                                | DI       | PI | AI       | SI             | HV | LV | NV  | Nominal voltage only follows<br>R: Reserved<br>DI: Power down Curr. info<br>PI: Peak current info<br>AI: Average current info<br>SI: Static current info<br>HV: Max voltage info<br>LV: Min voltage info<br>NV: Nominal voltage info | Power parameters for VCC  |                                   |
| B6h              | 55h  | X                                | Mantissa |    | Exponent |                |    |    |   |  | Nominal voltage = 5 V   | VCC nominal value                 |
| B8h              | 4Dh  | X                                | Mantissa |    | Exponent |                |    |    |   |  | VCC nominal 4.5V  | VCC min value                     |
| BAh              | 5Dh  | X                                | Mantissa |    | Exponent |                |    |    |   |  | VCC nominal 5.5V  | VCC max value                     |
| BCh              | 75h  | X                                | Mantissa |    | Exponent |                |    |    |   |  | Max average current over 10msec is 80mA   | Max average current               |
| BEh              | EAh  | R                                | S        | E  | IO       | AddrLine       |    |    |   | R = 1: Range follows<br>S = 1: 16-bit hosts supported<br>E = 1: 8-bit hosts supported<br>IO AddrLines: 10 lines decoded  | I/O space description field<br>TPCE_IO  |                                   |
| C0h              | 61h  | LS                               | AS       |    | N range  |                |    |    | LS = 1: Size of lengths is 1 byte<br>AS = 2: Size of address is 2 bytes<br>N Range = 1: Address Range-1 |  |   | I/O range format description      |
| C2h              | F0h  | 1 <sup>st</sup> I/O base address |          |    |          |                |    |    |   |  | 1st I/O base address (LSB)  | 1st I/O range address             |
| C4h              | 01h  | 1 <sup>st</sup> I/O base address |          |    |          |                |    |    |   |  | 1st I/O base address (MSB)  |                                   |
| C6h              | 07h  | 1 <sup>st</sup> I/O base address |          |    |          |                |    |    |   |  | 1st I/O length - 1  | 1st I/O range length              |

## 4.4. Card Information Structure (CIS)

| Attribute Offset | Data | 7                                | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description of Contents  | CIS Function                                       |
|------------------|------|----------------------------------|---|---|---|---|---|---|---|--|--|
| C8h              | F6h  | 2 <sup>nd</sup> I/O base address |   |   |   |   |   |   |   | 2 <sup>nd</sup> I/O base address (LSB)   | 2 <sup>nd</sup> I/O range address                  |
| CAh              | 03h  | 2 <sup>nd</sup> I/O base address |   |   |   |   |   |   |   | 2 <sup>nd</sup> I/O base address(MSB)  |  |
| CCh              | 01h  | 2 <sup>nd</sup> I/O range length |   |   |   |   |   |   |   | 2 <sup>nd</sup> I/O length – 1   | 2 <sup>nd</sup> I/O range length                   |
| CEh              | EEh  | S P L M IRQ level                |   |   |   |   |   |   |   | S = 1: Share logic active<br>P = 1: Pulse mode IRQ supported<br>L = 1: Level mode IRQ supported<br>M = 0: Bit mask of IRQs present<br>IRQ level is IRQ14                               | Interrupt request description structure<br>TPCE_IR |
| D0h              | 21h  | X R P RO A T                     |   |   |   |   |   |   |   | X = 0: No more misc fields<br>R: reserved<br>P = 1: Power down supp.<br>RO = 0: Not read only mode<br>A = 0: Audio not supported<br>T = 0: Single drive                                | Miscellaneous features field<br>TPCE_MI            |
| D2h              | 1Bh  | CISTPL_TABLE_ENTRY               |   |   |   |   |   |   |   | Configuration table entry Tuple  | Tuple code   |
| D4h              | 06h  | TPL_LINK                         |   |   |   |   |   |   |   | Link length is 6 bytes   | Link to next tuple                                 |
| D6h              | 02h  | I D Configuration index          |   |   |   |   |   |   |   | ATA primary I/O mapped configuration<br>I = 0: No Interface byte<br>D = 0: No Default entry<br>Configuration index = 2   | Configuration table index<br>Byte TPCE_INDX        |
| D8h              | 01h  | I D Configuration index          |   |   |   |   |   |   |   | Contiguous I/O mapped ATA registers configuration<br>I = 0: No Interface byte<br>D = 0: No Default entry<br>Configuration index = 1  | Configuration table index<br>Byte TPCE_INDX        |
| DAh              | 21h  | M MS IR IO T P                   |   |   |   |   |   |   |   | M = 0: No Misc info<br>MS = 00: No Memory space info<br>IR = 0: No interrupt info present<br>IO = 0: No I/O port info present<br>T = 0: No timing info present<br>P = 1: VCC only info | Feature selection byte<br>TPCE_FS                  |

## 4.4. Card Information Structure (CIS)

| Attribute Offset | Data | 7                  | 6        | 5  | 4        | 3  | 2  | 1  | 0  | Description of Contents  | CIS Function  |                                   |
|------------------|------|--------------------|----------|----|----------|----|----|----|----|--|---|-----------------------------------|
| DCh              | B5h  | R                  | DI       | PI | AI       | SI | HV | LV | NV | Nominal voltage only follows<br>R: Reserved<br>DI: Power down current info<br>PI: Peak current info<br>AI: Average current info<br>SI: Static current info<br>HV: Max voltage info<br>LV: Min voltage info<br>NV: Nominal voltage info | Power parameters for VCC  |                                   |
| DEh              | 1Eh  | X                  | Mantissa |    | Exponent |    |    |    |    |  | Nominal voltage = 3.0 V   | VCC nominal value                 |
| E0h              | 4Dh  | Extension          |          |    |          |    |    |    |    | +0.3 V   | Extension byte  |                                   |
| E2h              | 1Bh  | CISTPL_TABLE_ENTRY |          |    |          |    |    |    |    | Config. table entry Tuple  | Tuple code  |                                   |
| E4h              | 12h  | TPL_LINK           |          |    |          |    |    |    |    | Link length is 18 bytes  | Link to next tuple  |                                   |
| E6h              | C3h  | M                  | MS       | IR | IO       | T  | P  |    |    |  | M = 0: No Misc info<br>MS = 00: No Memory space info<br>IR = 0: No interrupt info present<br>IO = 0: No I/O port info present<br>T = 0: No timing info present<br>P = 1: VCC only info  | Feature selection byte<br>TPCE_FS |
| E8h              | 41h  | R                  | DI       | PI | AI       | SI | HV | LV | NV | Nominal voltage only follows<br>R: Reserved<br>DI: Power down current info<br>PI: Peak current info<br>AI: Average current info<br>SI: Static current info<br>HV: Max voltage info<br>LV: Min voltage info<br>NV: Nominal voltage info | Power parameters for VCC  |                                   |
| EAh              | 99h  | M                  | MS       | IR | IO       | T  | P  |    |    |  | M = 1: No Misc info<br>MS = 00: No Memory space info<br>IR = 1: No interrupt info present<br>IO = 1: No I/O port info present<br>T = 0: No timing info present<br>P = 01: VCC only info | Feature selection byte<br>TPCE_FS |

## 4.4. Card Information Structure (CIS)

| Attribute Offset | Data | 7  | 6        | 5       | 4        | 3        | 2     | 1  | 0  | Description of Contents  | CIS Function   |   |                              |
|------------------|------|----|----------|---------|----------|----------|-------|----|----|--|--|---|------------------------------|
| ECh              | 27h  | R  | DI       | PI      | AI       | SI       | HV    | LV | NV | Nominal voltage only follows<br>R: Reserved<br>DI: Power down Curr. info<br>PI: Peak current info<br>AI: Average current info<br>SI: Static current info<br>HV: Max voltage info<br>LV: Min voltage info<br>NV: Nominal voltage info | Power parameters for VCC   |   |                              |
| EEh              | 55h  | X  | Mantissa |         | Exponent |          |       |    |    |  | Nominal voltage = 5 V  | VCC nominal value   |                              |
| F0h              | 4Dh  | X  | Mantissa |         | Exponent |          |       |    |    |  | VCC nominal 4.5V   | VCC min value   |                              |
| F2h              | 5Dh  | X  | Mantissa |         | Exponent |          |       |    |    |  | VCC nominal 5.5V   | VCC max value   |                              |
| F4h              | 75h  | X  | Mantissa |         | Exponent |          |       |    |    |  | Max average current over 10msec is 80mA  | Max average current   |                              |
| F6h              | EAh  | R  | S        | E       | IO       | AddrLine |       |    |    | R = 1: Range follows<br>S = 1: 16-bit hosts supported<br>E = 1: 8-bit hosts supported<br>IO AddrLines: 10 lines Decoded  | I/O space description field TPCE_IO  |   |                              |
| F8h              | 61h  | LS | AS       | N range |          |          |       |    |    |  |  | LS = 1: Size of lengths is 1 Byte<br>AS = 2: Size of address is 2 bytes<br>N Range = 1: Address range - 1 | I/O range format description |
| FAh              | 70h  |    |          |         |          |          |       |    |    |  | 1st I/O base address (LSB)   | 1st I/O range address   |                              |
| FCh              | 01h  |    |          |         |          |          |       |    |    |  | 1st I/O base address (MSB)   |   |                              |
| FEh              | 07h  |    |          |         |          |          |       |    |    |  | 1st I/O length - 1   | 1st I/O range length  |                              |
| 100h             | 76h  |    |          |         |          |          |       |    |    |  | 2nd I/O base address (LSB)   | 2nd I/O range address   |                              |
| 102h             | 03h  |    |          |         |          |          |       |    |    |  | 2nd I/O base address (MSB)   |   |                              |
| 104h             | 01h  |    |          |         |          |          |       |    |    |  | 2 <sup>nd</sup> I/O length   | 2st I/O range length  |                              |
| 106h             | EEh  | S  | P        | L       | M        | IRQ      | level |    |    |  | S = 1: Share logic active<br>P = 1: Pulse mode IRQ supported<br>L = 1: Level mode IRQ supported<br>M = 0: Bit mask of IRQs present<br>IRQ level is IRQ14 | Interrupt request description structure TPCE_IR<br>Miscellaneous features field TPCE_MI                   |                              |

## 4.4. Card Information Structure (CIS)

| Attribute Offset | Data | 7                  | 6        | 5                   | 4  | 3  | 2        | 1  | 0  | Description of Contents  | CIS Function   |  |
|------------------|------|--------------------|----------|---------------------|----|----|----------|----|----|--|--|--|
| 108h             | 21h  | X                  | R        | P                   | RO | A  | T        |    |    | X = 0: No more misc fields<br>R: reserved<br>P = 1: Power down supported<br>RO = 0: Not read only mode<br>A = 0: Audio not supported<br>T = 0: Single drive  |  |  |
| 10Ah             | 1Bh  | CISTPL_TABLE_ENTRY |          |                     |    |    |          |    |    | Configuration table entry Tuple  | Tuple code   |  |
| 10Ch             | 06h  | TPL_LINK           |          |                     |    |    |          |    |    | Link length is 6 bytes   | Link to next tuple   |  |
| 10Eh             | 03h  | I                  | D        | Configuration index |    |    |          |    |    |  | ATA primary I/O mapped configuration<br>I = 0: No Interface byte<br>D = 0: No Default entry<br>Configuration index = 2 | Configuration table index<br>Byte TPCE_INDXX |
| 110h             | 01h  | M                  | MS       | IR                  | IO | T  | P        |    |    | M = 0: No Misc info<br>MS = 00: No Memory space info<br>IR = 0: No interrupt info present<br>IO = 0: No I/O port info present<br>T = 0: No timing info present<br>P = 1: VCC only info   | Feature selection byte<br>TPCE_FS  |  |
| 112h             | 21h  | R                  | DI       | PI                  | AI | SI | HV       | LV | NV | Nominal voltage only follows<br>R: Reserved<br>DI: Power down current info<br>PI: Peak current info<br>AI: Average current info<br>SI: Static current info<br>HV: Max voltage info<br>LV: Min voltage info<br>NV: Nominal voltage info | Power parameters for VCC   |  |
| 114h             | B5h  | X                  | Mantissa |                     |    |    | Exponent |    |    | Nominal voltage = 3.0 V  | VCC nominal value  |  |
| 116h             | 1Eh  | Extension          |          |                     |    |    |          |    |    | +0.3 V   | Extension byte   |  |
| 118h             | 4Dh  | X                  | Mantissa |                     |    |    | Exponent |    |    | Max average current over 10msec is 45 mA   | Max. average current   |  |
| 11Ah             | 1Bh  | CISTPL_MANFID      |          |                     |    |    |          |    |    | Manufacturer's ID code   | Tuple Code   |  |
| 11Ch             | 04h  | TPL_LINK           |          |                     |    |    |          |    |    | Link length is 4 bytes   | Link to next tuple   |  |
| 11Eh             | 07h  | I                  | D        | Configuration Index |    |    |          |    |    |  | AT Fixed Disk Secondary I/O 3.3V configuration   | TPCE_INDXX                                   |
| 120h             | 00h  | M                  | MS       | IR                  | IO | T  | P        |    |    | P: Power info type   | TPCL_FS  |  |
| 122h             | 28h  |                    |          |                     |    |    |          |    |    | Manufacturer code for SiliconDrive CF  | Reserved   |  |

## 4.4. Card Information Structure (CIS)

| Attribute Offset | Data | 7              | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description of Contents               | CIS Function       |
|------------------|------|----------------|---|---|---|---|---|---|---|---------------------------------------|--------------------|
| 124h             | D3h  |                |   |   |   |   |   |   |   | Manufacturer code for SiliconDrive CF | Reserved           |
| 126h             | 14h  | CISTPL_NO_LINK |   |   |   |   |   |   |   | No link control tuple                 | Tuple code         |
| 128h             | 00h  |                |   |   |   |   |   |   |   | Link is 0 bytes                       | Link to next tuple |
| 12Ah             | 15h  | CISTPL_VERS_1  |   |   |   |   |   |   |   | Level 1 version                       | Tuple code         |
| 12Ch             | 1Ah  | TPL_LINK       |   |   |   |   |   |   |   | Link length is 26h bytes              | Link to Next Tuple |
| 12Eh             | 04h  | TPPLV1_MAJOR   |   |   |   |   |   |   |   | PC Card 2.0/JEIDA4.1                  | END marker         |
| 130h             | 01h  | TPPLV1_MINOR   |   |   |   |   |   |   |   | PC Card 2.0/JEIDA4.1                  | Tuple code         |
| 132h             | 53h  |                |   |   |   |   |   |   |   | S                                     | Info String        |
| 134h             | 49h  |                |   |   |   |   |   |   |   | I                                     |                    |
| 136h             | 4Ch  |                |   |   |   |   |   |   |   | L                                     |                    |
| 138h             | 49h  |                |   |   |   |   |   |   |   | I                                     |                    |
| 13Ah             | 43h  |                |   |   |   |   |   |   |   | C                                     |                    |
| 13Ch             | 4Fh  |                |   |   |   |   |   |   |   | O                                     |                    |
| 13Eh             | 4Eh  |                |   |   |   |   |   |   |   | N                                     |                    |
| 140h             | 53h  |                |   |   |   |   |   |   |   | S                                     |                    |
| 142h             | 59h  |                |   |   |   |   |   |   |   | Y                                     |                    |
| 144h             | 53h  |                |   |   |   |   |   |   |   | S                                     |                    |
| 146h             | 54h  |                |   |   |   |   |   |   |   | T                                     |                    |
| 148h             | 45h  |                |   |   |   |   |   |   |   | E                                     |                    |
| 14Ah             | 4Dh  |                |   |   |   |   |   |   |   | M                                     |                    |
| 14Ch             | 53h  |                |   |   |   |   |   |   |   | S                                     |                    |
| 14Eh             | 00h  |                |   |   |   |   |   |   |   | "Space"                               |                    |
| 150h             | 56h  |                |   |   |   |   |   |   |   | V                                     |                    |
| 152h             | 45h  |                |   |   |   |   |   |   |   | E                                     |                    |
| 154h             | 52h  |                |   |   |   |   |   |   |   | R                                     |                    |
| 156h             | 32h  |                |   |   |   |   |   |   |   | 2                                     |                    |
| 158h             | 2Eh  |                |   |   |   |   |   |   |   | .                                     |                    |
| 15Ah             | 30h  |                |   |   |   |   |   |   |   | 0                                     |                    |
| 15Ch             | 30h  |                |   |   |   |   |   |   |   | 0                                     |                    |
| 15Eh             | 00h  |                |   |   |   |   |   |   |   |                                       |                    |
| 160h             | FFh  |                |   |   |   |   |   |   |   |                                       |                    |

## 4.5. Configuration Option Register (200h)

The Configuration Option Register is used to configure the SiliconDrive PC Card, define the address decoding, and initiate the software RESET sequence.

| Operation     | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub>      | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|----------------|----------------|---------------------|----------------|----------------|----------------|----------------|----------------|
| Read/Write    | SRESET         | LevIREQ        | Configuration Index |                |                |                |                |                |
| Default Value | 0              | 0              | 0                   | 0              | 0              | 0              | 0              | 0              |

**Notes**

- SRESET:                               When set this bit initiates a software reset sequence, which is equivalent to a Power-On Reset or Hardware Reset.
- LevIREQ:                              IREQ# interrupt signal level mode select:  
Logic '0' = Pulse mode, logic '1' = Level mode.
- Configuration Index:               Memory Mapped Mode   000000B  
  Independent I/O Mode   000001B  
  Primary Mode           000010B  
  Secondary Mode        000011B

## 4.6. Configuration & Status Register (202h)

The Configuration and Status Register (CSR) informs the host of any status changes with regard to power-down.

| Operation     | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read          | Changed        | SigChg         | IOis8          | 0              | 0              | PwrDn          | Int            | 0              |
| Write         | 0              | SigChg         | IOis8          | 0              | 0              | PwrDn          | 0              | 0              |
| Default Value | 0              | 0              | 0              | 0              | 0              | 0              | 0              | 0              |

### Notes

- Changed:** Indicates that either CREADY (D5) or CWPort (D4) of the Pin Replacement Register is set. Additionally, this bit changes state as the Power Down (D2) bit changes.
- SigChg:** Outputs the inverse state of the Changed bit to the hardware interface signal STSCHG# at the card interface.
- IOis8:** Informs the host of the valid data bus width for the operations in progress, "0" indicates a 16-bit data transfer, "1" indicates an 8-bit data transfer.
- PwrDwn:** Indicates the state of the card: Operating – "0", or Power Down mode "1". During power-down mode, no commands are accepted. Additionally, the host may not initiate a Power-Down request when the card is BUSY via the Status Register or the Hardware RDY/BSY pin.
- Int:** Indicates the inverse of the IREQ# status signal.

## 4.7. Pin Placement Register (204h)

| Operation     | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read/Write    | CBVD1          | CBVD2          | CRDY           | CWProt         | RBVD1          | RBVD2          | RRDY           | RWProt         |
| Default Value | 0              | 0              | 0              | 0              | 1              | 1              | 0              | 0              |

### Notes

- CRDY:** Indicates a bit change in the RRDY (D1) bit.
- CWProt** Indicates a bit change in the RWProt (D0) bit.
- RRDY:** When set high "1" informs the host that the card is ready, low "0" state indicates the card is busy.
- RWProt:** Indicates Write Protect is enabled when set to "1", and disabled when "0".

## 4.8. Socket & Copy Register (206h)

| Operation     | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read/Write    | RFU            | Copy Number    |                |                | Socket Number  |                |                |                |
| Default Value | 0              | 0              | 0              | 0              | 0              | 0              | 0              | 0              |

### Notes

RFU: Reserved for future use.

Copy Number: Indicates the card number. Allows the host to differentiate between identical card by writing to this bit which card is being accessed. This value will be compared to the DRV bit in the ATA Drive/Head Register.

Card 0: 000B = (D6,D5,D4). (Default).

Card 1: 001B = (D6,D5,D4). (Alternate).

Socket Number: The host writes the socket number identifying the inserted card.

## 5. COMMON MEMORY DESCRIPTION & OPERATION

Common memory space can be accessed when the card is configured in Memory Mapped mode.

### 5.1. Common Memory Read Operations

Common memory write operations are issued by asserting either CE1# or CE2# or both, and OE# low, REG# and WE# must be inactive.

| Function Mode        | REG# | CE1# | CE2# | A0 | OE# | WE# | D[15:8] | D[7:0] |
|----------------------|------|------|------|----|-----|-----|---------|--------|
| Standby              | H    | H    | H    | X  | X   | X   | High-Z  | High-Z |
| Byte Access          | H    | L    | H    | L  | L   | H   | High-Z  | Even   |
|                      | H    | H    | L    | H  | L   | H   | High-Z  | Odd    |
| Word Access          | H    | L    | L    | X  | L   | H   | Odd     | Even   |
| Odd Byte Only Access | H    | L    | H    | X  | H   | H   | Odd     | High-Z |

### 5.2. Common Memory Write Operations

Common memory read operations are issued by asserting either CE1# or CE2# or both, and OE# low, REG# and WE# must be inactive.

| Function Mode        | REG# | CE1# | CE2# | A0 | OE# | WE# | D[15:8] | D[7:0] |
|----------------------|------|------|------|----|-----|-----|---------|--------|
| Standby              | H    | H    | H    | X  | X   | X   | High-Z  | High-Z |
| Byte Access          | H    | L    | H    | L  | H   | L   | High-Z  | Even   |
|                      | H    | H    | L    | H  | H   | L   | High-Z  | Odd    |
| Word Access          | H    | L    | L    | X  | H   | L   | Odd     | Even   |
| Odd Byte Only Access | H    | L    | H    | X  | H   | H   | Odd     | High-Z |

## 6. I/O SPACE DESCRIPTION & OPERATION

### 6.1. I/O Space Input Operations

| Function Mode           | REG#<br>IOW# | CE1#<br>D[15:8] | CE2#<br>D[7:0] | A0 | IOR# |   |        |        |
|-------------------------|--------------|-----------------|----------------|----|------|---|--------|--------|
| Standby                 | X            | H               | H              | X  | X    | X | High-Z | High-Z |
| Byte Access             | L            | L               | H              | L  | L    | H | High-Z | Even   |
|                         | L            | L               | H              | H  | L    | H | High-Z | Odd    |
| Word Access             | L            | L               | L              | L  | L    | H | Odd    | Even   |
| I/O Inhibit             | H            | X               | X              | X  | L    | H | High-Z | High-Z |
| Odd Byte Only<br>Access | L            | H               | L              | X  | L    | H | Odd    | High-Z |

### 6.2. I/O Space Output Operations

| Function Mode           | REG# | CE1# | CE2# | A0 | IOR# | IOWR# | D[15:8] | D[7:0] |
|-------------------------|------|------|------|----|------|-------|---------|--------|
| Standby                 | X    | H    | H    | X  | X    | X     | X       | X      |
| Byte Access             | L    | L    | H    | L  | H    | L     | X       | Even   |
|                         | L    | L    | H    | H  | H    | L     | X       | Odd    |
| Word Access             | L    | L    | L    | L  | H    | L     | Odd     | Even   |
| I/O Inhibit             | H    | X    | X    | X  | H    | L     | X       | X      |
| Odd Byte Only<br>Access | L    | H    | L    | X  | H    | L     | Odd     | X      |

## 7. ATA & TRUE IDE REGISTER DECODING

SiliconDrive PC Cards can be configured as either Memory Mapped or I/O Devices. As noted earlier communication to and from the card is accomplished using the ATA Command Block.

### 7.1. Memory Mapped Register Decoding

In Memory Mapped mode, the cards' registers are accessed via standard memory references (i.e., OE# and WE#). The ATA registers are mapped to common memory space in a 2K byte window starting at address 0.

| Reg# | Offset | A10 | A9:A4 | A3 | A2 | A1 | A0 | OE# = L                  | WE# = L                   |
|------|--------|-----|-------|----|----|----|----|--------------------------|---------------------------|
| 1    | 0      | 0   | X     | 0  | 0  | 0  | 0  | Even Data Read           | Even Data Write           |
| 1    | 1      | 0   | X     | 0  | 0  | 0  | 1  | Error                    | Feature                   |
| 1    | 2      | 0   | X     | 0  | 0  | 1  | 0  | Sector Count             | Sector Count              |
| 1    | 3      | 0   | X     | 0  | 0  | 1  | 1  | Sector Number            | Sector Number             |
| 1    | 4      | 0   | X     | 0  | 1  | 0  | 0  | Cylinder Low             | Cylinder Low              |
| 1    | 5      | 0   | X     | 0  | 1  | 0  | 1  | Cylinder High            | Cylinder High             |
| 1    | 6      | 0   | X     | 0  | 1  | 1  | 0  | Drive/Head               | Drive/Head                |
| 1    | 7      | 0   | X     | 0  | 1  | 1  | 1  | Status                   | Command                   |
| 1    | 8      | 0   | X     | 1  | 0  | 0  | 0  | Duplicate Even Data Read | Duplicate Even Data Write |
| 1    | 9      | 0   | X     | 1  | 0  | 0  | 1  | Duplicate Odd Data Read  | Duplicate Odd Data Write  |
| 1    | D      | 0   | X     | 1  | 1  | 0  | 1  | Duplicate Error          | Duplicate Feature         |
| 1    | E      | 0   | X     | 1  | 1  | 1  | 0  | Alternate Status         | Device Control            |
| 1    | F      | 0   | X     | 1  | 1  | 1  | 1  | Drive Address            | Reserved                  |
| 1    | X      | 1   | X     | X  | X  | X  | 0  | Even Data Read           | Even Data Write           |
| 1    | X      | 1   | X     | X  | X  | X  | 1  | Odd Data Read            | Odd Data Write            |

## 7.2. Independent I/O Mode Register Decoding

Independent I/O Mode, or Contiguous I/O mode requires the host to decode a contiguous block of 16 I/O registers to select the card.

| REG# | Offset | A10 | A9:A4 | A3 | A2 | A1 | A0 | IORD# = L                | IOWR# = L                 |
|------|--------|-----|-------|----|----|----|----|--------------------------|---------------------------|
| 0    | 0      | X   | X     | 0  | 0  | 0  | 0  | Even Data Read           | Even Data Write           |
| 0    | 1      | X   | X     | 0  | 0  | 0  | 1  | Error                    | Feature                   |
| 0    | 2      | X   | X     | 0  | 0  | 1  | 0  | Sector Count             | Sector Count              |
| 0    | 3      | X   | X     | 0  | 0  | 1  | 1  | Sector Number            | Sector Number             |
| 0    | 4      | X   | X     | 0  | 1  | 0  | 0  | Cylinder Low             | Cylinder Low              |
| 0    | 5      | X   | X     | 0  | 1  | 0  | 1  | Cylinder High            | Cylinder High             |
| 0    | 6      | X   | X     | 0  | 1  | 1  | 0  | Drive/Head               | Drive/Head                |
| 0    | 7      | X   | X     | 0  | 1  | 1  | 1  | Status                   | Command                   |
| 0    | 8      | X   | X     | 1  | 0  | 0  | 0  | Duplicate Even Data Read | Duplicate Even Data Write |
| 0    | 9      | X   | X     | 1  | 0  | 0  | 1  | Duplicate Odd Data Read  | Duplicate Odd Data Write  |
| 0    | D      | X   | X     | 1  | 1  | 0  | 1  | Duplicate Error          | Duplicate Feature         |
| 0    | E      | X   | X     | 1  | 1  | 1  | 0  | Alternate Status         | Device Control            |
| 0    | F      | X   | X     | 1  | 1  | 1  | 1  | Drive Address            | Reserved                  |

### 7.3. Primary and Secondary I/O Mapped Register Decoding

| REG# | A10 | A9:A4<br>Primary | A9:A4<br>Secondary | A3 | A2 | A1 | A0 | IORD# = L        | IOWR# = L       |
|------|-----|------------------|--------------------|----|----|----|----|------------------|-----------------|
| 0    | X   | 1Fyh             | 17yh               | 0  | 0  | 0  | 0  | Even Data Read   | Even Data Write |
| 0    | X   | 1Fyh             | 17yh               | 0  | 0  | 0  | 1  | Error            | Feature         |
| 0    | X   | 1Fyh             | 17yh               | 0  | 0  | 1  | 0  | Sector Count     | Sector Count    |
| 0    | X   | 1Fyh             | 17yh               | 0  | 0  | 1  | 1  | Sector Number    | Sector Number   |
| 0    | X   | 1Fyh             | 17yh               | 0  | 1  | 0  | 0  | Cylinder Low     | Cylinder Low    |
| 0    | X   | 1Fyh             | 17yh               | 0  | 1  | 0  | 1  | Cylinder High    | Cylinder High   |
| 0    | X   | 1Fyh             | 17yh               | 0  | 1  | 1  | 0  | Drive/Head       | Drive/Head      |
| 0    | X   | 1Fyh             | 17yh               | 0  | 1  | 1  | 1  | Status           | Command         |
| 0    | X   | 3Fyh             | 37yh               | 0  | 1  | 1  | 0  | Alternate Status | Device Control  |
| 0    | X   | 3Fyh             | 37yh               | 0  | 1  | 1  | 1  | Drive Address    | Reserved        |

### 7.4. Task File Register Specification

The Task File Registers are used for reading and writing the storage data in the SiliconDrive PC Card. The decoded addresses are as shown.

| CS0# | CS1# | DA02 | DA01 | DA00 | DIOR# = L        | DIOW# = L      |
|------|------|------|------|------|------------------|----------------|
| 0    | 1    | 0    | 0    | 0    | Data             | Data           |
| 0    | 1    | 0    | 0    | 1    | Error            | Feature        |
| 0    | 1    | 0    | 1    | 0    | Sector Count     | Sector Count   |
| 0    | 1    | 0    | 1    | 1    | Sector Number    | Sector Number  |
| 0    | 1    | 0    | 1    | 1    | Cylinder Low     | Cylinder Low   |
| 0    | 1    | 1    | 0    | 1    | Cylinder High    | Cylinder High  |
| 0    | 1    | 1    | 1    | 0    | Drive/Head       | Drive/Head     |
| 0    | 1    | 1    | 1    | 1    | Status           | Command        |
| 0    | 0    | X    | X    | X    | Invalid          | Invalid        |
| 1    | 1    | X    | X    | X    | High-Z           | Not Used       |
| 1    | 0    | 0    | X    | X    | High-Z           | Not Used       |
| 1    | 0    | 1    | 0    | X    | High-Z           | Not Used       |
| 1    | 0    | 1    | 1    | 0    | Alternate Status | Device Control |
| 1    | 0    | 1    | 1    | 1    | Device Address   | Not Used       |

## 8. ATA REGISTERS

### 8.1. Data Register

The Data Register is a 16-bit Register used to transfer data blocks between the Host and the Drive buffer. This register may set to 8-bit mode by using the Set Features Command defined in Section 9.1.15.

### 8.2. Error Register

The Error Register contains the error status, if any, generated from the last executed ATA Command. The contents are qualified by the ERR bit being set in the Status Register Section 8.9.

| Operation     | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read          | BBK            | UNC            | MC             | IDNF           | MCR            | ABRT           | TKNOF          | AMNF           |
| Default Value | 0              | 0              | 0              | 0              | 0              | 0              | 0              | 0              |

#### Notes

|                                       |  |
|---------------------------------------|--|
| Bit 7: BBK (Bad Block Detected)       | Set when a Bad Block is detected.                |
| Bit 6: UNC (Uncorrectable Data Error) | Set when Uncorrectable Error is encountered.     |
| Bit 5: MC (Media Changed)             | Set to 0.  |
| Bit 4: IDNF (ID Not Found)            | Set when Sector ID not found.                    |
| Bit 3: MCR (Media Change Request)     | Set to 0.  |
| Bit 2: ABRT (Aborted Command)         | Set when Command Aborted due to drive error.     |
| Bit 1: TKNOF (Track 0 Not Found)      | Set when Executive Drive Diagnostic Command. Bit |
| 0: AMNF (Address mark Not Found)      | Set in case of a general error.                  |

### 8.3. Feature Register

The Feature Register is command specific and is used to enable and disable interface features. This register supports either odd or even byte data transfers only.

| Operation  | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read/Write | Feature Byte   |                |                |                |                |                |                |                |

### 8.4. Sector Count Register

The Sector Count Register is used to read or write the sector count of the data for which an ATA transfer has been made.

| Operation     | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read/Write    | Sector Count   |                |                |                |                |                |                |                |
| Default Value | 0              | 0              | 0              | 0              | 0              | 0              | 0              | 1              |

### 8.5. Sector Number Register

The Sector Number Register is set by the host to specify the starting sector number associated with the next ATA command to be executed. Following a qualified ATA command sequence the device will set the register value to the last sector read or written as a result of the previous AT command.

When LBA mode is implemented and the host issues a command the contents of this register describe the Logical Block Number bits A[7:0]. Following an ATA Command the device will load this register with the LBA block number resulting from the last ATA command.

| Operation     | D <sub>7</sub>                                     | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|--|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read/Write    | Sector Number (CHS Addressing)                     |                |                |                |                |                |                |                |
|               | Logical Block Number bits A07-A00 (LBA Addressing) |                |                |                |                |                |                |                |
| Default Value | 0  | 0              | 0              | 0              | 0              | 0              | 0              | 1              |

## 8.6. Cylinder Low Register

The Cylinder Low Register is set by the host to specify the cylinder number low byte. Following an ATA command, the contents of this register is written by the device, identifying the cylinder number low byte.

In LBA mode, this 8-bit register maintains the contents of the Logical Block number address bits A15:A08.

| Operation     | D <sub>7</sub>                                     | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|--|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read/Write    | Cylinder Number Low Byte (CHS Addressing)          |                |                |                |                |                |                |                |
|               | Logical Block Number bits A15-A08 (LBA Addressing) |                |                |                |                |                |                |                |
| Default Value | 0  | 0              | 0              | 0              | 0              | 0              | 0              | 0              |

## 8.7. Cylinder High Register

The Cylinder High Register is set by the host to specify the cylinder number high byte. Following an ATA command, the contents of this register is set internally by the device, identifying the cylinder number high byte.

In LBA mode, this 8-bit register maintains the contents of the Logical Block number address bits A23:A16.

| Operation     | D <sub>7</sub>                                     | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|--|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read/Write    | Cylinder Number Low Byte (CHS Addressing)          |                |                |                |                |                |                |                |
|               | Logical Block Number bits A23-A16 (LBA Addressing) |                |                |                |                |                |                |                |
| Default Value | 0  | 0              | 0              | 0              | 0              | 0              | 0              | 0              |

## 8.8. Drive/Head Register

The Drive/Head Register is used by the host and the device to select the type of addressing (CHS or LBA), the drive letter, and either bits 3 through 0 of the head number in CHS mode or in LBA mode bits D3:D0 reflect the logical block number bits LBA27:LBA24.

| Operation     | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read/Write    | 1              | LBA            | 1              | DRV            | HS3<br>LBA27   | HS2<br>LBA26   | HS1<br>LBA25   | HS0<br>LBA24   |
| Default Value | 0              | 0              | 0              | 0              | 0              | 0              | 0              | 0              |

The Drive/Head Register is used by the host, to specify one of a pair of ATA drives present in the platform.

### Notes

Bit 6: LBA (Logical Block Addressing)

Selects between CHS (0) and LBA (1) addressing mode.

Bit 7: DRV (Drive Address)

Indicates the drive number selected by the host, either 0 or 1.

Bits 3 - 0: HS3 to 0  
mode.

Indicates bits 3 to 0 of the head number in CHS addressing

or LBA bits 27 thru 24 in LBA mode.

CHS to LBA conversion:

$$LBA = (C \times HpC + H) \times SpH + S - 1$$

LBA to CHS conversion:

$$C = LBA / (HpC \times SpH)$$

$$H = (LBA / SpH) \bmod (HpC)$$

$$S = (LBA \bmod (SpH)) + 1$$

Where:

'C' is the Cylinder Number.

'H' is the Head Number.

'S' is the Sector Count.

'HpC' is the Head count per Cylinder Count.

'SpH' is the Sector count per Head Count (Track).

## 8.9. Status Register

The Status Register provides the device's current status to the host. The status register is an 8-bit read only register. When the contents of this register are read by the host, the IREQ# bit is cleared.

| Operation     | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read/Write    | BSY            | DRDY           | DWF            | DSC            | DRQ            | CORR           | IDX            | ERR            |
| Default Value | 0              | 0              | 0              | 0              | 0              | 0              | 0              | 0              |

### Notes

|                                  |  |
|----------------------------------|--|
| Bit 7: BSY (Busy)                | Set when the drive is busy and unable to process any new ATA commands.                         |
| Bit 6: DRDY (Data Ready)         | Set when the device is ready to accept ATA commands from the host.                             |
| Bit 5: DWF (Drive Write Fault)   | Always set to 0.   |
| Bit 4: DSC (Drive Seek Complete) | Set when the drive heads have been positioned over a specific track.                           |
| Bit 3: DRQ (Data Request)        | Set when device is read to transfer a word or byte of data to or from the host and the device. |
| Bit 2: CORR (Corrected Data)     | Always set to 0.   |
| Bit 1: IDX (Index)               | Always set to 0.   |
| Bit 0: ERR (Error)               | Set when an error occurred during the previous ATA command.                                    |

## 8.10. Command Register

The Command Register specifies the ATA Command code being issued to the drive by the host. Execution of the command begins immediately following the issuance of the command register code by the host.

| Operation  | D <sub>7</sub>   | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|------------|------------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read/Write | ATA Command Code |                |                |                |                |                |                |                |

Refer to Section 9.1. ATA Command Set, for a listing of the supported ATA Commands.

## 8.11. Alternate Status Register

The Alternate Status Register is a read-only register indicating the status of the device, following the previous ATA command. Refer to Section 8.9, Status Register for specific details.

| Operation     | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read/Write    | BSY            | DRDY           | DWF            | DSC            | DRQ            | CORR           | IDX            | ERR            |
| Default Value | 0              | 0              | 0              | 0              | 0              | 0              | 0              | 0              |

## 8.12. Device Control Register

The Device Control Register is used to control the Interrupt Request and issue ATA Software Resets.

| Operation | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Write     | -              | -              | -              | -              | 1              | SRST           | nIEN           | 0              |

### Notes

|                               |  |
|-------------------------------|--|
| Bits 7-4:                     | Reserved bits.   |
| Bit 3:                        | Always set to 1  |
| Bit 2: SRST (Software Reset)  | When set, resets the ATA software.   |
| Bit 1: nIEN(Interrupt Enable) | When set, device interrupts are disabled. No function in Memory Mapped mode. |
| Bit 0:                        | Always set to 0.   |

## 8.13. Device Address Register

The Device Address Register is used to maintain compatibility with ATA disk drive interfaces.

| Operation     | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read/Write    | -              | nWTG           | nHS3           | nHS2           | nHS1           | nHS0           | nDS1           | nDS0           |
| Default Value | 0              | 0              | 1              | 1              | 1              | 1              | 1              | 0              |

### Notes

|                          |  |
|--------------------------|--|
| Bit 7:                   | Reserved bit.  |
| Bit 6: nWTG (Write Gate) | Low when a write to the device is in process.          |
| Bits 5-2: nHS3 to nHS0   | Negated binary address of the currently selected head. |
| Bit 1: nDS1              | Low when Drive 1 is selected and active.               |
| Bit 0: nDS0              | Low when Drive 0 is selected and active.               |

## 9. ATA COMMAND BLOCK & SET DESCRIPTION

In accordance with the ANSI ATA-3 Specification, the device implements seven registers which are used to transfer instructions to the device by the host. These commands follow the ANSI standard ATA protocol, a description of the ATA Command block is provided below.

| Register      | D7 | D6  | D5 | D4    | D3 | D2 | D1 | D0 |
|---------------|----|-----|----|-------|----|----|----|----|
| Feature       | X  |     |    |       |    |    |    |    |
| Sector Count  | X  |     |    |       |    |    |    |    |
| Sector Number | X  |     |    |       |    |    |    |    |
| Cylinder Low  | X  |     |    |       |    |    |    |    |
| Cylinder High | X  |     |    |       |    |    |    |    |
| Drive Head    | 1  | LBA | 1  | Drive | X  |    |    |    |
| Command       | X  |     |    |       |    |    |    |    |

## 9.1. ATA Command Set

| Class | Command Name                | Command Code | Registers Used |    |    |    |    |     |
|-------|-----------------------------|--------------|----------------|----|----|----|----|-----|
|       |                             |              | FR             | SC | SN | CY | DH | LBA |
| 1     | Check Power Mode            | 98h,E5h      |                |    |    |    | D  |     |
| 1     | Execute Drive Diagnostics   | 90h          |                |    |    |    | D  |     |
| 1     | Erase Sector                | C0h          |                | Y  | Y  | Y  | Y  | Y   |
| 2     | Format Track                | 50h          |                | Y  |    | Y  | Y  | Y   |
| 1     | Identify Drive              | ECh          |                |    |    |    | D  |     |
| 1     | Idle                        | 97h,E3h      |                | Y  |    |    | D  |     |
| 1     | Idle Immediate              | 95h,E1h      |                |    |    |    | D  |     |
| 1     | Initialize Drive Parameters | 91h          |                | Y  |    |    | Y  |     |
| 1     | Read Buffer                 | E4h          |                |    |    |    | D  |     |
| 1     | Read DMA                    | C8h          |                | Y  | Y  | Y  | Y  | Y   |
| 1     | Read Multiple               | C4h          |                | Y  | Y  | Y  | Y  | Y   |
| 1     | Read Long Sector            | 22h,23h      |                |    | Y  | Y  | Y  | Y   |
| 1     | Read Sector(s)              | 20h,21h      |                |    | Y  | Y  | Y  | Y   |
| 1     | Read Verify Sector(s)       | 40h,41h      |                | Y  | Y  | Y  | Y  | Y   |
| 1     | Recalibrate                 | 1Xh          |                |    |    |    | Y  |     |
| 1     | Request Sense               | 03h          |                |    |    |    | D  |     |
| 1     | Seek                        | 7Xh          |                |    | Y  | Y  | Y  | Y   |
| 1     | Set Features                | Efh          | Y              |    |    |    | D  |     |
| 1     | Set Multiple Mode           | C6h          |                | Y  |    |    | D  |     |
| 1     | Set Sleep Mode              | 99h,E6h      |                |    |    |    | D  |     |
| 1     | Standby                     | 96h,E2h      |                |    |    |    | D  |     |
| 1     | Standby Immediate           | 94h,E0h      |                |    |    |    | D  |     |
| 1     | Translate Sector            | 87h          |                | Y  | Y  | Y  | Y  | Y   |
| 1     | Wear Level                  | F5h          |                |    |    |    | Y  |     |
| 2     | Write Buffer                | E8h          |                |    |    |    | D  |     |
| 1     | Write DMA                   | CAh          |                | Y  | Y  | Y  | Y  | Y   |
| 2     | Write Long Sector           | 32h,33h      |                |    | Y  | Y  | Y  | Y   |
| 3     | Write Multiple              | C5h          |                | Y  | Y  | Y  | Y  | Y   |
| 3     | Write Multiple w/o Erase    | CDh          |                | Y  | Y  | Y  | Y  | Y   |
| 2     | Write Sector(s)             | 30h,31h      |                | Y  | Y  | Y  | Y  | Y   |
| 2     | Write Sector(s) w/o Erase   | 38h          |                | Y  | Y  | Y  | Y  | Y   |
| 3     | Write Verify                | 3Ch          |                | Y  | Y  | Y  | Y  | Y   |
| -     | NOP                         | FFh          |                |    |    |    |    |     |

**Register Notes:** CY - Cylinder; SC - Sector Count; DH – Drive/Head; SN – Sector Number; FR – Feature LBA – LBA bit of the Drive/Head Register ('D' denotes that only the drive bit is used)

### 9.1.1. Check Power Mode – 98h, E5h

| Register      | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature       | X              |                |                |                |                |                |                |                |
| Sector Count  | X              |                |                |                |                |                |                |                |
| Sector Number | X              |                |                |                |                |                |                |                |
| Cylinder Low  | X              |                |                |                |                |                |                |                |
| Cylinder High | X              |                |                |                |                |                |                |                |
| Drive Head    | X              | X              | X              | Drive          |                |                |                |                |
| Command       | 98h or E5h     |                |                |                |                |                |                |                |

The Check Power Mode command verifies the device's current power mode. When the device is configured for standby mode, or is entering or exiting Standby, the BSY bit will be set and the Sector Count register is set to 00h, then clears the BSY bit. In Idle mode, BSY is set and the Sector Count Register is set to FFh, then the BSY bit is cleared and an interrupt is issued.

### 9.1.2. Executive Drive Diagnostic – 90h

| Register      | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature       | X              |                |                |                |                |                |                |                |
| Sector Count  | X              |                |                |                |                |                |                |                |
| Sector Number | X              |                |                |                |                |                |                |                |
| Cylinder Low  | X              |                |                |                |                |                |                |                |
| Cylinder High | X              |                |                |                |                |                |                |                |
| Drive Head    | X              | X              | X              | Drive          |                |                |                |                |
| Command       | 90h            |                |                |                |                |                |                |                |

The Executive Drive Diagnostic performs an internal read write diagnostic test using (AA55h and 55Aah). If an error is detected in the read/write buffer, the Error Register will report the appropriate Diagnostic Code.

### 9.1.3. Format Track – 50h

| Register      | D <sub>7</sub>           | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub>         | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature       | X                        |                |                |                |                        |                |                |                |
| Sector Count  | Sector Count             |                |                |                |                        |                |                |                |
| Sector Number | Sector Number (LBA7 – 0) |                |                |                |                        |                |                |                |
| Cylinder Low  | Cylinder Low (LBA15-8)   |                |                |                |                        |                |                |                |
| Cylinder High | Cylinder High (LBA23-16) |                |                |                |                        |                |                |                |
| Drive Head    | 1                        | LBA            | 1              | Drive          | Head Number (LBA27-24) |                |                |                |
| Command       | 50h                      |                |                |                |                        |                |                |                |

The Format Track command formats the common solid-state memory array.

### 9.1.4. Identify Drive – ECh

| Register      | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature       | X              |                |                |                |                |                |                |                |
| Sector Count  | X              |                |                |                |                |                |                |                |
| Sector Number | X              |                |                |                |                |                |                |                |
| Cylinder Low  | X              |                |                |                |                |                |                |                |
| Cylinder High | X              |                |                |                |                |                |                |                |
| Drive Head    | X              | X              | X              | Drive          | X              |                |                |                |
| Command       | Ech            |                |                |                |                |                |                |                |

Issued by the host, the Identify Drive command provides 256 bytes of Drive attribute data (i.e., Sector Size, Count, etc.) The Identify Drive data structure is detailed in the preceding table.

### 9.1.4.1. Identify Drive – Drive Attribute Data

| 9.1.4.1 Identify Drive – Drive Attribute Data |   |       |   |
|---|---|-------|---|
| Word Address                                  | Data Default  | Bytes | Data Description  |
| 0   | 044Ah for Fixed ID Bit products (3012, 3021 and others)<br><br>848A for Removable ID Bit products (3038, 3005 and others) | 2     | General Configuration Bit Information<br>15: Non-magnetic Disk<br>14: Formatting Speed Latency Permissible Gap needed<br>13: Track Offset Option supported<br>12: Data Strobe Offset Option supported<br>11: Over 0.5% Rotational Speed Difference<br>10: Disk Transfer Rate > 10Mbps<br>9: 10Mbps >= Disk Transfer Rate > 5Mbps<br>8: 5Mbps >= Disk Transfer Rate<br>7: Removable Cartridge Drive<br>6: Fixed Drive<br>5: Spindle Motor Control Option executed<br>4: Over 15µs Changing Head Time<br>3: Non-MFM Encoding<br>2: Soft Sector Allocation<br>1: Hard Sector Allocation<br>0: Reserved |
| 1   | XXXXh   | 2     | Number of Cylinders   |
| 2   | 0000h   | 2     | Reserved  |
| 3   | 00XXh   | 2     | Number of Heads   |
| 4   | 0000h   | 2     | Number of Unformatted Bytes per Track   |
| 5   | XXXXh   | 2     | Number of Unformatted Bytes per Sector  |
| 6   | XXXXh   | 2     | Number of Sectors per Track   |
| 7 - 8   | XXXXh   | 4     | Number of Sectors per Device  |
| 9   | 0000h   | 2     | Reserved  |
| 10 – 19                                       | XXXXh   | 20    | Serial Number   |
| 20  | 0002h   | 2     | Buffer Type<br>0000h: Not specified<br>0001h: A single ported single sector buffer<br>0002h: A dual ported multi-sector buffer<br>0003h: A dual ported multi-sector buffer with a read caching  |
| 21  | 0002h   | 2     | Buffer Size in 512-byte increments  |
| 22  | 0004h   | 2     | Number of ECC Bytes passed on Read/Write Long Cmds  |
| 23 - 26                                       | XXXXh   | 8     | Firmware Revision (8 ASCII Characters)  |
| 27 - 46                                       | XXXXh   | 40    | Model Number (40 ASCII Characters)  |
| 47  | 0001h   | 2     | 7 – 0: Max Number of Sectors that can be transferred with a Read/Write Multiple Command per Interrupt   |
| 48  | 0000h   | 2     | Double Word (32 bit) not supported  |
| 49  | 0200h   | 2     | 9: LBA supported<br>8: DMA supported  |
| 50  | 0000h   | 2     | Reserved  |
| 51  | 0100h   | 2     | 15 – 8: PIO data transfer cycle timing  |
| 52  | 0000h   | 2     | 15 – 8: DMA data transfer cycle timing  |
| 53  | 0000h   | 2     | 0: Translation Parameters (Word 54 to 58) are valid   |

### 9.1.4.1 Identify Drive – Drive Attribute Data

| Word Address | Data Default | Bytes | Data Description   |
|--------------|--------------|-------|--|
| 54           | XXXXh        | 2     | Current Number of Cylinders  |
| 55           | XXXXh        | 2     | Current Number of Heads  |
| 56           | XXXXh        | 2     | Current Sectors per Track  |
| 57 – 58      | XXXXh        | 4     | Current Capacity in Sectors  |
| 59           | 010Xh        | 2     | 7 – 0: Current Sectors can be transferred with a Read/Write Multiple command per interrupt |
| 60 - 61      | XXXXh        | 4     | Total Number of Sectors addressable in LBA Mode  |
| 62 –127      | 0000h        | 132   | Reserved   |
| 128 – 159    | 0000h        | 64    | Vendor Unique  |
| 160 - 255    | 0000h        | 192   | Reserved   |

### 9.1.5. Idle – 97h, E3h

| Register      | D <sub>7</sub>               | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|------------------------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature       | X                            |                |                |                |                |                |                |                |
| Sector Count  | Timer Count (5ms increments) |                |                |                |                |                |                |                |
| Sector Number | X                            |                |                |                |                |                |                |                |
| Cylinder Low  | X                            |                |                |                |                |                |                |                |
| Cylinder High | X                            |                |                |                |                |                |                |                |
| Drive Head    | X                            | X              | X              | Drive          | X              |                |                |                |
| Command       | 97h or E3h                   |                |                |                |                |                |                |                |

When issued by the host, the device's internal controller sets the BSY bit, enters the Idle mode, clears the BSY bit, and generates an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power-down mode is enabled. If the sector count is zero, the automatic power-down mode is disabled.

### 9.1.6. Idle Immediate – 95h, E1h

| Register      | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature       | X              |                |                |                |                |                |                |                |
| Sector Count  | X              |                |                |                |                |                |                |                |
| Sector Number | X              |                |                |                |                |                |                |                |
| Cylinder Low  | X              |                |                |                |                |                |                |                |
| Cylinder High | X              |                |                |                |                |                |                |                |
| Drive Head    | X              | X              | X              | Drive          | X              |                |                |                |
| Command       | 95h or E1h     |                |                |                |                |                |                |                |

When issued by the host the device's internal controller sets the BSY bit, enters Idle Mode, clears the BSY bit, and issues an interrupt. The interrupt is issued whether or not the Idle mode is fully entered.

### 9.1.7. Initialize Drive Parameters – 91h

| Register      | D <sub>7</sub>                   | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub>                       | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|----------------------------------|----------------|----------------|----------------|--------------------------------------|----------------|----------------|----------------|
| Feature       | X                                |                |                |                |                                      |                |                |                |
| Sector Count  | Sector Count (Number of Sectors) |                |                |                |                                      |                |                |                |
| Sector Number | X                                |                |                |                |                                      |                |                |                |
| Cylinder Low  | X                                |                |                |                |                                      |                |                |                |
| Cylinder High | X                                |                |                |                |                                      |                |                |                |
| Drive Head    | X                                | 0              | X              | Drive          | Head Number<br>(Number of Heads – 1) |                |                |                |
| Command       | 91h                              |                |                |                |                                      |                |                |                |

Initialize Drive Parameters allows the host to set the sector counts per track and the head counts per cylinder to "1" fixed. Upon issuance of the command the device will set the BSY bit and associated parameters, clears the BSY bit and issues an interrupt.

### 9.1.8. Recalibrate – 1Xh

| Register      | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature       | X              |                |                |                |                |                |                |                |
| Sector Count  | X              |                |                |                |                |                |                |                |
| Sector Number | X              |                |                |                |                |                |                |                |
| Cylinder Low  | X              |                |                |                |                |                |                |                |
| Cylinder High | X              |                |                |                |                |                |                |                |
| Drive Head    | 1              | LBA            | 1              | Drive          | X              |                |                |                |
| Command       | 1Xh            |                |                |                |                |                |                |                |

The Recalibrate command sets the Cylinder Low & High, and the Head Number to “0h”, and Sector Number to “1h” in CHS mode. In LBA mode (i.e., LBA = 1) the Sector Number is set to “0h”.

### 9.1.9. Read Buffer – E4h

| Register      | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature       | X              |                |                |                |                |                |                |                |
| Sector Count  | X              |                |                |                |                |                |                |                |
| Sector Number | X              |                |                |                |                |                |                |                |
| Cylinder Low  | X              |                |                |                |                |                |                |                |
| Cylinder High | X              |                |                |                |                |                |                |                |
| Drive Head    | X              | X              | X              | Drive          | X              |                |                |                |
| Command       | E4h            |                |                |                |                |                |                |                |

This command allows the host to read the contents of the sector buffer. When issued the device sets the BSY bit and sets up the sector buffer data in preparation for the read operation. Once the data is ready, the DRQ bit is set and the BSY bit in the status register are set and cleared, respectively.

### 9.1.10. Read DMA – C8h

| Register      | D <sub>7</sub>           | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub>         | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature       | X                        |                |                |                |                        |                |                |                |
| Sector Count  | Sector Count             |                |                |                |                        |                |                |                |
| Sector Number | Sector Number (LBA7-0)   |                |                |                |                        |                |                |                |
| Cylinder Low  | Cylinder Low (LBA15-8)   |                |                |                |                        |                |                |                |
| Cylinder High | Cylinder High (LBA23-16) |                |                |                |                        |                |                |                |
| Drive Head    | 1                        | LBA            | 1              | Drive          | Head Number (LBA27-24) |                |                |                |
| Command       | C8h                      |                |                |                |                        |                |                |                |

This command allows the host to read data using the DMA transfer protocol.

### 9.1.11. Read Multiple – C4h

| Register      | D <sub>7</sub>           | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub>         | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature       | X                        |                |                |                |                        |                |                |                |
| Sector Count  | Sector Count             |                |                |                |                        |                |                |                |
| Sector Number | Sector Number (LBA7-0)   |                |                |                |                        |                |                |                |
| Cylinder Low  | Cylinder Low (LBA15-8)   |                |                |                |                        |                |                |                |
| Cylinder High | Cylinder High (LBA23-16) |                |                |                |                        |                |                |                |
| Drive Head    | 1                        | LBA            | 1              | Drive          | Head Number (LBA27-24) |                |                |                |
| Command       | C4h                      |                |                |                |                        |                |                |                |

This command executes similarly to the Read Sector command with the exception that, interrupts are issued only when a block containing the counts of sectors defined by the Set Multiple command is transferred.

### 9.1.12. Read Sector – 20h, 21h

| Register      | D <sub>7</sub>           | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub>         | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature       | X                        |                |                |                |                        |                |                |                |
| Sector Count  | Sector Count             |                |                |                |                        |                |                |                |
| Sector Number | Sector Number (LBA7-0)   |                |                |                |                        |                |                |                |
| Cylinder Low  | Cylinder Low (LBA15-8)   |                |                |                |                        |                |                |                |
| Cylinder High | Cylinder High (LBA23-16) |                |                |                |                        |                |                |                |
| Drive Head    | 1                        | LBA            | 1              | Drive          | Head Number (LBA27-24) |                |                |                |
| Command       | 20h or 21h               |                |                |                |                        |                |                |                |

The Read Sector command allows the host to read sectors 1 to 256 as specified in the Sector Count Register. If the Sector count is set to "0h", all 256 Sectors of data will be made available. Once the command code is issued and the first sector of data has been transferred to the buffer the DRQ bit will be set. The Read Sector command is terminated by writing the cylinder, head, and sector number of the last sector read in the task file. On error, the read operation is aborted in the errant sector.

### 9.1.13. Read Long Sector(s) – 22h, 23h

| Register      | D <sub>7</sub>           | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub>         | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature       | X                        |                |                |                |                        |                |                |                |
| Sector Count  | X                        |                |                |                |                        |                |                |                |
| Sector Number | Sector Number (LBA7-0)   |                |                |                |                        |                |                |                |
| Cylinder Low  | Cylinder Low (LBA15-8)   |                |                |                |                        |                |                |                |
| Cylinder High | Cylinder High (LBA23-16) |                |                |                |                        |                |                |                |
| Drive Head    | 1                        | LBA            | 1              | Drive          | Head Number (LBA27-24) |                |                |                |
| Command       | 22h or 23h               |                |                |                |                        |                |                |                |

The Read Long Sector(s) command operates similarly to the Read Sector(s) command, with the exception that it transfers requested data sectors and ECC data. The long instruction ECC byte transfer for Long commands is a byte transfer at a fixed length of 4 bytes.

**9.1.14. Read Verify Sector(s) – 40h, 41h**

| Register      | D7                       | D6  | D5 | D4    | D3                     | D2 | D1 | D0 |
|---------------|--------------------------|-----|----|-------|------------------------|----|----|----|
| Feature       | X                        |     |    |       |                        |    |    |    |
| Sector Count  | Sector Count             |     |    |       |                        |    |    |    |
| Sector Number | Sector Number (LBA7-0)   |     |    |       |                        |    |    |    |
| Cylinder Low  | Cylinder Low (LBA15-8)   |     |    |       |                        |    |    |    |
| Cylinder High | Cylinder High (LBA23-16) |     |    |       |                        |    |    |    |
| Drive Head    | 1                        | LBA | 1  | Drive | Head Number (LBA27-24) |    |    |    |
| Command       | 40h or 41h               |     |    |       |                        |    |    |    |

The Read Verify Sector(s) command operates similarly to the Read Sector(s) command, with the exception that it does not set the DRQ bit and does not transfer data to the host. Once the requested sectors have been verified, the onboard controller clears the BSY bit and issues an interrupt.

### 9.1.15. Seek – 7Xh

| Register      | D <sub>7</sub>           | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub>         | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature       | X                        |                |                |                |                        |                |                |                |
| Sector Count  | X                        |                |                |                |                        |                |                |                |
| Sector Number | Sector Number (LBA7-0)   |                |                |                |                        |                |                |                |
| Cylinder Low  | Cylinder Low (LBA15-8)   |                |                |                |                        |                |                |                |
| Cylinder High | Cylinder High (LBA23-16) |                |                |                |                        |                |                |                |
| Drive Head    | 1                        | LBA            | 1              | Drive          | Head Number (LBA27-24) |                |                |                |
| Command       | 7Xh                      |                |                |                |                        |                |                |                |

The Seek command seeks and picks up the head to tracks specified in the task file. When the command is issued, the Solid-state memory chips need not be formatted. After an appropriate amount of time the DSC bit is set.

### 9.1.16. Set Features – EFh

| Register      | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature       | Feature        |                |                |                |                |                |                |                |
| Sector Count  | X              |                |                |                |                |                |                |                |
| Sector Number | X              |                |                |                |                |                |                |                |
| Cylinder Low  | X              |                |                |                |                |                |                |                |
| Cylinder High | X              |                |                |                |                |                |                |                |
| Drive Head    | X              | X              | X              | Drive          | X              |                |                |                |
| Command       | EFh            |                |                |                |                |                |                |                |

### 9.1.16. Set Features – EFh (*continued*)

This command allows the host to configure the Feature Set of the device according to the attributes listed below.

| Feature | Operation   |
|---------|---|
| 01h     | Enable 8 bit Data Transfer                        |
| 66h     | Disable Reverting to Power On Defaults            |
| 81h     | Disable 8 bit Data Transfer                       |
| BBh     | 4 Bytes of Data Apply on Read/Write Long Commands |
| CCh     | Enable revert to Power on Defaults                |

On Power-up or following a Hardware Reset, the device will be set to the default mode “81h”.

### 9.1.17. Set Multiple Mode – C6h

| Register      | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature       | X              |                |                |                |                |                |                |                |
| Sector Count  | Sector Count   |                |                |                |                |                |                |                |
| Sector Number | X              |                |                |                |                |                |                |                |
| Cylinder Low  | X              |                |                |                |                |                |                |                |
| Cylinder High | X              |                |                |                |                |                |                |                |
| Drive Head    | X              | X              | X              | Drive          | X              |                |                |                |
| Command       | C6h            |                |                |                |                |                |                |                |

The Set Multiple Mode command allows the host to access the drive via Read Multiple and Write Multiple ATA commands. Additionally, the command sets the block count (i.e., the number of sectors within the block) for the Read/Write Multiple command. The sector count per block is set in the Sector Count register.

### 9.1.18. Set Sleep Mode – 99h, E6h

| Register      | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature       | X              |                |                |                |                |                |                |                |
| Sector Count  | X              |                |                |                |                |                |                |                |
| Sector Number | X              |                |                |                |                |                |                |                |
| Cylinder Low  | X              |                |                |                |                |                |                |                |
| Cylinder High | X              |                |                |                |                |                |                |                |
| Drive Head    | X              | X              | X              | Drive          | X              |                |                |                |
| Command       | 99h or E6h     |                |                |                |                |                |                |                |

The Set Sleep Mode command allows the host to set the device in Sleep mode. When the onboard controller transitions to Sleep mode, it clears the BSY bit and issues an interrupt, and the device interface becomes inactive. Sleep mode can be exited by issuing either a hardware or software reset.

### 9.1.19. Standby – 96h, E2h

| Register      | D <sub>7</sub>                   | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|----------------------------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature       | X                                |                |                |                |                |                |                |                |
| Sector Count  | Timer Count(5msec x Timer Count) |                |                |                |                |                |                |                |
| Sector Number | X                                |                |                |                |                |                |                |                |
| Cylinder Low  | X                                |                |                |                |                |                |                |                |
| Cylinder High | X                                |                |                |                |                |                |                |                |
| Drive Head    | X                                | X              | X              | Drive          | X              |                |                |                |
| Command       | 96h or E2h                       |                |                |                |                |                |                |                |

The Standby command, when issued by the host will transition the device into the Standby mode. If the Sector Count Register is set to a value other than “0h”, the Auto Power Down function is enabled and the device will return to Idle mode.

### 9.1.20. Standby Immediate – 94h, E0h

| Register      | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature       | X              |                |                |                |                |                |                |                |
| Sector Count  | X              |                |                |                |                |                |                |                |
| Sector Number | X              |                |                |                |                |                |                |                |
| Cylinder Low  | X              |                |                |                |                |                |                |                |
| Cylinder High | X              |                |                |                |                |                |                |                |
| Drive Head    | X              | X              | X              | Drive          | X              |                |                |                |
| Command       | 94h or E0h     |                |                |                |                |                |                |                |

The Standby Immediate command, when issued by the host will transition the device into the Standby mode.

### 9.1.21. Write Buffer – E8h

| Register      | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature       | X              |                |                |                |                |                |                |                |
| Sector Count  | X              |                |                |                |                |                |                |                |
| Sector Number | X              |                |                |                |                |                |                |                |
| Cylinder Low  | X              |                |                |                |                |                |                |                |
| Cylinder High | X              |                |                |                |                |                |                |                |
| Drive Head    | X              | X              | X              | Drive          | X              |                |                |                |
| Command       | E8h            |                |                |                |                |                |                |                |

The Write Buffer command allows the host to rewrite the contents of the 512 byte data buffer with the desired data.

### 9.1.22. Write DMA – CAh

| Register      | D <sub>7</sub>          | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub>        | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|-------------------------|----------------|----------------|----------------|-----------------------|----------------|----------------|----------------|
| Feature       | X                       |                |                |                |                       |                |                |                |
| Sector Count  | Sector Count            |                |                |                |                       |                |                |                |
| Sector Number | Sector Number (LBA7-0)  |                |                |                |                       |                |                |                |
| Cylinder Low  | Cylinder Low(LBA15-8)   |                |                |                |                       |                |                |                |
| Cylinder High | Cylinder High(LBA23-16) |                |                |                |                       |                |                |                |
| Drive Head    | X                       | LBA            | X              | Drive          | Head Number(LBA27-24) |                |                |                |
| Command       | CAh                     |                |                |                |                       |                |                |                |

The Write DMA command allows the host to write data using the DMA transfer protocol.

### 9.1.23. Write Multiple – C5h

| Register      | D <sub>7</sub>          | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub>        | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|-------------------------|----------------|----------------|----------------|-----------------------|----------------|----------------|----------------|
| Feature       | X                       |                |                |                |                       |                |                |                |
| Sector Count  | Sector Count            |                |                |                |                       |                |                |                |
| Sector Number | Sector Number (LBA7-0)  |                |                |                |                       |                |                |                |
| Cylinder Low  | Cylinder Low(LBA15-8)   |                |                |                |                       |                |                |                |
| Cylinder High | Cylinder High(LBA23-16) |                |                |                |                       |                |                |                |
| Drive Head    | X                       | LBA            | X              | Drive          | Head Number(LBA27-24) |                |                |                |
| Command       | C5h                     |                |                |                |                       |                |                |                |

The Write Multiple command operates in the same manner as the Write Sector command, when issued the device will set the BSY bit within 400nsec, an interrupt is generated at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

### 9.1.24. Write Sector(s) – 30h, 31h

| Register      | D <sub>7</sub>           | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub>         | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature       | X                        |                |                |                |                        |                |                |                |
| Sector Count  | Sector Count             |                |                |                |                        |                |                |                |
| Sector Number | Sector Number (LBA7-0)   |                |                |                |                        |                |                |                |
| Cylinder Low  | Cylinder Low (LBA15-8)   |                |                |                |                        |                |                |                |
| Cylinder High | Cylinder High (LBA23-16) |                |                |                |                        |                |                |                |
| Drive Head    | X                        | LBA            | X              | Drive          | Head Number (LBA27-24) |                |                |                |
| Command       | 30h or 31h               |                |                |                |                        |                |                |                |

The Write Sector(s) command writes from 1 to 256 sectors as specified in the Sector Count Register. A Sector count of 0 requests 256 Sectors. When issued the device will set the BSY bit within 400nsec, an interrupt is generated at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

### 9.1.25. Write Long Sector(s) – 32h, 33h

| Register      | D <sub>7</sub>           | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub>         | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature       | X                        |                |                |                |                        |                |                |                |
| Sector Count  | Sector Count             |                |                |                |                        |                |                |                |
| Sector Number | Sector Number (LBA7-0)   |                |                |                |                        |                |                |                |
| Cylinder Low  | Cylinder Low (LBA15-8)   |                |                |                |                        |                |                |                |
| Cylinder High | Cylinder High (LBA23-16) |                |                |                |                        |                |                |                |
| Drive Head    | X                        | LBA            | X              | Drive          | Head Number (LBA27-24) |                |                |                |
| Command       | 32h or 33h               |                |                |                |                        |                |                |                |

The Write Long Sector(s) command operates in the same manner as the Write Sector command, when issued the device will set the BSY bit within 400nsec, an interrupt is generated at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

### 9.1.26. Erase Sector(s) – C0h

| Register      | D <sub>7</sub>           | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub>         | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature       | X                        |                |                |                |                        |                |                |                |
| Sector Count  | Sector Count             |                |                |                |                        |                |                |                |
| Sector Number | Sector Number (LBA7-0)   |                |                |                |                        |                |                |                |
| Cylinder Low  | Cylinder Low (LBA15-8)   |                |                |                |                        |                |                |                |
| Cylinder High | Cylinder High (LBA23-16) |                |                |                |                        |                |                |                |
| Drive Head    | X                        | LBA            | X              | Drive          | Head Number (LBA27-24) |                |                |                |
| Command       | C0h                      |                |                |                |                        |                |                |                |

The Erase Sector(s) command is issued prior to the issuance of a Write Sector(s) or Write Multiple w/o Erase command.

## 9.1.27. Request Sense – 03h

| Register      | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature       | X              |                |                |                |                |                |                |                |
| Sector Count  | X              |                |                |                |                |                |                |                |
| Sector Number | X              |                |                |                |                |                |                |                |
| Cylinder Low  | X              |                |                |                |                |                |                |                |
| Cylinder High | X              |                |                |                |                |                |                |                |
| Drive Head    | 1              | X              | 1              | Drive          | X              |                |                |                |
| Command       | 03h            |                |                |                |                |                |                |                |

The Request Sense command identifies the Extended Error Codes generated by the preceding ATA command. The Request Sense command must be issued immediately following the detection of an error via the Error Register.

| Extended Error Codes    | Description  |
|-------------------------|--|
| 00h                     | No Error Detected                                  |
| 01h                     | Self Test OK (No Error)                            |
| 09h                     | Miscellaneous Error                                |
| 20h                     | Invalid Command                                    |
| 21h                     | Invalid Address (Requested Head or Sector Invalid) |
| 2Fh                     | Address Overflow (Address Too Large)               |
| 35h, 36h                | Supply or Generated Voltage Out of Tolerance       |
| 11h                     | Uncorrectable ECC Error                            |
| 18h                     | Corrected ECC Error                                |
| 05h, 30h-32h, 37h, 3Eh  | Self Test of Diagnostic Failed                     |
| 10h, 14h                | ID Not Found                                       |
| 3Ah                     | Spare Sectors Exhausted                            |
| 1Fh                     | Data Transfer Error/ Aborted Command               |
| 0Ch, 38h, 3Bh, 3Ch, 3Fh | Computed Media Format                              |
| 03h                     | Write/Erase Failed                                 |

### 9.1.28. Translate Sector – 87h

| Register      | D <sub>7</sub>           | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub>         | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature       | X                        |                |                |                |                        |                |                |                |
| Sector Count  | Sector Count             |                |                |                |                        |                |                |                |
| Sector Number | Sector Number (LBA7-0)   |                |                |                |                        |                |                |                |
| Cylinder Low  | Cylinder Low (LBA15-8)   |                |                |                |                        |                |                |                |
| Cylinder High | Cylinder High (LBA23-16) |                |                |                |                        |                |                |                |
| Drive Head    | 1                        | LBA            | 1              | Drive          | Head Number (LBA27-24) |                |                |                |
| Command       | 87h                      |                |                |                |                        |                |                |                |

The Translate Sector command is not currently supported by the SiliconSystems SiliconDrive PC Card. If the host issues this command the device will respond with 0x00h in the data register.

### 9.1.29. Wear Level – F5h

| Register      | D <sub>7</sub>    | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|-------------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature       | X                 |                |                |                |                |                |                |                |
| Sector Count  | Completion Status |                |                |                |                |                |                |                |
| Sector Number | X                 |                |                |                |                |                |                |                |
| Cylinder Low  | X                 |                |                |                |                |                |                |                |
| Cylinder High | X                 |                |                |                |                |                |                |                |
| Drive Head    | X                 | X              | X              | Drive          | Flag           |                |                |                |
| Command       | F5h               |                |                |                |                |                |                |                |

The Wear Level command is supported as a NOP command for the purposes of backward compatibility with the ANSI AT Attachment Standard. This command sets the Sector Count Register to 0x00h after processing this command.

### 9.1.30. Write Multiple w/o Erase – CDh

| Register      | D <sub>7</sub>           | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub>         | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature       | X                        |                |                |                |                        |                |                |                |
| Sector Count  | Sector Count             |                |                |                |                        |                |                |                |
| Sector Number | Sector Number (LBA7-0)   |                |                |                |                        |                |                |                |
| Cylinder Low  | Cylinder Low (LBA15-8)   |                |                |                |                        |                |                |                |
| Cylinder High | Cylinder High (LBA23-16) |                |                |                |                        |                |                |                |
| Drive Head    | X                        | LBA            | X              | Drive          | Head Number (LBA27-24) |                |                |                |
| Command       | CDh                      |                |                |                |                        |                |                |                |

The Write Multiple w/o Erase command functions identically to the Write Multiple command with the exception that the implied pre-erase (i.e., Erase Sector(s) Command) is not issued prior to writing the sectors.

### 9.1.31. Write Sector(s) w/o Erase – 38h

| Register      | D <sub>7</sub>           | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub>         | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature       | X                        |                |                |                |                        |                |                |                |
| Sector Count  | Sector Count             |                |                |                |                        |                |                |                |
| Sector Number | Sector Number (LBA7-0)   |                |                |                |                        |                |                |                |
| Cylinder Low  | Cylinder Low (LBA15-8)   |                |                |                |                        |                |                |                |
| Cylinder High | Cylinder High (LBA23-16) |                |                |                |                        |                |                |                |
| Drive Head    | X                        | LBA            | X              | Drive          | Head Number (LBA27-24) |                |                |                |
| Command       | 38h                      |                |                |                |                        |                |                |                |

The Write Sector(s) w/o Erase command functions similar to the Write Sector command, however the implied pre-erase (i.e., Erase Sector(s) Command) is not issued prior to writing the sectors.

### 9.1.32. Write Verify – 3Ch

| Register      | D <sub>7</sub>           | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub>         | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature       | X                        |                |                |                |                        |                |                |                |
| Sector Count  | Sector Count             |                |                |                |                        |                |                |                |
| Sector Number | Sector Number (LBA7-0)   |                |                |                |                        |                |                |                |
| Cylinder Low  | Cylinder Low (LBA15-8)   |                |                |                |                        |                |                |                |
| Cylinder High | Cylinder High (LBA23-16) |                |                |                |                        |                |                |                |
| Drive Head    | X                        | LBA            | X              | Drive          | Head Number (LBA27-24) |                |                |                |
| Command       | 3Ch                      |                |                |                |                        |                |                |                |

The Write Verify command verifies each sector immediately after it is written. This command performs identically to the Write Sector(s) command with the added feature of verifying each sector written.

## 10. SALES AND SUPPORT

To order or to obtain information on pricing and delivery, please contact your SiliconSystems Sales Representative.

### 10.1. Part Numbering Nomenclature

The following table defines the SiliconDrive PC Card part numbering scheme:

| Definition   |   |     |   |  |  |  |
|--|---|-----|---|--|--|--|
| SSD-   | P | YYY | T | -XXXX  |  |  |
|  |   |     |   | <i>SiliconSystems Proprietary</i>                  |  |  |
|  |   |     |   | <i>Temp. Range: Blank=Commercial, I=Industrial</i> |  |  |
|  |   |     |   | <i>Capacity: 08G=8GB / 128=12M</i>                 |  |  |
|  |   |     |   | <i>Form Factor: P = PC Card</i>                    |  |  |
| <i>SiliconSystems SiliconDrive</i>   |   |     |   |  |  |  |
| <i>Operating Temperature Range: Commercial: 0°C to 70°C, Industrial: -40°C to +85°C</i>  |   |     |   |  |  |  |
| <i>Note: XXXX = 3012 for SiliconDrive PC Card with fixed ID bit and DMA support; XXXX = 3021 for fixed ID bit and DMA disabled; XXXX = 3038 for removable ID bit and DMA support; XXXX = 3005 for removable ID bit and DMA disabled. Other configurations are available. Please contact your SiliconSystems Sales Representative for more details.</i> |   |     |   |  |  |  |

| Part Number   | Description                                 |
|---------------|---|
| SSD-P08G-xxxx | 8GB SiliconDrive PC Card, Commercial Temp   |
| SSD-P06G-xxxx | 6GB SiliconDrive PC Card, Commercial Temp   |
| SSD-P04G-xxxx | 4GB SiliconDrive PC Card, Commercial Temp   |
| SSD-P02G-xxxx | 2GB SiliconDrive PC Card, Commercial Temp   |
| SSD-P01G-xxxx | 1GB SiliconDrive PC Card, Commercial Temp   |
| SSD-P51M-xxxx | 512MB SiliconDrive PC Card, Commercial Temp |
| SSD-P25M-xxxx | 256MB SiliconDrive PC Card, Commercial Temp |
| SSD-P12M-xxxx | 128MB SiliconDrive PC Card, Commercial Temp |

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