

**PCMCIA 2.1 Compliant FLASH Memory Cards - 1 to 10 Megabyte
Card Features AMD 4Mbit Devices for 5 Volts Only Operation (AMD's "C-Series" equivalent)**

Description

These SMART Modular products are high quality PCMCIA 2.1 compliant Type I FLASH memory cards which operate in a 5 Volt only environment. These cards feature an array of 2 to 20 AMD® Am29F040 4 Megabit FLASH components which are packaged in a quality PCMCIA housing by our ISO 9001 certified production team. These cards are compatible with AMC00XCFLKA, "C-Series" cards from AMD. FLASH technology assures data retention without the need for battery back-up of any kind, even when system power is removed.

These products offer memory capacities of between 1 to 10 Megabytes with a 64 Kbyte block erase resolution. Memory blocks that are not busy with program/erase operations, may be accessed by both read and write commands without concern for on going operations in other blocks. Additionally data may be handled in either 8 bit or 16 bit bus modes.

These features make SMART Modular memory cards especially desirable for a wide variety of custom applications that utilize PCMCIA slots such as PDAs and other handheld devices.

Features

- PCMCIA 2.1 compliant
- FLASH Architecture, non volatile memory
- Single Supply Voltage Operation (5V ±5%)
- Standard 150 and 200ns Access Time from Standby
- Byte-wide and Word-wide access
- Embedded Program/Erase Algorithms
- Erase Suspend/Resume Feature
- 64 Kilobyte Sector Erase Resolution
- High Write Endurance
1,000,000 Write/Erase Cycles Min per sector
- WP Switch to Prevent Accidental Data Loss
- Dedicated Attribute Memory EE PROM
- Extremely Low Power Consumption
- ISO 9001 Quality Controls

PIN DESCRIPTION

Signal	Name	Function
A[25:0]	Address Bus	Address Inputs, A25-A0
D[15:0]	Data Bus	Data Input/Outputs
/OE	Output Enable	Active Low for Read
/WE	Write Enable	Active Low for Write
/CE1	Card Enable Low Byte	Active Low for Read/ Write Even Byte
/CE2	Card Enable High Byte	Active Low for Read/ Write Odd Byte
/REG	Register Select	Active Low to enables Attribute Memory
WP	Write Protect	Output Signal indicates the WP switch state
/VS1, /VS2	Voltage Sense 1, 2	Voltage Sense Outputs (both open = 5V card)
/CD1, /CD2	Card Detect Signals 1, 2	Tied to GND
V _{CC}	Power Supply	Power Supply Voltage, +5.0V ±5%
GND (V _{SS})	Ground	Card Ground

PIN ASSIGNMENTS

Pin #	Signal	I/O	Function		Pin #	Signal	I/O	Function	
1	GND		Ground		35	GND		Ground	
2	D3	I/O	Data Bit 3	PL	36	/CD1	O	Card Detect - Grounded	
3	D4	I/O	Data Bit 4	PL	37	D11	I/O	Data Bit 11	PL
4	D5	I/O	Data Bit 5	PL	38	D12	I/O	Data Bit 12	PL
5	D6	I/O	Data Bit 6	PL	39	D13	I/O	Data Bit 13	PL
6	D7	I/O	Data Bit 7	PL	40	D14	I/O	Data Bit 14	PL
7	/CE1	I	Card Enable Low byte	PH	41	D15	I/O	Data Bit 15	PL
8	A10	I	Address Bit 10		42	/CE2	I	Card Enable High byte	PH
9	/OE	I	Output Enable	PH	43	/VS1		Vltg Sense Signal 1- Open	
10	A11	I	Address Bit 11		44	<i>RFU</i>		<i>Reserved For Future Use</i>	NC
11	A9	I	Address Bit 9		45	<i>RFU</i>		<i>Reserved For Future Use</i>	NC
12	A8	I	Address Bit 8		46	A17	I	Address Bit 17	
13	A13	I	Address Bit 13		47	A18	I	Address Bit 18	
14	A14	I	Address Bit 14		48	A19	I	Address Bit 19	
15	/WE	I	Write Enable	PH	49	A20	I	Address Bit 20 (Note 1)	PL
16	/BUSY	O	Ready Busy Signal	NC	50	A21	I	Address Bit 21 (Note 2)	PL
17	V _{cc}		Power Supply		51	V _{cc}		Power Supply	
18	V _{pp1}		<i>Program Voltage 1</i>	NC	52	V _{pp2}		<i>Program Voltage 2</i>	NC
19	A16	I	Address Bit 16		53	A22	I	Address Bit 22 (Note 3)	PL
20	A15	I	Address Bit 15		54	A23	I	Address Bit 23	NC
21	A12	I	Address Bit 12		55	A24	I	Address Bit 24	NC
22	A7	I	Address Bit 7		56	A25	I	Address Bit 25	NC
23	A6	I	Address Bit 6		57	/VS2		Vltg Sense Signal 2- Open	
24	A5	I	Address Bit 5		58	RESET	I	Hardware RESET	NC
25	A4	I	Address Bit 4		59	WAIT	O	Wait State Control (Note 4)	NC
26	A3	I	Address Bit 3		60	<i>RFU</i>		<i>Reserved For Future Use</i>	NC
27	A2	I	Address Bit 2		61	/REG	I	Register Select	PH
28	A1	I	Address Bit 1		62	/BVD2	O	Batt. Voltage Detect 2	PH
29	A0	I	Address Bit 0	PL	63	/BVD1	O	Batt. Voltage Detect 1	PH
30	D0	I/O	Data Bit 0	PL	64	D8	I/O	Data Bit 8	PL
31	D1	I/O	Data Bit 1	PL	65	D9	I/O	Data Bit 9	PL
32	D2	I/O	Data Bit 2	PL	66	D10	I/O	Data Bit 10	PL
33	WP	O	Write Protect		67	/CD2	O	Card Detect - Grounded	
34	GND		Ground		68	GND		Ground	

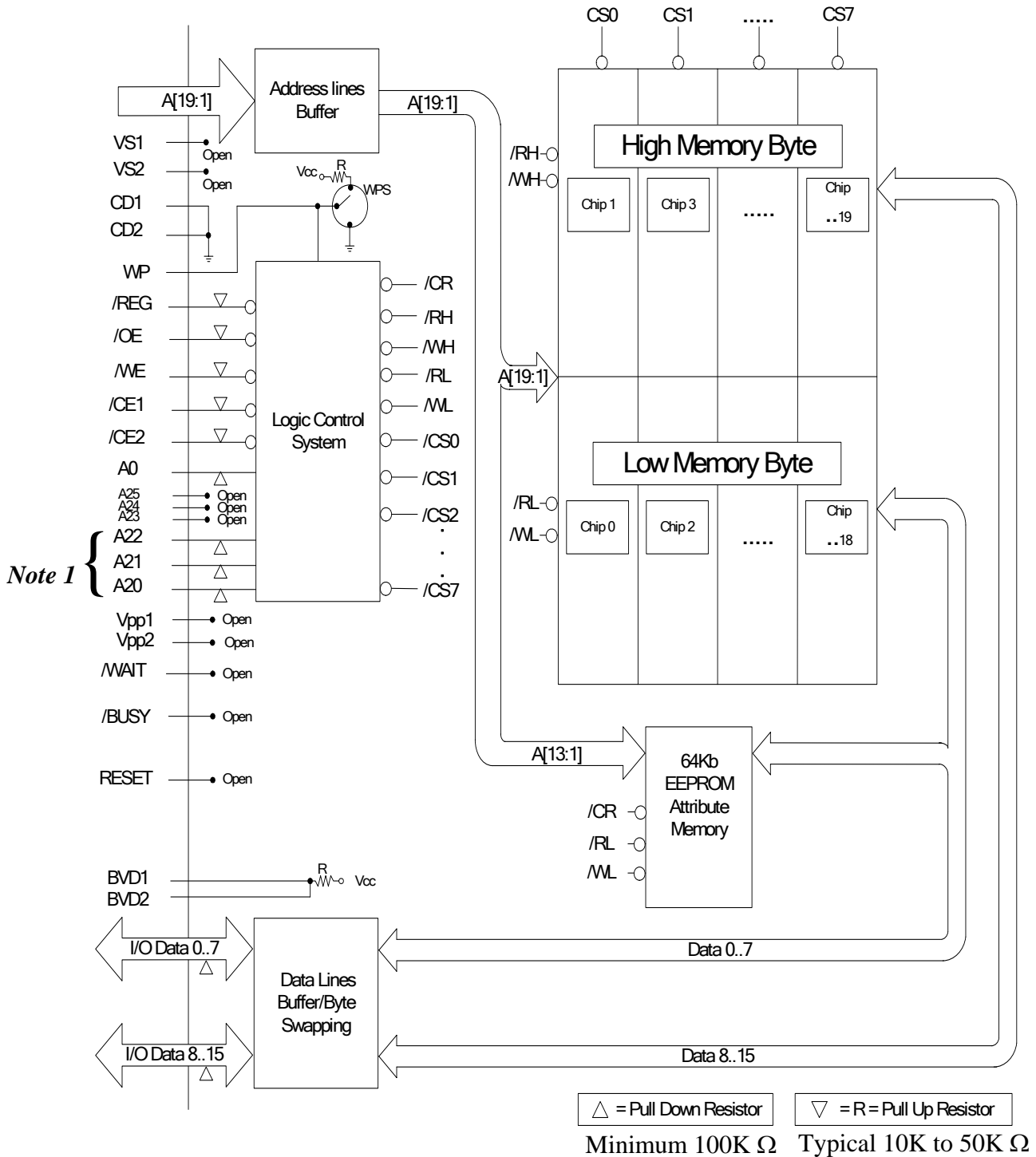
Notes :

1. This address bit is MSB for 2MB cards.
Higher order address bits are NC for cards with "address wrap"
2. This address bit is MSB for 4MB cards.
Higher order address bits are NC for cards with "address wrap"
3. This address bit is MSB for 8MB cards.
Higher order address bits are NC for cards with "address wrap".
4. There are not wait states generated by these cards. This Signal must be pulled by the Host socket.

Legend:

- I = Input to card only
 - O = Output from card only
 - I/O = Bi-directional signal
 - PH = Pulled High (10 - 50K Typ.)
 - PL = Pulled Low (100K Min.)
 - NC = Not Connected
- Functions of the shaded pins are not used.

FUNCTIONAL BLOCK DIAGRAM



Note:
 1. See Notes 1, 2 and 3 under Pin Assignment regarding utilized address lines.

COMMON MEMORY BUS OPERATIONS

Operation	/REG	/CE2	/CE1	/OE	/WE	A0	D8-D15	D0-D7
READ								
Read Even (x8)	H	H	L	L	H	L	High -Z	Data Out-Even
Read Odd (x8) (Note 1)	H	H	L	L	H	H	High -Z	Data Out-Odd
Read Odd (x8)	H	L	H	L	H	X	Data Out-Odd	High-Z
Read Word (x16)	H	L	L	L	H	X	Data Out-Odd	Data Out-Even
WRITE/ERASE								
Write Even (x8)	H	H	L	H	L	L	High -Z	Data In-Even
Write Odd (x8) (Note 1)	H	H	L	H	L	H	High -Z	Data In-Odd
Write Odd (x8)	H	L	H	H	L	X	Data In-Odd	High-Z
Write Word (x16) (Note 2)	H	L	L	H	L	X	Data In-Odd	Data In-Even
INACTIVE								
Card Output Disable	X	X	X	H	X	X	High-Z	High-Z
Standby	X	H	H	X	X	X	High-Z	High-Z

Notes:

1. *Byte access - Odd. In this x8 mode, A0 = V_{IH} outputs or inputs the “odd” byte (high byte of the x16 word on D0 - D7). This is accomplished internal to the card by transposing D8-D15 to D0-D7.*
2. *During 16-bit write and erase operations one IC of a device pair may complete the operation prior to the other. It is therefore necessary to monitor the card busy signal or poll both components before considering the operation complete.*

Legend:

H = V_{IH}
L = V_{IL}
X = Don't Care

Warning: Raising address lines to voltages levels above CMOS levels is not permitted. Applying voltages above these levels will destroy the card. Any attempt to identify memory components in this way is not permitted.

ATTRIBUTE MEMORY BUS OPERATIONS

Pins/Operation	/REG	/CE2	/CE1	/OE	/WE	A0	D8-D15	D0-D7
READ (Note 1)								
Read Even (x8)	L	H	L	L	H	L	High -Z	Data Out-Even
Read Odd (x8) (Note 2)	L	H	L	L	H	H	High -Z	Data Out-Odd Not Valid
Read Odd (x8) (Note 2)	L	L	H	L	H	X	Data Out-Odd Not Valid	High-Z
Read Word (x16) (Note 2)	L	L	L	L	H	X	Data Out-Odd Not Valid	Data Out-Even
WRITE (Note 1)								
Write Even (x8)	L	H	L	H	L	L	High -Z	Data In-Even
Write Odd (x8) (Note 3)	L	H	L	H	L	H	High -Z	Data In-Odd Not Valid
Write Odd (x8) (Note 3)	L	L	H	H	L	X	Data In-Odd Not Valid	High-Z
Write Word(x16) (Note 3)	L	L	L	H	L	X	Data In-Odd Not Valid	Data In-Even
INACTIVE								
Card Output Disable	X	X	X	H	X	X	High-Z	High-Z
Standby	X	H	H	X	X	X	High-Z	High-Z

Note:

1. Refer to the data sheets for the Catalyst CAT28C64B EEPROM for details on programming the attribute memory.
2. Data Read operations will produce data information that has no valid meaning for the Odd byte of information.
3. Data Write operations may be initiated, however data information for the Odd byte will not be stored.

Legend:

H = V_{IH}
L = V_{IL}
X = Don't Care

Warning: Raising address lines to voltages levels above CMOS levels is not permitted. Applying voltages above these levels will destroy the card. Any attempt to identify memory components in this way is not permitted.

PIN DESCRIPTIONS**Vcc****Card Power Supply**

Power input required for device operation. The Vcc must be 5.0 V \pm 5% (4.75V to 5.25V).

GND**Card Ground**

The V_{ss} pins of all IC components and related circuitry are connected to this card ground, which must be connected to the Host systems ground.

NC**Not Connected**

These pins are physically not connected to any circuitry.

A0-A25**Address Bus**

These signals are address input lines that are used for accesses to card memory. A0 is used to select the odd or even bank of memory components. A20 through A22 select which Device Pair of ICs will be accessed. A1 through A19 are used to select the specific address that is to be accessed on an individual memory component. A25, A24, and A23 are Not Connected.

(See also PIN ASSIGNMENTS Notes 1 - 3).

D0-D15**Data (Input/Output) Bus**

Data lines D0 through D15 are used to transfer data to and from the card. When memory is not selected or outputs are disabled data lines are placed in a high impedance state.

/OE**Output Enable Signal**

This active low input signal enables memory devices to activate data lines and output data information.

/WE**Write Enable Signal**

This active low input signal controls memory write functions and is used to strobe data into the card memory.

WP**Write Protect Signal**

This output signal indicates whether or not card write operations have been disabled by the Write Protect Switch (WPS). When the signal is asserted high, card write operations are disabled. When this signal is asserted low, card write operation function normally.

/CE1, /CE2**Card Enable**

These are active low inputs used to enable the card memory. /CE1 accesses the low bank of memory which provides storage for even numbered bytes. /CE2 accesses the high bank of memory, which provides storage for odd numbered bytes. During byte-wide operations these Card Enable signals are used in conjunction with address line A0 to access even or odd bytes of data. The memory card is de-selected and power consumption is reduced to stand-by levels when both /CE1 and /CE2 are driven high.

PIN DESCRIPTIONS**(CONTINUED)****/REG****Register Select Signal**

This active low input signal enables access to the Attribute memory EEPROM. Attribute memory is typically used to store the CIS file, which contains specific card information. Access to common memory is not possible when /REG is asserted low.

RESET**RESET Signal**

This is an active high input signal that normally is used by the Host to place the card in the deep power down mode of operation. On these cards this signal is Not Connected.

/WAIT**Extended Bus Cycle**

This active low output signal is used by the card to delay completion of a memory access operation. There are no wait states generated by these memory cards. For this reason the /WAIT signal is left open. It is the responsibility of the Host to pull this signal high to prevent false activation.

/BUSY**Ready Busy Signal**

This active low output signal normally indicates that at least one memory device in the card is busy performing a task. On these cards this signal is Not Connected.

/CD1, /CD2**Card Detect**

These pins are tied directly to ground and are used by the Host system to detect the presence of the card. If /CD1 and /CD2 are not both detected low by the Host, then the card is not properly inserted.

/VS1, /VS2**Voltage Sense Signals**

The Voltage Sense Signals notify the socket of the card's Vcc requirements on initial power up. When both /VS1 and /VS2 are open, as is the case on these cards, the card is identified to the Host system as a 5V only card.

/Vpp1, /Vpp2**Program and Peripheral Voltages**

These signals are normally used to supply additional programming voltages for memory devices that require programming voltages other than the Vcc supply. These memory cards require only Vcc voltages, therefore Vpp1 and Vpp2 are Not Connected.

/BVD1, /BVD2**Battery Voltage Detect**

These pins are normally used to indicate the status of an internal card battery. Since FLASH cards do not require or use a battery, these signals are internally pulled high by a resistor.

MANUFACTURER'S IDENTIFICATION CODE TABLE

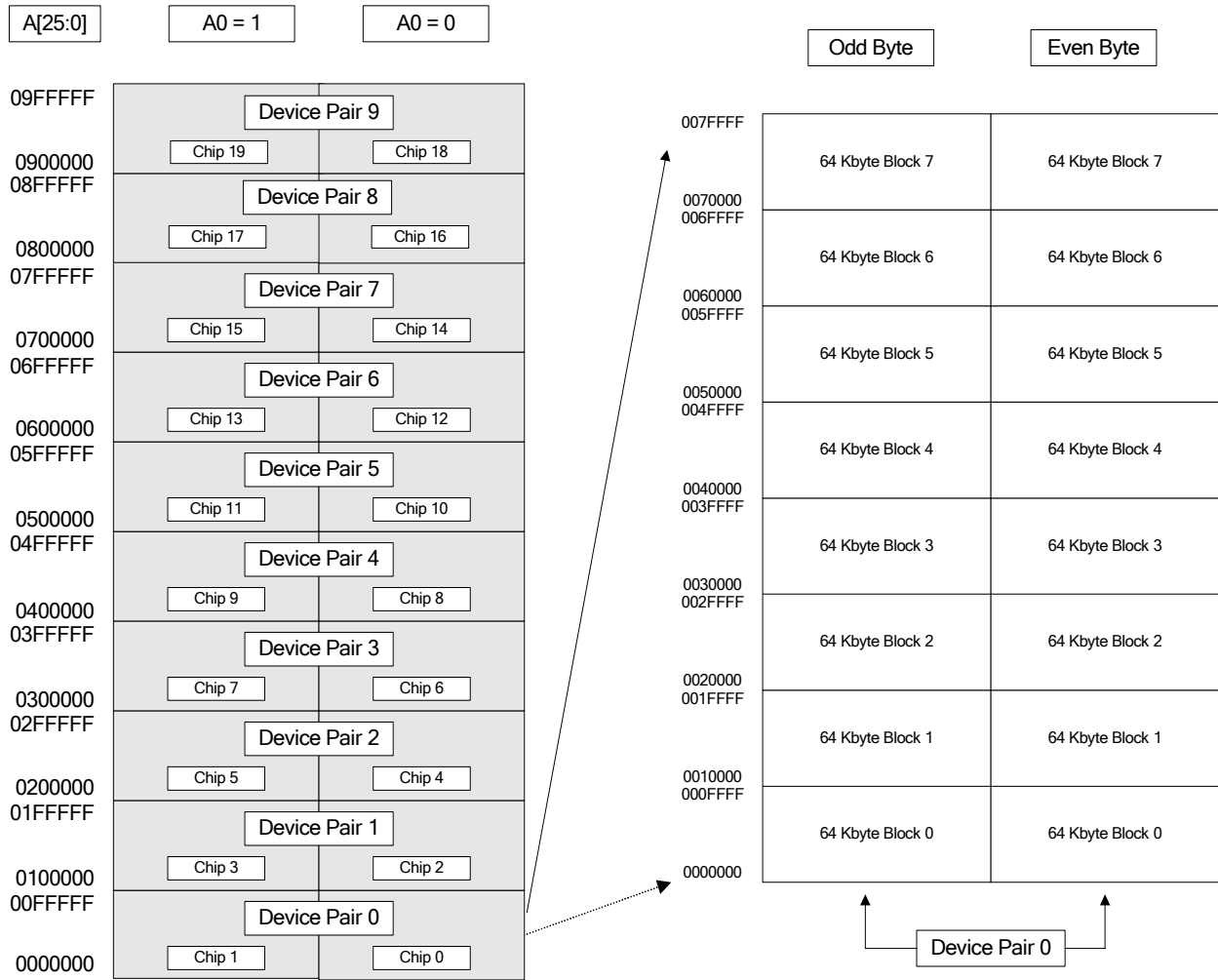
Device	Manufacturer	Hex Data		Operational Voltages
		Manufacturer Code	Device Code	V _{CC}
Am29F040	AMD	01h	A4h	5V ± 5%

The component manufacturer and device ID codes of each common memory component may be read from the Card Information Structure (CIS), or directly from each memory device. The CIS file is located in the Attribute Section of the card memory. Typically the CIS is stored in the EEPROM.

Directly reading the IDs from a memory component may be done by initiating the embedded Autoselect Command (See COMMAND DEFINITIONS Table for command sequence and codes). Once the appropriate command sequence codes have been written to a device, a read operation at chip address 00000h will return the Manufacture ID code and a read at 00001h will return the device ID code for the specific component use on the Card. This mode may only be exited by initiating valid read command operation.

For complete details of these memory devices refer to the manufacturers published data sheets.

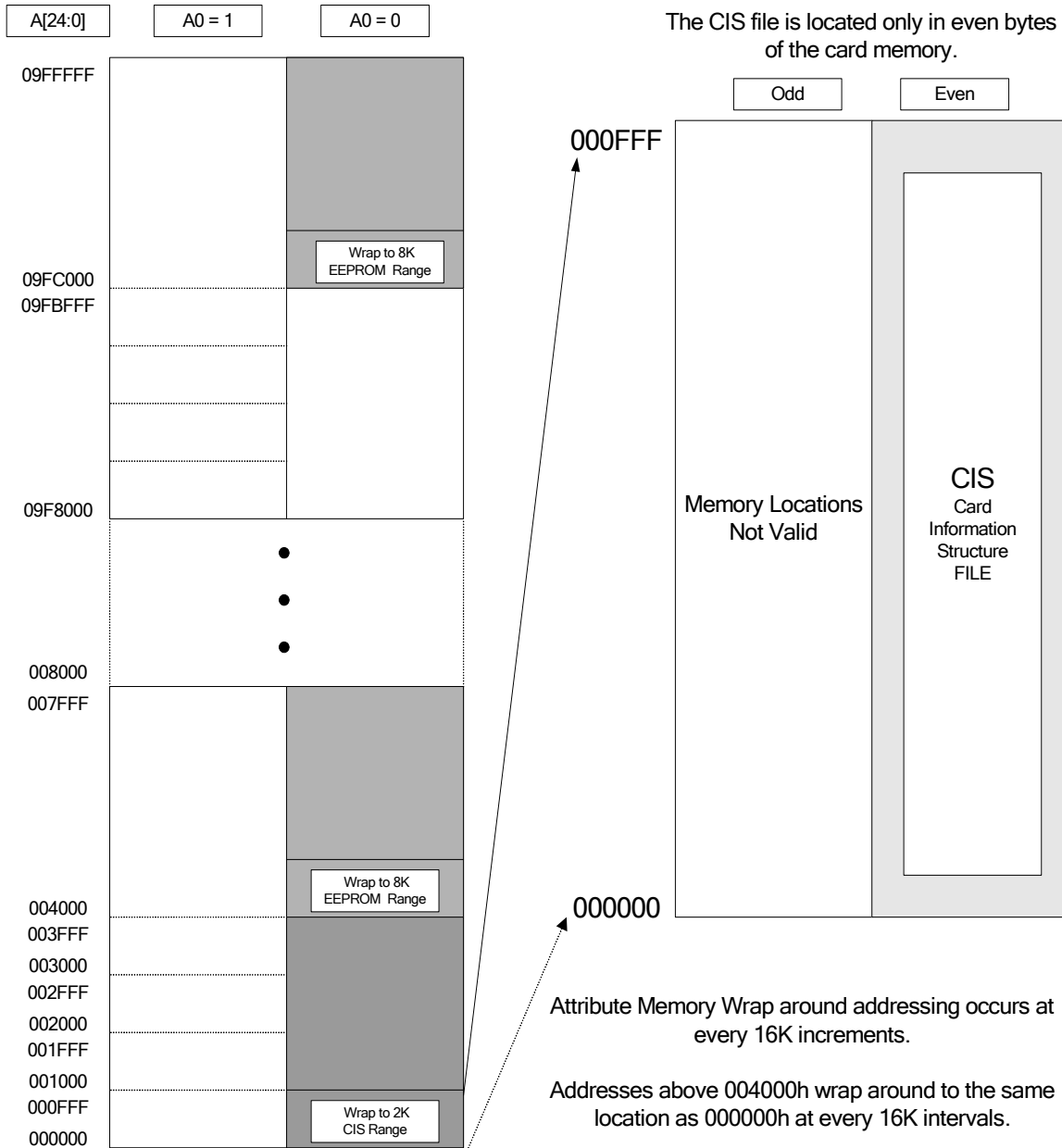
CARD COMMON MEMORY MAP



Each Device Pair Represents 1MByte of Card memory.

Each 4Mbit memory chip is segmented into 8 equally spaced 64 Kbyte blocks

ATTRIBUTE MEMORY MAP



COMMAND DEFINITIONS TABLE

All Address and Data values are in Hexadecimal unless otherwise noted. Addresses (Addr) are chip ,not card, addresses. Refer to datasheet of the Am29F040 for detailed information about the commands.

Am29F040 Command Definitions

Command Sequence	Cycles	Bus Cycles (Notes 2-4)											
		First		Second		Third		Fourth		Fifth		Sixth	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	RA	RD										
Reset	1	XXX	F0										
Auto select	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	01			
	Device ID	4	555	AA	2AA	55	555	90	X01	A4			
Program	4	555	AA	2AA	55	555	A0	PA	PD				
Chip Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend	1	XXX	B0										
Erase Resume	1	XXX	30										

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Address latch on the falling edge of the WE# or CE# puls whichever happens later

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A20-A16 select a unique sector.

Note:

Cards may be read in Byte wide or Word-Wide modes. In Word-Wide mode, each byte of memory is independently read from each device pair. Each memory device in the card may read at different rates. Therefore the Host should wait until each byte has a valid data output (See MEMORY BUS OPERATIONS Table for specific Control line States and CARD TIMING CHARACTERISTICS for timing information).

CARD ADDRESS VS. CHIP ADDRESS CALCULATIONS

Specific memory addresses may be calculated by the following method;

Card Address	Chip Address	Device Pair Number	Chip Memory Capacity	Binary Shift Left by 1 bit	A0 = 0 = Even byte A0 = 1 = Odd byte
A [25 : 0] =	(Addr + (DP# * 80000h)) * 2) + A0				

Where: Addr = Chip addresses.

DP# = the device pair number that the memory device belongs to (see Common Memory Map).

A0 = Card address line used for access to even or odd byte of memory.

CARD TIMING CHARACTERISTICS

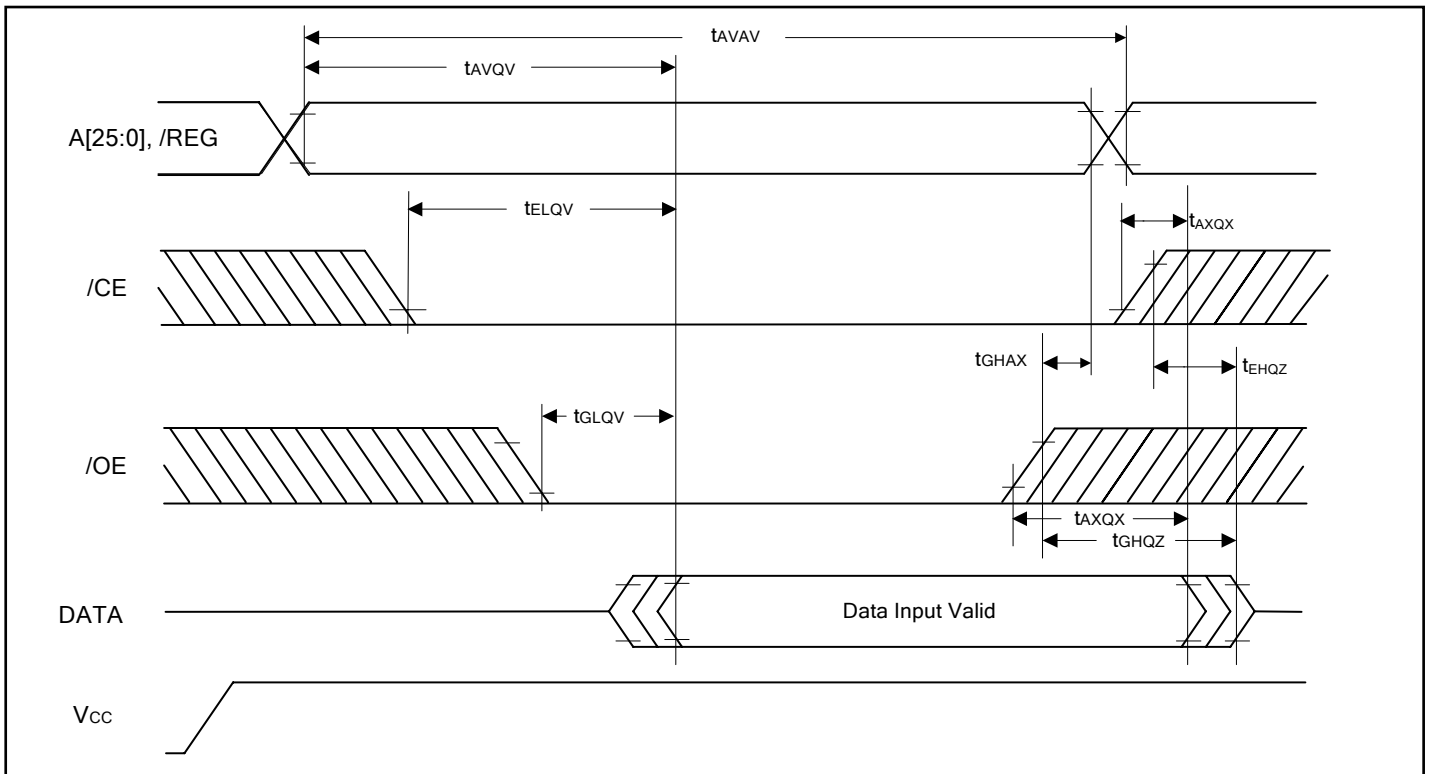
(Standard operating times for both Common and Attribute Memory unless otherwise noted.)
 Refer to datasheet of the Am29F040 for more detailed information.

Read Cycle Timing (/WE = V_{HI})

Parameter	Symbol	150ns		200ns		Units
		Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	150		200		
Address Access Time	t _{AVQV}		150		200	ns
Card Enable Access Time	t _{ELQV}		150		200	ns
Output Enable Access Time	t _{GLQV}		75		100	ns
/OE High to Data Output Disable	t _{GHQZ}		50		75	ns
Output Hold Time from Addresses, /CE or /OE Whichever Occurs First	t _{AXQX}	0		0		ns
CE High to Data Output Disable	t _{EHQZ}		50		75	ns

Common and Attribute Memory Read and Write Cycle Timing.

READ Cycle Timing (/WE=V_{HI})



CARD TIMING CHARACTERISTICS

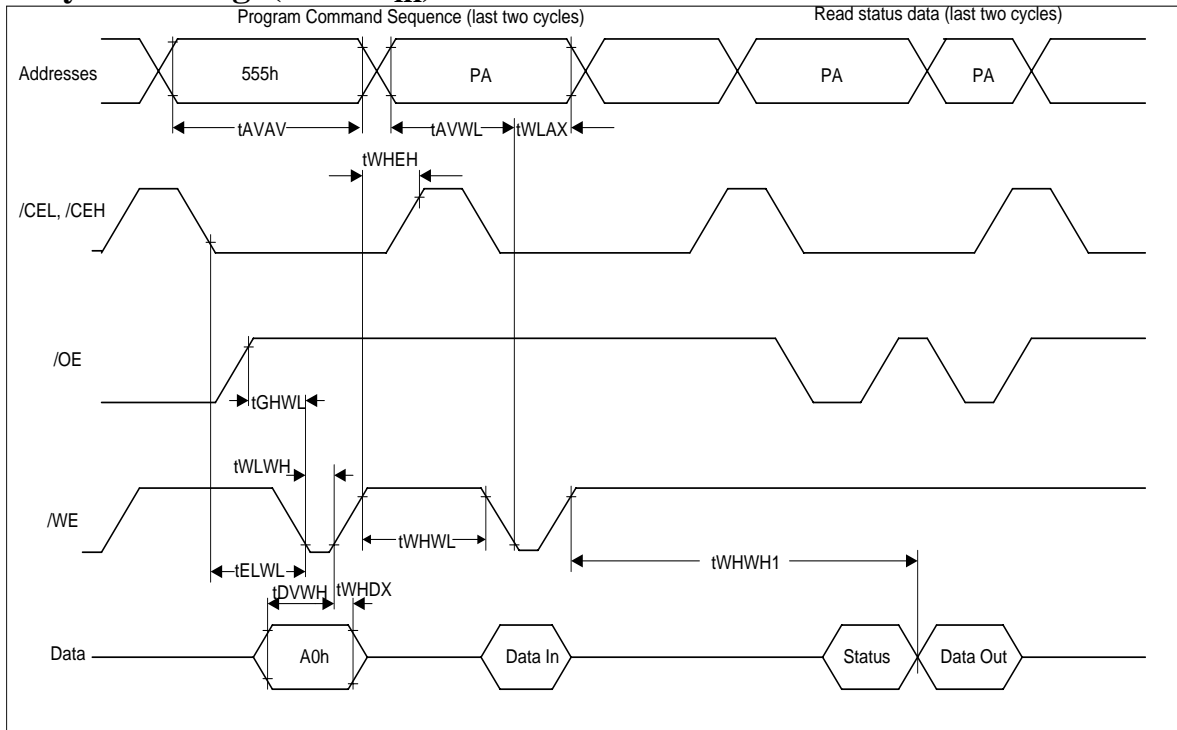
(CONTINUED)

/WE controlled write timing and data polling

Write Cycle Timing (/OE = V_{IH})

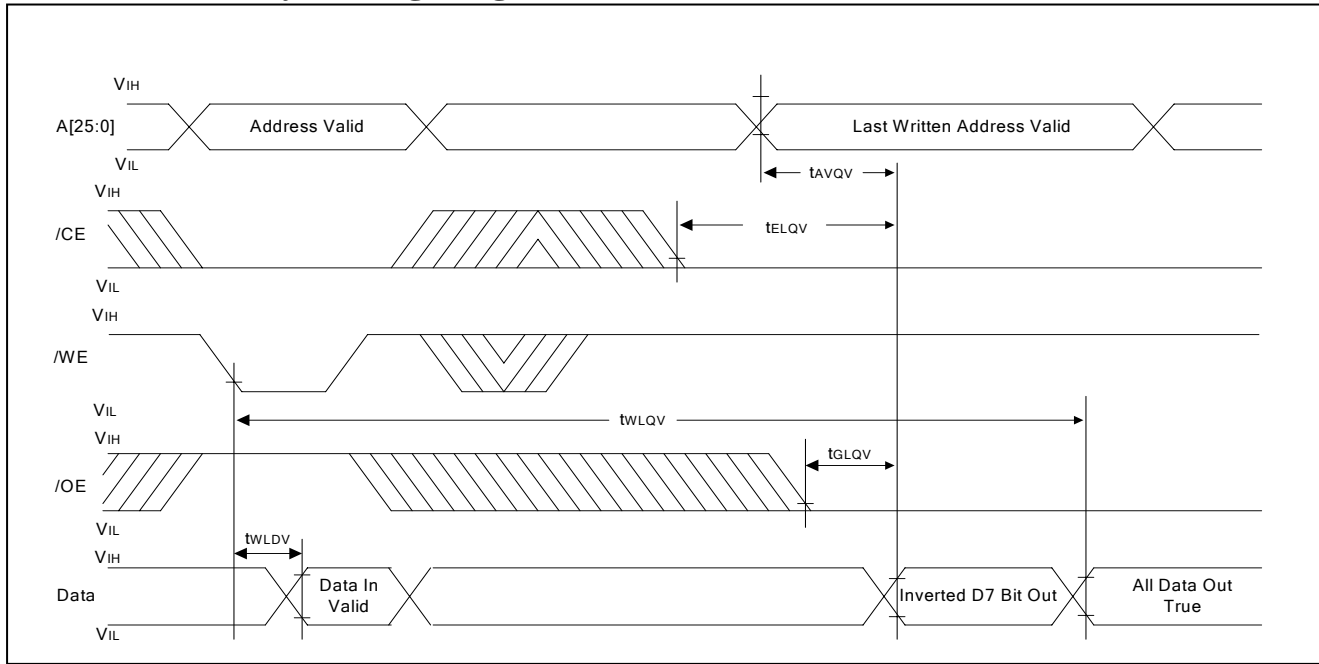
Item	Symbol	150ns	200ns	Units
		Min	Min	
Write Cycle Time	t _{AVAV}	150	200	ns
Write Pulse Width	t _{WLWH}	60	75	ns
Write Pulse Width High	t _{WHWL}	30	30	ns
Address Setup Time	t _{AVWL}	0	0	ns
Data Setup time for /WE inactive	t _{DVWH}	60	75	ns
Card Enable Setup Time to /WE or /OE active	t _{ELWL}	0	0	ns
Data Hold Time from /WE inactive	t _{WHDX}	0	0	ns
Address Hold Time from /WE inactive	t _{WLAX}	60	75	ns
/CE Hold Time form /WE inactive	t _{WHEH}	0	0	ns
Read Recovery Time Before Write	t _{GHWL}	0	0	ns
Byte Programming Operation	t _{WHWH1}	8 typical	8 typical	μs
Sector Erase Operation		1 typical	1 typical	sec

Write Cycle Timing (/OE=V_{IH})



CARD TIMING CHARACTERISTICS (CONTINUED)

Attribute Memory Timing Diagram



Attribute Parameter	(Note 1, 2)	Symbol	150ns		200ns		Unit
			Min	Max	Min	Max	
Read Cycle Time		t_{AVAV}	150		200		ns
Card Enable Access Time		t_{ELQV}		150		200	ns
Output Enable Access Time		t_{GLQV}				70	ns
Write Enable Low to Data Valid Time		t_{WLDV}				1000	ns
Write Enable Low to Data Read Valid Time		t_{WLQV}				1	ms

Note:

1. All timing values are constant with standard Read/Write Times, unless otherwise shown in the Table.
2. Attribute memory latches address values on the falling edge of /WE. Data is latched on the rising edge of /WE.

Attribute Data Polling Mode:

Data Polling the 28C64B features /DATA polling to signal the completion of a byte write cycle. During a write cycle, an attempt to read the last byte written to memory will produce the complement of the D7 (D6 to D0 are indeterminate). After completion the true data is available. Data Polling allows a simple read/compare operation to determine the status of the chip.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min.	Max.	Units
V _{CC} Supply Voltage	V _{CC}	4.75	5.25	V
Operating Temperature Commercial	T _A	-10	+70	°C
Operating Temperature Industrial	T _A	-40	+85	°C

DC CHARACTERISTICS

Supply current is an RMS value. Typical values at nominal V_{CC} voltage at T_A = +25°C.

Symbol	Parameter	Condition	Min	Max	Units
I _{CCS}	Standby Current	Per device: TTL; V _{CC} = V _{CC} Max , V _{IN} = GND to V _{CC} /CE1, /CE2 = V _{IH}		1	mA
I _{CCR}	Active Read Current	Per device: TTL; V _{CC} = V _{CC} Max /CE1 or /CE2 = V _{IL}		30	mA
		Byte (×8) Byte (×16) /OE = V _{IH}		60	mA
I _{CCW}	Active Program Current	Per device: /CE1 or /CE2 = GND (including programming current)		40	mA
I _{CCE}	Active Sector Erase Current	Per device: (including programming current)		40	mA
I _{IL}	Input Leakage Current	V _{IN} = GND to V _{CC} , V _{CC} MAX Per Pin:	-300	+20	µA
I _{ILpu}	Input Leakage Current with Pull Up Resistor	V _{IN} = GND to V _{CC} , V _{CC} MAX Per Pin with 10KΩ pull up resistor		+500	µA
I _{ILpd}	Input Leakage Current with Pull Down Resistor	V _{IN} = GND to V _{CC} , V _{CC} MAX Per Pin with 100KΩ pull down resistor		-50	µA
I _{OLpd}	Output Leakage Current with Pull Down Resistor	V _{OUT} = GND to V _{CC} , V _{CC} MAX Per Pin with 100KΩ pull down resistor		±20	µA
V _{IL}	Input Low Voltage (Note 1)			0.8	V
V _{IH}	Input High Voltage (Note 1)		2		V
V _{OL}	Output Low Voltage (Note 1)	V _{CC} = V _{CC} Min I _{OL} = 3.22 mA		0.26	V
V _{OH}	Output High Voltage (Note 1)	CMOS; V _{CC} = V _{CC} Min I _{out} = 2.0 mA	3.98		V
V _{LKO}	V _{CC} Erase / Program Lock Voltage		3.2	4.2	V

Notes:

1. Sample tested by component manufacturer.

CARD INFORMATION STRUCTURE

The CIS is data, which describes the PCMCIA card and is described by the PCMCIA standard. This information can be used by the Host system to determine a number of things about the card that has been inserted. For information regarding the exact nature of this data, and how to design Host software to interpret it, refer to the PCMCIA standard Metaformat Specification.

The following is an example of the contents of a typical CIS file for Flash cards covered by this product specification. Please note that information can vary for different part numbers.

<u>Physical Address</u>	<u>Logical Address</u>	<u>Data Value(s)</u>	<u>Tuple Description</u>
00h	00h	01h	CISTPL_DEVICE
02h	01h	03h	CISTPL_LINK
04h	02h	53h (52h)	Speed = 150ns (200ns), WPS=Yes, FLASH
06h	03h	1Eh (Note 1)	Bits 2-0 = 110b = 2 Meg units, Bits 7-3 = 00011b = 4 Units (0=1, 1=2...) 2 Meg x 4 = 8 Meg size
08h	04h	FFh	CISTPL_END - End of Tuple
0Ah	05h	18h	CISTPL_JEDEC
0Ch	06h	03h	CISTPL_LINK
0Eh	07h	01h	Manufacturer ID (AMD)
10h	08h	A4h	Device ID (Am29F040)
12h	09h	FFh	CISTPL_END - End of Tuple
14h	0Ah	1Eh	CISTPL_DEVICEGEO
16h	0Bh	07h	CISTPL_LINK
18h	0Ch	02h	DGTPL_BUS - Bus Width - 2 Bytes
1Ah	0Dh	11h	DGTPL_EBS - Erase Block Size 2^10h = 64K Bytes or Words
1Ch	0Eh	01h	DGTPL_RBS - Byte Accessible
1Eh	0Fh	01h	DGTPL_WBS - Byte Accessible
20h	10h	01h	DGTPL_PART - One Partition
22h	11h	01h	DGTPL_HWIL - No Interleave
24h	12h	FFh	CISTPL_END - End of Tuple

Note:

1. Refer to the table (right) for SMART Modular part numbers and corresponding data value.

Part Number	Data value
FX01M-XX-1XX14	0Dh
FX02M-XX-1XX14	06h
FX04M-XX-1XX14	0Eh
FX08M-XX-1XX14	1Eh
FX10M-XX-1XX14	9Dh

CARD INFORMATION STRUCTURE (CONTINUED)

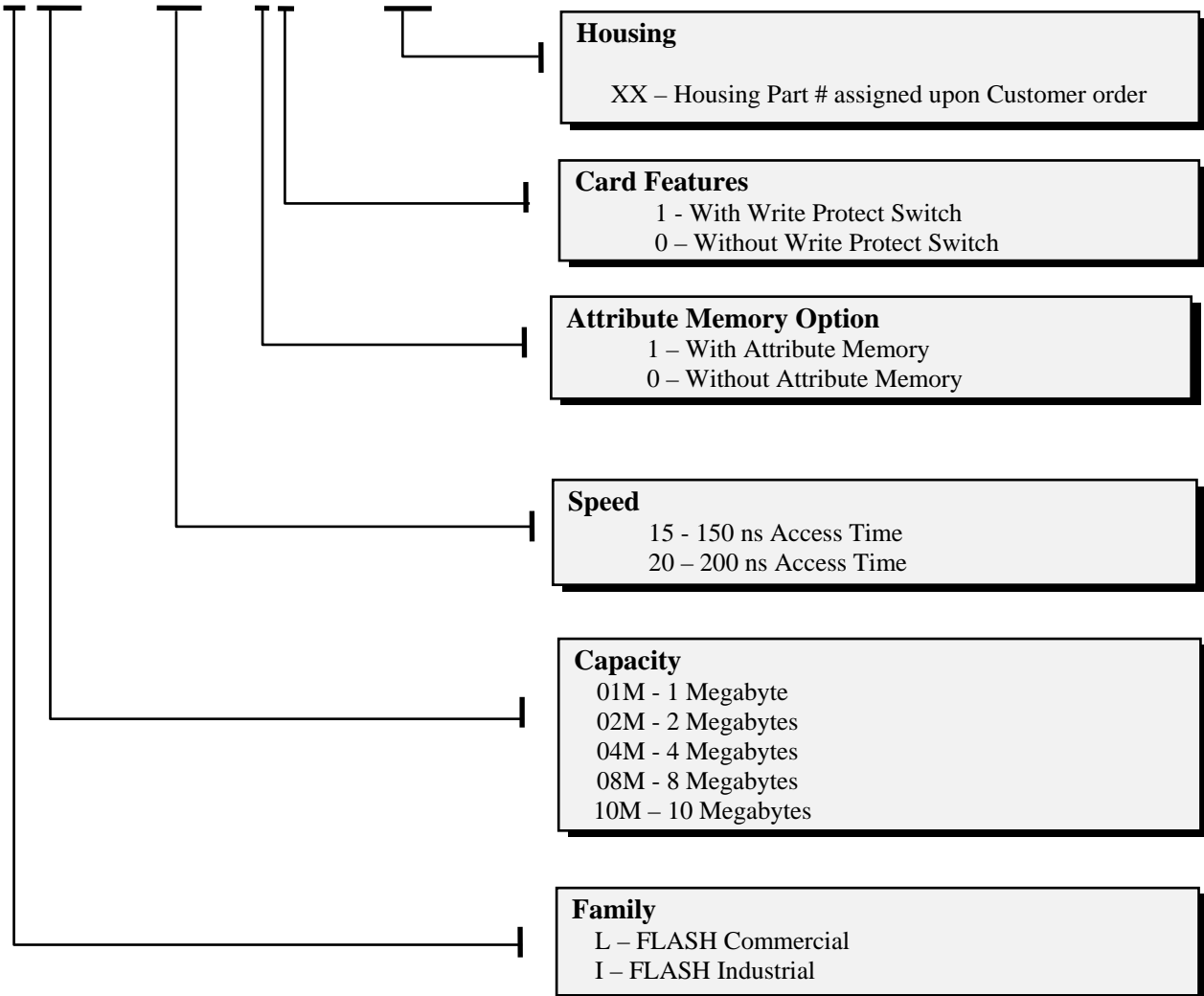
<u>Physical Address</u>	<u>Logical Address</u>	<u>Data Value(s)</u>	<u>Tuple Description</u>
26h	13h	15h	CISTPL_VERS1
28h	14h	52h	CISTPL_LINK
2Ah	15h	04h	TPLL1_V1_MAJOR (PCMCIA 2.1/JEIDA 4.2)
2Ch	16h	01h	TPLL1_V1_MINOR
2Eh...66h	17h...33h	43 65 6E 74 65 6E 6E 69 61 6C 20 54 65 63 68 6E 6F 6C 6F 67 69 65 73 2C 20 49 6E 63 2E	ASCII Text is : Centennial Technologies, Inc. {29 Characters total}
68h	34h	00	NULL String Delimiter (String 1)
6Ah...84h	35h...42h	46 4C 30 38 4D 2D 32 30 2D 31 31 31 31 34	ASCII Text is : FL08M-20-11114 (Note 2) {14 Characters total}
86h	43h	00	NULL String Delimiter (String 2)
88h...C6h	44h...63h	38 20 4D 45 47 20 46 4C 41 53 48 20 77 2F 34 20 4D 62 69 74 20 41 4D 44 20 64 65 76 69 63 65 73	ASCII Text is : 8 MEG FLASH w/4 Mbit AMD devices (Note 3) {32 Characters total}
C8h	64h	00	NULL String Delimiter (String 3)
CAh	65h	00	NULL String Delimiter (String 4)
CCh	66h	FF	CISTPL_END - End of Tuple
CEh	67h	FF	CISTPL_END - End of Chain Tuple

Notes:

- 2. Specific Product description will be listed.
- 3. Specific Product memory capacities will be listed for specific products.

SALES AND SUPPORT

To order or to obtain information on pricing or delivery, contact a SMART Modular Technologies Sales and Support representative.

PART NUMBER INFORMATION
FLXXM - 15 - 11114 - XX


Variations of this standard Centennial Technologies Product are available. Contact a Centennial Sales Representative for additional information.

ORDERING INFORMATION

Description	Ordering Part Number	
	RoHS	Non RoHS
FL01M-15-11114-67	PG22049	PM22049
FL01M-20-11114-67	PG22030	PM22030
FI02M-20-11114-67	PG23069	PM23069
FL02M-15-11114-67	PG23067	PM23067
FL02M-20-11114-03	PG23023	PM23023
FL04M-20-11114-67	PG24045	PM24045
FL08M-20-11114-03	PG24141	PM24141
FL10M-15-11114-03	PG24211	PM24211
FL10M-20-11114-67	PG24636	PM24636

Note:

PM = Non RoHS products

PG = RoHS products



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