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Product Specification

Industrial Rugged PCMCIA ATA Cards

-Hermit Series-

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1. Introduction

APRO Industrial Rugged PCMCIA ATA Card – Hermit Series designed to follow ATAPI-4 (ATA-66) standard. The main used Flash memories are Samsung NAND Type SLC Flash memory chips. The available Card capacities are 128MB, 256MB, 512MB, 1GB, 2GB, 4GB, 8GB and 16GB. The operating temperature grade is optional for commercial level 0°C ~ 70°C and wide temperature level -40°C ~ +85°C. The APRO Industrial Rugged PCMCIA ATA Cards- Hermit Series are designed electrically complies with the conventional IDE hard Card and support True IDE Mode. The data transfer modes supports PIO mode 0, 1, 2, 3, and 4 or MDMA- 0,1,2,3, and 4 or UDMA- 0, 1, 2, 3, and 4. The fastest reading speed is up to 40 MB/sec and writing speed is up to 20 MB/sec.

The APRO Industrial PCMCIA ATA products provide a high level interface to the host computer. This interface allows a host computer to issue commands to the Rugged PCMCIA ATA Card to read or write blocks of memory. Each sector is protected by a powerful 4 bits Error Correcting Code (ECC). APRO Industrial Rugged PCMCIA ATA Card's HA-Series intelligent controller manages interface protocols, data storage and retrieval as well as ECC, defect handling and diagnostics, power management and clock control.

Figure 1 shows a block diagram of the used high tech Industrial Rugged PCMCIA ATA Card controller.

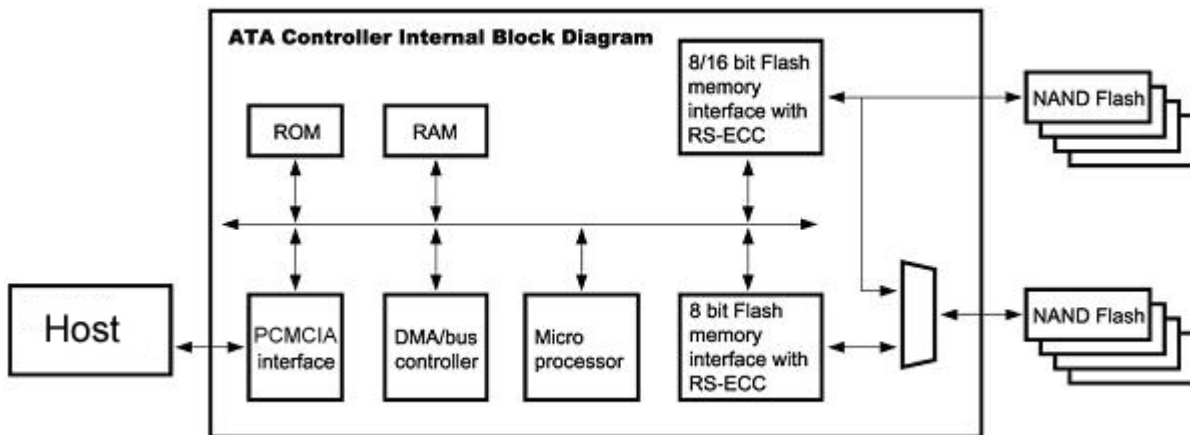


Figure 1: Rugged PCMCIA ATA Card HA-Series Controller Block Diagram

1.1. Scope

This document describes the features and specifications and installation guide of APRO's Industrial Rugged PCMCIA ATA Cards – Hermit Series. In the appendix, there provides order information, warranty policy, RMA/DOA procedure for the most convenient reference.

1.2. System Features

- Non-volatile memory and no moving parts
- NAND type SLC flash technology
- Card capacity from 128MB to 16GB
- ATA inter face and support PC Card Memory mode, PC Card I/O mode and True IDE mode
- Data transfer supports PIO 0~ 4, MDMA 0~ 4, and UDMA 0~4
- Performance up to 40 MB/sec
- Automatic 4 bits error correction (ECC) and retry capabilities
- +5 V $\pm 10\%$ or +3.3 V $\pm 5\%$ operation
- MTBF 3,000,000 hours.
- Shock : 1,500G , compliance to MIL-STD-810F
- Vibration : 15G, compliance to MIL-STD-810F
- Support various rugged and harsh environments
- Very high performance, very low power consumption
- Low weight, Noiseless

1.3. PCMCIA Specification

APRO Industrial PCMCIA ATA Flash Cards are fully electrically compatible with following PCMCIA specifications:

- *PCMCIA PC Card Standard, 7.0*
- *PCMCIA PC card Specification, 7.0*

PCMCIA (Personal Computer Memory Card International Association)
2635 North First Street Suite #218
San Jose, CA 95134 USA
Tel: (408) 433-2273
Fax: (408) 433-9558
<http://www.pcmcia.org>

1.4. ATA/ATAPI-6 Standard

APRO Industrial Rugged PCMCIA ATA Cards – Hermit Series is compliant to ATA/ATAPI-6 and below version.

1.5. Technology Independence

With the proprietary method to manage variable kinds of flash in terms of wear-leveling and ECC (Error Code Correction), it translate the ATA control, address and data bus signals into the management unit of NAND type flash devices and constitute the Rugged PCMCIA ATA Cards more ideal than the conventional hard Card drives.

2. Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. System Environmental Specifications

Table 1: Environmental Specification

		Commercial Grade	Industrial Grade
APRO Industrial Rugged PCMCIA ATA Card		SRAFxxxH-ACSC Series	WRAFxxxH-AISI Series
Temperature	Operating:	0°C ~ +70°C	-40°C ~ +85°C
	Non-operating:	-55°C ~ +95°C	-55°C ~ +95°C
Humidity	Operating & Non-operating:	10% ~ 95% non-condensing	
Vibration	Operating & Non-operating:	15G peak-to-peak maximum	
Shock	Operating & Non-operating:	1,500G maximum	

2.2. System Power Requirements

Table 2: Power Requirement

		Commercial Grade	Industrial Grade
APRO Industrial Rugged PCMCIA ATA Card		SRAFxxxH-ACSC Series	WRAFxxxH-AISI Series
DC Input Voltage (VCC) 100mV max. ripple(p-p)		5V±10% or 3V±10%	
+5V Current (Average value)	Reading Mode :	125 mA (Typ.)	
	Writing Mode :	120 mA (Typ.)	
	Power Down Mode :	1.3 mA (Typ./ Max.)	
+3V Current (Average value)	Reading Mode :	121 mA (Typ.)	
	Writing Mode :	115 mA (Typ.)	
	Power Down Mode :	0.6 mA (Typ.), 0.7 mA (Max.)	

2.3. System Performance

Table 3: System Performances

Data Transfer Mode supporting		- PIO mode : 0, 1, 2, 3, 4 (PIO – 4 defaulted) - DMA SW Mode: Not supported - DMA MW Mode:0,1,2, 3 and 4 - UDMA Mode: 0,1,2,3, and 4								
Data Transfer Rate To/From Host		16.6Mybtes/sec burst under PIO Mode 4 66.6Mbytes/sec burst under UDMA-4 Mode								
Average Access Time		0.6 ms(estimated)								
Maximum Performance	Capacity	128MB	256MB	512MB	1GB	2GB	4GB	8GB	16GB	
	Sequential Read (MB/s)	PIO- 4	4.6	4.7	4.6	4.6	4.7	4.7	4.6	TBC
		UDMA -4	18.5	33.7	21.1	21.1	39.6	39.6	39.6	39.0
	Sequential Write(MB/s)	PIO- 4	4.2	4.4	4.0	4.4	4.6	4.6	4.0	TBC
UDMA -4		18.6	16.7	19.7	19.4	19.9	19.9	19.4	18.7	
The number of Channel		Single	Dual	Single	Single	Dual	Dual	Dual	Dual	

Note:

(1). All values quoted are typically at 25°C and nominal supply voltage.

(2). Testing of the Industrial Rugged PCMCIA ATA Card maximum performance was performed under the following platform:

- Computer with AMD 3.0GHz processor
- Windows XP Professional operating system

2.4. System Reliability

Table 4: System Reliability

MTBF	3,000,000 hours
Data Reliability	<1 non-recoverable error in 10^{14} bits read <1 erroneous correction in 10^{20} bits read
Wear-leveling Algorithms	Supportive
ECC Technology	4 bits Error Connection Code
Endurance	Greater than 2,000,000 cycles Logically contributed by Wear-leveling and advanced bad sector management
Data Retention	10 years

2.5. Physical Specifications

Refer to Table 5 and see Figure 2 for PCMCIA ATA Flash Card physical specifications and dimensions.

Table 5: Physical Specifications

APRO Industrial PCMCIA ATA Flash Card (Type II PCMCIA ATA Flash)	
Length:	85.50±0.15mm(3.37±0.006 in)
Width:	54.00±0.10mm(2.13±0.004 in)
Thickness:	5.00±0.10mm(0.2±0.004 in)
Weight:	43.0g(1.52oz) typical

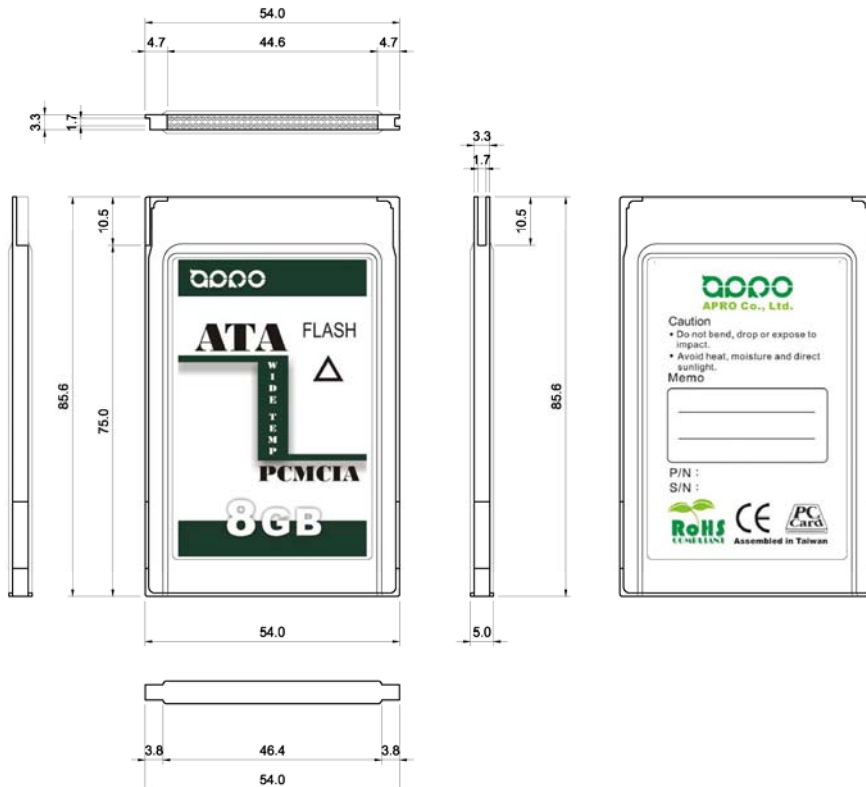


Figure 2: Rugged Metal PCMCIA ATA Flash Card Dimensions

2.6. Capacity Specifications

APRO Industrial Rugged PCMCIA ATA Cards are built-in mainly Samsung NAND Type SLC Flash memory chips. The Table 6 shows the equipollent part number of applied Samsung Flash memory chips for each card.

Table 6: Card Configuration vs. Samsung NAND SLC part number

Card Capacity	Samsung SLC Flash Memory Part Number * Q'TY	
128MB	Commercial Grade:	K9F1G08U0A-PCB0(1Gb) or equipollent * 1
	Industrial Grade:	K9F1G08U0A-PIB0 (1Gb) or equipollent * 1
256MB	Commercial Grade:	K9F2G08U0A-PCB0 (2Gb) or equipollent * 1
		K9F1G08U0A-PCB0(1Gb) or equipollent * 2
	Industrial Grade:	K9F2G08U0A-PIB0 (2Gb) or equipollent * 1
		K9F1G08U0A-PIB0 (1Gb) or equipollent * 2
512MB	Commercial Grade:	K9F4G08U0M-PCB0 (4Gb) or equipollent * 1
		K9F2G08U0A-PCB0 (2Gb) or equipollent * 2
		K9F1G08U0A-PCB0(1Gb) or equipollent * 4
	Industrial Grade:	K9F4G08U0M-PIB0 (4Gb) or equipollent * 1
		K9F2G08U0A-PIB0 (2Gb) or equipollent * 2
		K9F1G08U0A-PIB0 (1Gb) or equipollent * 4
1GB	Commercial Grade:	K9K8G08U0M-PCB0 (8Gb) or equipollent * 1
		K9F4G08U0M-PCB0 (4Gb) or equipollent * 2
	Industrial Grade:	K9K8G08U0M-PIB0 (8Gb) or equipollent * 1
		K9F4G08U0M-PIB0 (4Gb) or equipollent * 2
2GB	Commercial Grade:	K9WAG08U1M-PCB0 (16Gb) or equipollent *1
		K9K8G08U0M-PCB0 (8Gb) or equipollent *2
	Industrial Grade:	K9WAG08U1M-PIB0 (16Gb) or equipollent *1
		K9K8G08U0M-PIB0 (8Gb) or equipollent *2
4GB	Commercial Grade:	K9WAG08U1M-PCB0 (16Gb) or equipollent *2
		K9K8G08U0M-PCB0 (8Gb) or equipollent *4
	Industrial Grade:	K9WAG08U1M-PIB0 (16Gb) or equipollent *2
		K9K8G08U0M-PIB0 (8Gb) or equipollent *4
8GB	Commercial Grade:	K9WAG08U1M-PCB0 (16Gb) or equipollent *4
	Industrial Grade:	K9WAG08U1M-PIB0 (16Gb) or equipollent *4
16GB	Commercial Grade:	K9WBG08U1M-PCB0 (32Gb) or equipollent *4
	Industrial Grade:	K9WBG08U1M-PIB0 (32Gb) or equipollent *4

The table 7 shows the specific capacity for the various models and the default number of heads, sectors/track and cylinders.

Table 7: Model Capacity

Unformatted Capacity	Default Cylinder	Default Head	Default Sector	Default CHS Capacity
32MB	500	8	16	64,000
64MB	500	8	32	128,000
128MB	500	16	32	256,000
256MB	1,000	16	32	512,000
512MB	1,015	16	63	1,023,120
1,024MB	2,031	16	63	2,047,248
2.04GB	4,063	16	63	4,095,504
4GB	8,146	16	63	8,211,168
8GB	16,000	16	63	16,128,000
16GB	32,235	16	63	32,492,880

3. Interface Description

3.1. Physical Description

The PCMCIA ATA Card uses a 68 pin connector. The connector in the host consists of two rows of 34 pins with 0.05 inch spacing (1.27mm). Female pins are used on the card side, male pins on the system end.

3.2. Pin Assignments

The signal/pin assignments are listed in below Table 8. Low active signals have a “-” prefix. Pin types are Input, Output or Input/Output.

Table 8: Pin Assignments and Pin Type

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
Pin No.	Signal Name	Pin Type	Pin No.	Signal Name	Pin Type	Pin No.	Signal Name	Pin Type
1	GND	Ground	1	GND	Ground	1	GND	Ground
2	D3	I/O	2	D3	I/O	2	D3	I/O
3	D4	I/O	3	D4	I/O	3	D4	I/O
4	D5	I/O	4	D5	I/O	4	D5	I/O
5	D6	I/O	5	D6	I/O	5	D6	I/O
6	D7	I/O	6	D7	I/O	6	D7	I/O
7	CE1#	I	7	CE1#	I	7	CS0#	I
8	A10	I	8	A10	I	8	A10 ²	I
9	OE#	I	9	OE#	I	9	OE#	I
10	NC	-	10	NC	-	10	NC	-
11	A9	I	11	A9	I	11	A9 ²	I
12	A8	I	12	A8	I	12	A8 ²	I
13	NC	-	13	NC	-	13	NC	-
14	NC	-	14	NC	-	14	NC	-
15	WE#	I	15	WE#	I	15	WE# ³	I
16	RDY/BSY#	O	16	IREQ#	O	16	INTRQ	O
17	VCC	Power	17	VCC	Power	17	VCC	Power
18	NC	-	18	NC	-	18	NC	-
19	NC	-	19	NC	-	19	NC	-
20	NC	-	20	NC	-	20	NC	-
21	NC	-	21	NC	-	21	NC	-
22	A7	I	22	A7	I	22	A7 ²	I
23	A6	I	23	A6	I	23	A6 ²	I
24	A5	I	24	A5	I	24	A5 ²	I
25	A4	I	25	A4	I	25	A4 ²	I
26	A3	I	26	A3	I	26	A3 ²	I
27	A2	I	27	A2	I	27	A2	I
28	A1	I	28	A1	I	28	A1	I
29	A0	I	29	A0	I	29	A0	I
30	D0	I/O	30	D0	I/O	30	D0	I/O
31	D1	I/O	31	D1	I/O	31	D1	I/O
32	D2	I/O	32	D2	I/O	32	D2	I/O
33	WP	O	33	IOIS16#	O	33	IOCS16#	O
34	GND	Ground	34	GND	Ground	34	GND	Ground
35	GND	Ground	35	GND	Ground	35	GND	Ground
36	CD1#	O	36	CD1#	O	36	CD1#	O
37	D11 ¹	I/O	37	D11 ¹	I/O	37	D11 ¹	I/O
38	D12 ¹	I/O	38	D12 ¹	I/O	38	D12 ¹	I/O

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
Pin No.	Signal Name	Pin Type	Pin No.	Signal Name	Pin Type	Pin No.	Signal Name	Pin Type
39	D13 ¹	I/O	39	D13 ¹	I/O	39	D13 ¹	I/O
40	D14 ¹	I/O	40	D14 ¹	I/O	40	D14 ¹	I/O
41	D15 ¹	I/O	41	D15 ¹	I/O	41	D15 ¹	I/O
42	CE2# ¹	I	42	CE2# ¹	I	42	CS1# ¹	I
43	VS1#	O	43	VS1#	O	43	VS1#	O
44	IORD#	I	44	IORD#	I	44	IORD	I
45	IOWR#	I	45	IOWR#	I	45	IOWR	I
46	NC	-	46	NC	-	46	NC	-
47	NC	-	47	NC	-	47	NC	-
48	NC	-	48	NC	-	48	NC	-
49	NC	-	49	NC	-	49	NC	-
50	NC	-	50	NC	-	50	NC	-
51	VCC	Power	51	VCC	Power	51	VCC	Power
52	NC	-	52	NC	-	52	VPP	-
53	NC	-	53	NC	-	53	NC	-
54	NC	-	54	NC	-	54	NC	-
55	NC	-	55	NC	-	55	NC	-
56	NC	-	56	NC	-	56	CSEL#	-
57	VS2#	O	57	VS2#	O	57	VS2#	O
58	RESET	I	58	RESET	I	58	RESET#	I
59	WAIT#	O	59	WAIT#	O	59	IORDY	O
60	INPACK#	O	60	INPACK#	O	60	DREQ	O
61	REG#	I	61	REG#	I	61	DMACK	I
62	BVD2	I/O	62	SPKR#	I/O	62	DASP#	I/O
63	BVD1	I/O	63	STSCHG#	I/O	63	PDIAG#	I/O
64	D8 ¹	I/O	64	D8 ¹	I/O	64	D8 ¹	I/O
65	D9 ¹	I/O	65	D9 ¹	I/O	65	D9 ¹	I/O
66	D10 ¹	I/O	66	D10 ¹	I/O	66	D10 ¹	I/O
67	CD2#	O	67	CD2#	O	67	CD2#	O
68	GND	Ground	68	GND	Ground	68	GND	Ground

Note:

- 1) These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.
- 2) The signal should be grounded by the host.

3.3. Electrical Description

The PCMCIA ATA Flash Card Series is optimized for operation with hosts, which support the PCMCIA/ I/O interface standard conforming to the PC Card ATA specification. However, the PCMCIA ATA Flash Card may also be configured to operate in systems that support only the memory interface standard. Table 9: describes the I/O signals.

Table 9: Signal Description

Signal Name	Mode of operation	Pin Type	Pin No(s).	Description
-CD1, -CD2 (Card Detect Outputs)	PC Card Memory Mode	O	36, 67	These Card Detect pins are connected to ground on the PC Card. They are used by the host to determine that the PC Card is fully inserted into the socket.
	PC Card I/O Mode			This signal is same for all modes.
	True IDE Mode			This signal is same for all modes.
-IOWR (I/O Write Input)	PC Card Memory Mode	I	45	This signal is not used in this mode.
	PC Card I/O Mode			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the PC Card controller registers. The clocking will occur on the negative to positive going edge of the signal.
	True IDE Mode			This signal has the same function as in PC Card I/O Mode.
-IORD (I/O Read Input)	PC Card Memory Mode	I	44	This signal is not used in this mode.
	PC Card I/O Mode			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the PC Card.
	True IDE Mode			This signal has the same function as in PC Card I/O Mode.
-WE (Write Enable Input)	PC Card Memory Mode	I	15	This is a signal driven by the host and used for strobing memory write data to the registers of the PC Card. It is also used for writing the configuration registers.
	PC Card I/O Mode			In this mode, this signal is used to write the CIS and configuration registers.
	True IDE Mode ³			In this mode, this input signal is not used and should be connected to VCC by the host.
-OE (Output Enable Input)	PC Card Memory Mode	I	9	This is a strobe generated by the host interface. It is used to read data from the PC Card and to read the CIS and configuration registers.
	PC Card I/O Mode			This signal is used to read the CIS and configuration registers.
	True IDE Mode ³			To enable the True IDE Mode, this input should be grounded by the host.
-CE1,-CE2 (Card Enable Inputs)	PC Card Memory Mode	I	7, 42	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. CE2# always accesses the odd byte of the word. CE1# accesses the even byte or the odd byte of the word depending on A0 and CE2#. A multiplexing scheme based on A0, CE1#, CE2# allows 8 bit hosts to access all data on D0~D7.
	PC Card I/O Mode			This signal has the same function as in PC Card Memory Mode.

Signal Name	Mode of operation	Pin Type	Pin No(s).	Description
-CS0, -CS1 (Chip Select Inputs)	True IDE Mode			In the True IDE Mode, CS0# is the chip select for the task file registers while CS1# is used to select the Alternate Status Register and the Device Control Register.
WP (Write Protect / I/O Port 16 Output)	PC Card Memory Mode	O	33	The PC card does not have a WP switch. This signal is held low after reset initialization sequence.
IOIS16#	PC Card I/O Mode			A low signal indicates a 16 bit or odd byte only operation can be performed at the addressed port.
IOCS16#	True IDE Mode			In True IDE Mode this signal is asserted low when the card is expecting a word data transfer cycle.
GND (Ground)	PC Card Memory Mode	Power	1,34,35, 68	Ground Pins
	PC Card I/O Mode			This signal is same for all modes.
	True IDE Mode			This signal is same for all modes.
Vcc	PC Card Memory Mode	Power	17, 51	Power Supply Pin (5.0V/3.3V).
	PC Card I/O Mode			This signal is same for all modes.
	True IDE Mode			This signal is same for all modes.
RESET (Card Reset Input)	PC Card Memory Mode	I	58	When this pin is high, this signal resets the Flash Card. The card Reset is only at power up if this pin is left high or open from power-up. The card is also reset when the Soft Reset bit in the Card Configuration Option Register is set.
	PC Card I/O Mode			This signal has the same function as in PC Card Memory Mode.
-RESET	True IDE Mode			In this mode, this input pin is the active low from the host.
-REG (Attribute Memory Select Input)	PC Card Memory Mode	I	61	This signal is used during Memory Cycles to distinguish between Register (Attribute) Memory (REG# = low) and Common Memory (REG# = high).
	PC Card I/O Mode			This signal must be active low during I/O Cycles when the I/O address is on the Bus.
-DMACK (DMA Acknowledge)	True IDE Mode			This is a DMA Acknowledge signal that is asserted by the host in response to DMARQ to initiate DMA transfers. Note: This signal may be negated by the host to suspend the DMS transfer in process. For Multiword DMA transfers, the card may negate DMARQ with the tL specified time once the DMACK- is asserted and reasserted again at a later time to resume DMA operation. Alternatively, if the card is able to continue the data transfer, the card may leave DMARQ asserted and wait for the host to assert DMACK-.
RDY/BSY (Ready/Interrupt Request Output)	PC Card Memory Mode	O	16	In Memory Mode this signal is set high when the PC card is ready to accept a new data transfer operation and held low when the PC card is busy. The host memory card socket must have a pull-up resistor on this signal. At power up at Reset, RDY/BSY signal is held low (busy) until the PC card has completed its power up or reset function. No access of any type

Signal Name	Mode of operation	Pin Type	Pin No(s).	Description
				should be made of the PC card during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true: the PC card has been powered up with +RESET continuously disconnected or asserted.
-IREQ (Interrupt Request)	PC Card I/O Mode			In I/O mode, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (Interrupt Request)	True IDE Mode			In True IDE mode, the signal is active high Request to the host.
-INPACK (Input Port Acknowledge Output)	PC Card Memory Mode			This signal is not used in this mode.
	PC Card I/O Mode			This signal is asserted by the card when the card is selected and is responding to an I/O read cycle. This signal is used by the host to enable the input data buffers between the host and the card.
DMARQ¹	True IDE Mode	O	60	This signal is a DMA Request that is used for DMA data transfers between host and the PC card. The direction of data transfer is controlled by DIOR- and DIOW-. This signal is used in the handshake manner with DMACK- (i.e., the device waits until the host asserts DMACK- before negating DMARQ, and reasserting DMARQ if there is more data to transfer).
-CSEL (Cable Select Input)	PC Card Memory Mode			This signal is not used in this mode.
	PC Card I/O Mode			This signal is not used in this mode.
	True IDE Mode	I	56	This internally pulled up signal is used to configure this card as Master or Slave when configured in the True IDE Mode. When this pin is grounded, this PC card is configured as Master. When this pin is tied to VCC this card is configured as Slave.
-WAIT (Extend Bus Cycle/I/O Channel Ready Output) WAIT#	PC Card Memory Mode			This signal is driven low by the card to inform the host to delay completion of the cycle in progress.
	PC Card I/O Mode	O	59	This signal has the same function as in PC Card Memory Mode.
	True IDE Mode			This signal is negated to extend the host transfer cycle of any host register access (read or write) when the card is not ready to respond to a data transfer request. When not negated, the signal is in high-impedance state.
-VS1, -VS2 (Voltage Sense Outputs)	PC Card Memory Mode	O	43, 57	VS1# is grounded so that the Card's CIS can be read at 3.3V and VS2# is left open and reserved by PC card for a secondary voltage.
	PC Card I/O Mode			This signal is the same for all modes.
	True IDE Mode			This signal is the same for all modes.
D15~D0 (16-bit Data Input/Output)	PC Card Memory Mode	I/O	41,40, 39,38, 37,66,	These lines carry the Data, Commands, and Status Information between the host and the controller. D15 is the MSB of odd byte and D7 the MSB of even byte

Signal Name	Mode of operation	Pin Type	Pin No(s).	Description
Bus)			65,64,	in a Word Access.
	PC Card I/O Mode		6,5,4,	This signal has the same function as in PC Card Memory Mode.
	True IDE Mode		3,2,32, 31, 30	All task file operations occur in byte mode on D7~D0, while all data transfers are word (16-bit) accesses.
A10~A0 (Card Address Input Bus)	PC Card Memory Mode	I	8,11,12, 22,23, 24, 25,26, 27, 28,29	These addresses along with the REG# signal are used to select the following: the I/O port address registers within the card, the memory mapped port address registers, a byte in the CIS and Configuration Control and Status registers.
	PC Card I/O Mode			This signal has the same function as in PC Card Memory Mode.
A2~A0	True IDE Mode	I	27,28, 29	In this mode, only A2~A0 are used to select one of the eight Task File registers. All the remaining unused addresses should be grounded by the host.
BVD1 (Battery Voltage Detect Output)	PC Card Memory Mode	I/O	63	This signal is asserted high since the card does not contain a battery.
-STSCHG (Card Status Changed Output)	PC Card I/O Mode			This signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states. Its use is controlled through the Card Configuration and Status Registers.
-PDIAG (Passed Diagnostics Input/Output)	True IDE Mode			This signal is asserted by slave drive to indicate to master drive that it has completed diagnostics and is ready to provide status.
BVD2 (Battery Voltage Detect Output)	PC Card Memory Mode	O	62	This signal is asserted high since the card does not contain a battery.
-SPKR (Audio Waveform Output)	PC Card I/O Mode			This signal is asserted high since the card does not support audio.
-DASP (Drive Active/Drive 1 Preset Output)	True IDE Mode	I/O		This signal indicates that a drive is active or that a slave drive (Drive 1) is present.

4. Electrical Specification

Table 11, Table 12, and Table 13 defines all D.C. Characteristics for the Industrial Rugged PCMCIA ATA Card. Unless otherwise stated, a condition is as below Table 10:

Table 10: Electrical Condition

Commercial Grade SRAFxxxH-ACSC Series	Industrial Grade WRAFxxxH-AISI- Series
V _{cc} = 5V ±10%	V _{cc} = 5V ±10%
V _{cc} = 3.3V ± 10%	V _{cc} = 3.3V ± 10%
T _a = 0°C to 70°C	T _a = -40°C to 85°C

4.1. General DC Characteristics

4.1.1. Interface I/O at 5.0V

Table 11: Interface I/O at 5.0V

Symbol	Parameter	Min.	Max.	Units	Remark
V _{CC}	Power Supply	4.5	5.5	V	
V _{OH}	Output Voltage High Level	V _{CC} -0.8		V	
V _{OL}	Output Voltage Low Level		0.8	V	
V _{IH}	Input Voltage High Level	2.92		V	Schmitt trigger ¹
V _{IL}	Input Voltage Low Level		1.70	V	Schmitt trigger ¹
T _{OPR-W}	Operating temperature for wide grade	-40	+85	°C	
T _{OPR-S}	Operating temperature for standard grade	0	+70	°C	
T _{STG}	Storage temperature	-40	125	°C	
R _{PU}	Pull up resistance ²	50	73	kOhm	
R _{PD}	Pull down resistance	50	97	kOhm	

4.1.2. Interface I/O at 3.3V

Table 12: Interface I/O at 3.3V

Symbol	Parameter	Min.	Max.	Units	Remark
V _{OH}	Power Supply	2.97	3.63	V	
V _{OL}	Output Voltage High Level	V _{CC} -0.8		V	
V _{IH}	Output Voltage Low Level		0.8	V	
V _{IL}	Input Voltage High Level	2.05		V	Schmitt trigger ¹
V _{CC}	Input Voltage Low Level		1.25	V	Schmitt trigger ¹
T _{OPR-W}	Operating Temperature For Wide Grade	-40	+85	°C	
T _{OPR-S}	Operating Temperature For Standard Grade	0	+70	°C	
T _{STG}	Storage Temperature	-40	125	°C	
R _{PU}	Pull up resistance ²	52.7	141	kOhm	
R _{PD}	Pull down resistance	47.5	172	kOhm	

Notes:

- 1) Include CE1, CE2, HREG, HOE, HIOE, HWE, HIOW pins.
- 2) Include CE1, CE2, HREG, HOE, HIOE, HWE, HIOW, CSEL, PDIAG, DASP pins.

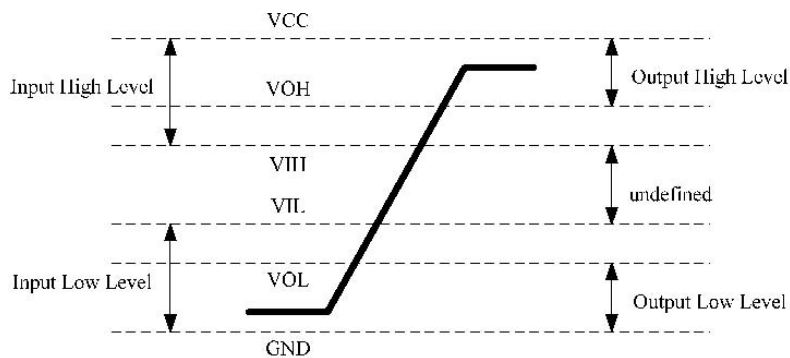


Figure 5: Interface I/O Voltage Diagram

4.2. AC Characteristics

4.2.1. Attribute Memory Read Timing

Table 13: Attribute Memory Read Timing

Speed Version	Symbol	300 ns	
Item		Min ns.	Max ns.
Read Cycle Time	t_c (R)	300	
Address Access Time	t_a (A)		300
Card Enable Access Time	t_a (CE)		300
Output Enable Access Time	t_a (OE)		150
Output Disable Time from CE	t_{dis} (CE)		100
Output Disable Time from OE	t_{dis} (OE)		100
Address Setup Time	t_{su} (A)	30	
Output Enable Time from CE	t_{en} (CE)	5	
Output Enable Time from OE	t_{en} (OE)	5	
Data Valid from Address Change	t_v (A)	0	

Notes: All times are in nanoseconds. HD signifies data provided by the PCMCIA ATA Card to the system. The CEx signal or both the HOE signal and the HWE signal shall be de-asserted between consecutive cycle operations.

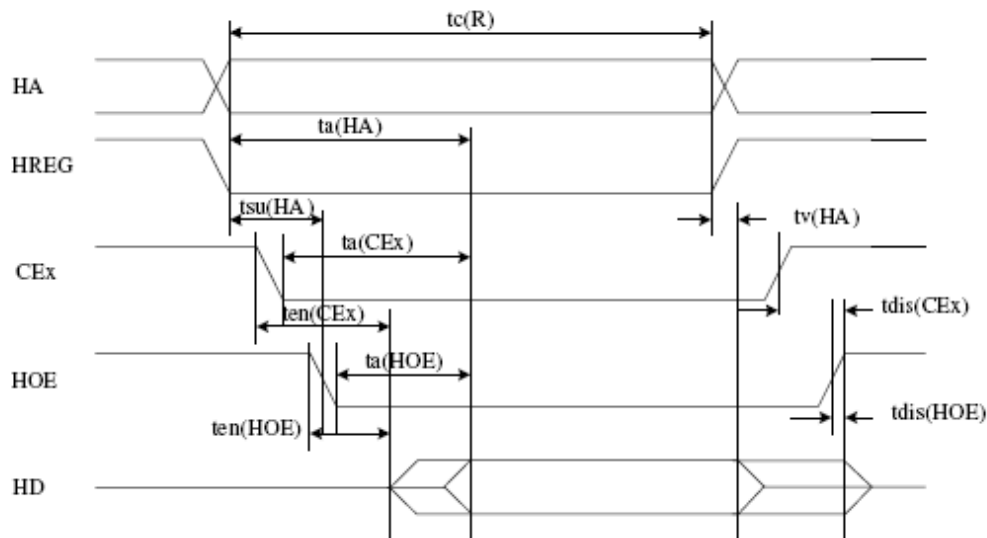


Figure6: Attribute Memory Read Timing Diagram

4.2.2. Configuration Register (Attribute Memory) Write Time

Table 14: Configuration Register (Attribute Memory) Write Time

Speed Version	Symbol	250 ns	
Item		Min ns.	Max ns.
Write Cycle Time	tc (W)	250	
Write Pulse Width	tw (WE)	150	
Address Setup Time	tsu (A)	30	
Write Recovery Time	trec (WE)	30	
Data Setup Time for HWE	tsu (D-WEH)	80	
Data Hold Time	th (D)	30	

Notes: All times are in nanoseconds. HD signifies data provided by the system to the PCMCIA ATA Card.

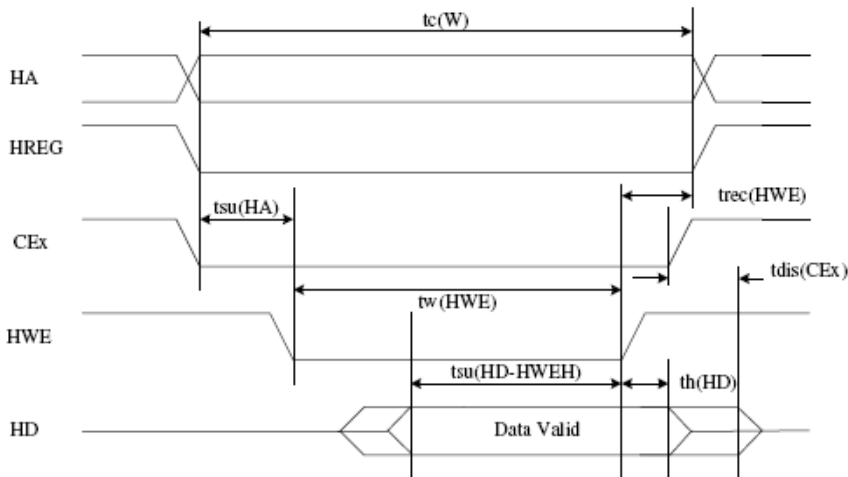


Figure 7: Configuration Register (Attribute Memory) Write Timing Diagram

4.2.3. Common Memory Read Timing

Table 15: Common Memory Read Timing

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Output Enable Access Time	ta (OE)		125		60		50		40
Output Disable Time from	tdis (OE)		100		60		50		40
Address Setup Time	tsu (A)	30		15		10		10	
Address Hold Time	th (A)	20		15		15		10	
CE Setup before OE	tsu (CE)	0		0		0		0	
CE Hold following OE	th (CE)	20		15		15		10	
Wait Delay Falling from OE	tv (WT-OE)		35		35		35		Na ¹
Data Setup for Wait Release	tv (WT)		0		0		0		Na ¹
Wait Width Time ²	tw (WT)		350		350		350		Na ¹

Notes:

- 1) IORDY is not supported in this mode
- 2) The Maximum load on IORDY is 1 LSTTL with 50pF (40pF below 120 nsec Cycle Time) total load. All times are in nanoseconds. HD signifies data provided by the PCMCIA ATA Card to the system. The IORDY signal may be ignored if the HOE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure.

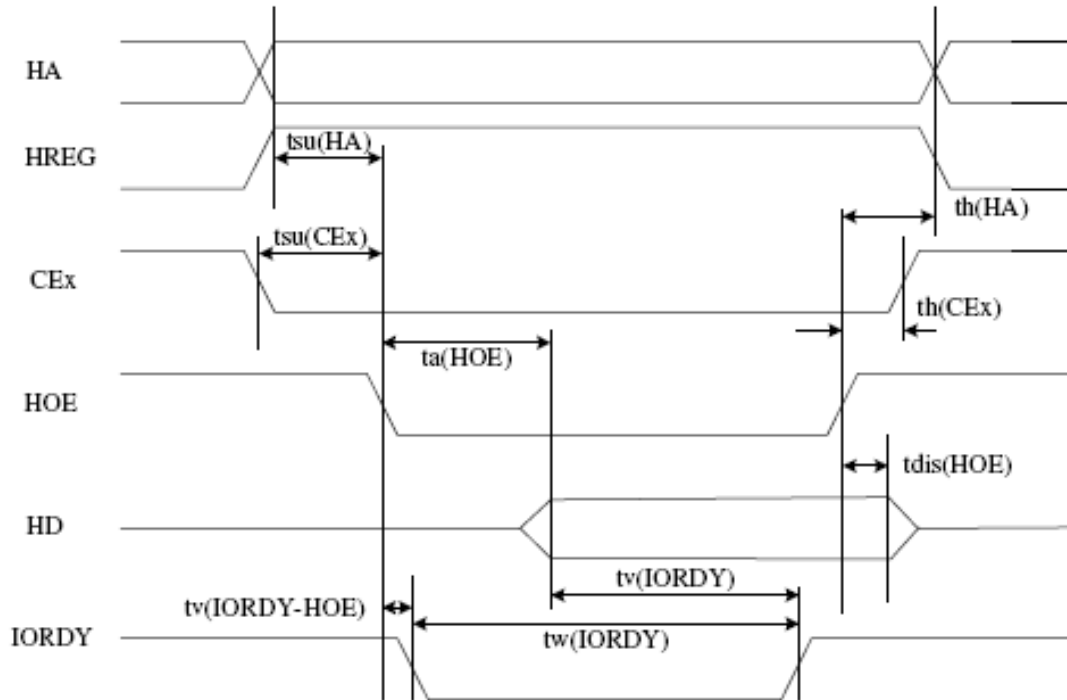


Figure 8: Common Memory Read Timing Diagram

4.2.4. Common Memory Write Timing

Table 15: Common Memory Write Timing

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Data Setup before WE	tsu (D-WEH)	80		50		40		30	
Data Hold following WE	th (D)	30		15		10		10	
WE Pulse Width	tw (WE)	150		70		60		55	
Address Setup Time	tsu (A)	30		15		10		10	
CE Setup before OE	tsu (CE)	0		0		0		0	
Write Recovery Time	trec (WE)	30		15		15		15	
Address Hold Time	th (A)	20		15		15		15	
CE Hold following OE	th (CE)	20		15		15		10	
Wait Delay Falling from OE	tv (WT-OE)		35		35		35		Na ¹
WE High from Wait Release	tv (WT)		0		0		0		Na ¹
Wait Width Time ²	tw (WT)		350		350		350		Na ¹

Notes:

- 1) IORDY is not supported in this mode
- 2) The Maximum load on IORDY is 1 LSTTL with 50pF (40pF below 120 nsec Cycle Time) total load. All times are in nanoseconds. HD signifies data provided by the PCMCIA ATA Card to the system. The IORDY signal may be ignored if the HOE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure.

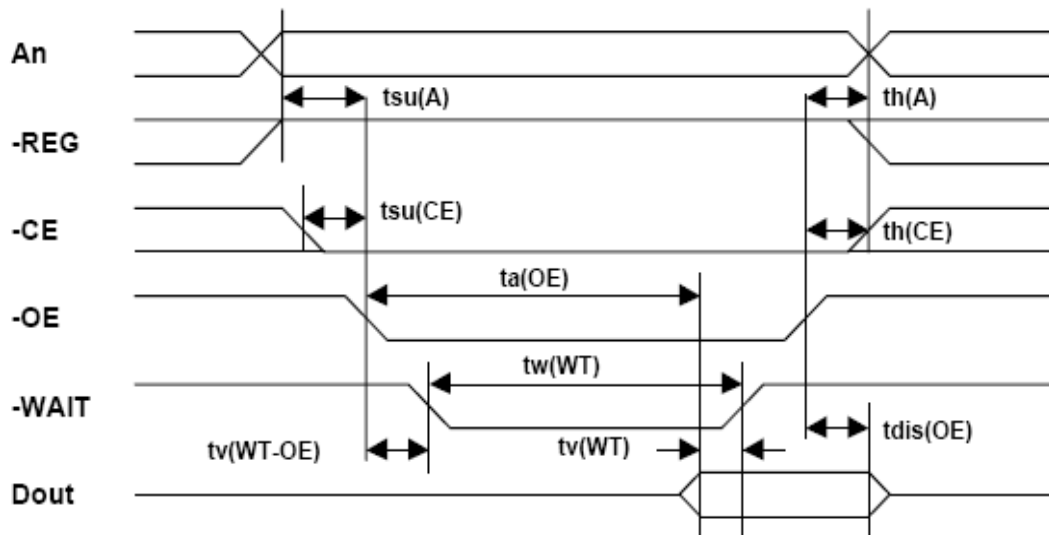


Figure 8: Common Memory Read Timing Diagram

4.2.5. I/O Read Timing

Table 16: I/O Read Timing

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Data Delay after IORD	td (IORD)		100		50		50		45
Data Hold following IORD	th (IORD)	0		5		5		5	
IORD Width Time	tw (IORD)	165		70		65		55	
Address Setup before IORD	tsuHA (IORD)	70		25		25		15	
Address Hold following IORD	thA (IORD)	20		10		10		10	
CE Setup before IORD	tsuCE (IORD)	5		5		5		5	
CE Hold following IORD	thCE (IORD)	20		10		10		10	
REG Setup before IORD	tsuREG(IORD)	5		5		5		5	
REG Hold following IORD	thREG (IORD)	0		0		0		0	
INPACK Delay Falling from IORD	tdFINPACK (IORD)	0	45	0	Na ¹	0	Na ¹	0	Na ¹
INPACK Delay Rising from IORD	tdrINPACK(IORD)		45		Na ¹		Na ¹		Na ¹
IOIS16 Delay Falling From Address	tdfIOIS16(ADR)		35		Na ¹		Na ¹		Na ¹
IOIS16 Delay Rising From Address	tdrIOIS16(ADR)		35		Na ¹		Na ¹		Na ¹
Wait Delay Falling From IORD	tdWT(IORD)		35		35		35		Na ²
Data Delay from Wait Rising	td(WT)		0		0		0		Na ²
Wait Width Time ²	tw(WT)		350		350		350		Na ²

Notes:1) -IOIS16 and -INPACK are not supported in this mode.

2) -WAIT is not supported in this mode.

3) Maximum load on -WAIT, -INPACK and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IORD high is 0 nsec, but minimum -IORD width shall still be met. Dout signifies data provided by the PCMCIA ATA Storage Card to the system. Wait Width time meets PCMCIA specification of 12µs but is intentionally less in this spec.

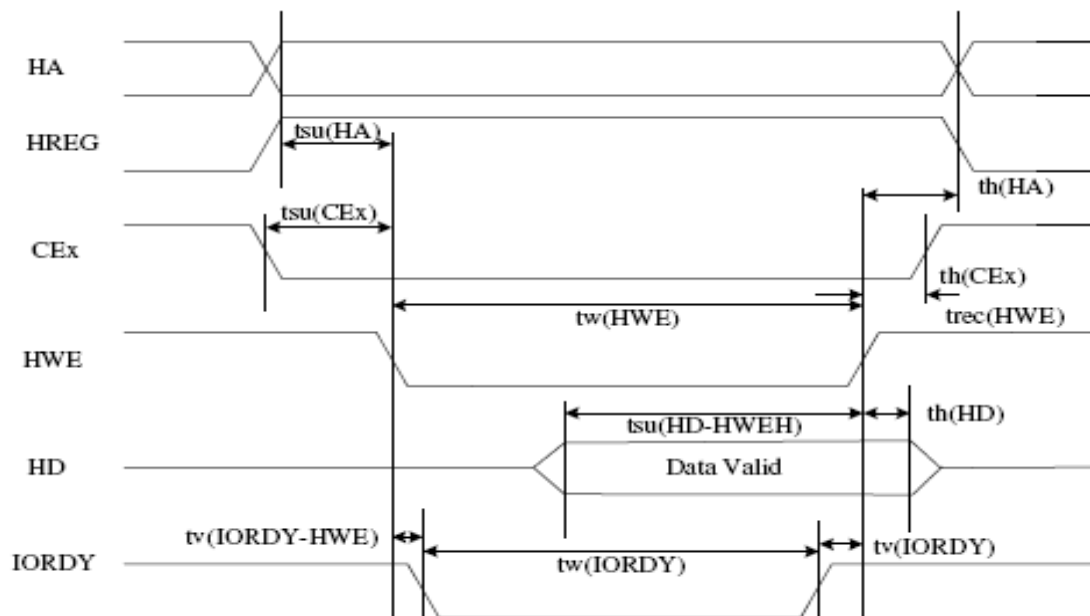


Figure 9: I/O Read Timing Diagram

4.2.6. I/O Write Timing

Table 17: I/O Write Timing

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Data Setup before IOWR	tsu (IOWR)	60		20		20		15	
Data Hold following IOWR	th (IOWR)	30		10		5		5	
IOWR Width Time	tw (IOWR)	165		70		65		55	
Address Setup before IOWR	tsuA (IOWR)	70		25		25		15	
Address Hold following IOWR	thA (IOWR)	20		20		10		10	
CE Setup before IOWR	tsuCE (IOWR)	5		5		5		5	
CE Hold following IOWR	thCE (IOWR)	20		20		10		10	
REG Setup before IOWR	tsuREG(IOWR)	5		5		5		5	
REG Hold following IOWR	thREG (IOWR)	0		0		0		0	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)		35		Na ¹		Na ¹		Na ¹
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)		35		Na ¹		Na ²		Na ²
Wait Delay Falling from IOWR	tdWT(IOWR)		35		35		Na ²		Na ²
IOWR High from Wait High ²	tdrIOWR(WT)	0		0		0			Na ²
Wait Width Time ²	tw(IORDY)		350		350		350		Na ¹

Notes: 1) -IOIS16 and -INPACK are not supported in this mode.

2) -WAIT is not supported in this mode.

3) The maximum load on -WAIT, -INPACK, and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IOWR high is 0 nsec, but minimum -IOWR width shall still be met.

Din signifies data provided by the system to the PCMCIA ATA Storage Card. The Wait Width time meets the PCMCIA specification of 12 μs but is intentionally less in this specification.

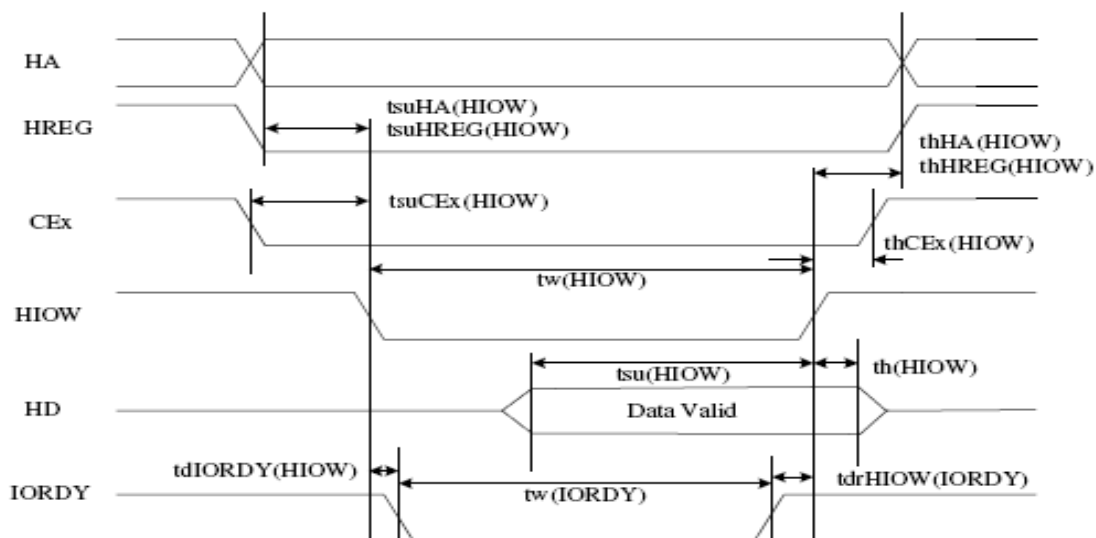


Figure 10: I/O Write Timing Diagram

4.2.7. True IDE PIO Mode Read/Write Timing

Table 18: True IDE PIO Mode Read/Write Timing

Item		Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
t0	Cycle time (min) ¹	600	383	240	180	120
t1	Address Valid to HIOR/HIOW setup (min)	70	50	30	30	25
t2	HIOR/HIOW (min) ¹	165	125	100	80	70
t2	HIOR/HIOW (min) Register (8 bit) ¹	290	290	290	80	70
t2i	HIOR/HIOW recovery time (min) ¹	-	-	-	70	25
t3	HIOW data setup (min)	60	45	30	30	20
t4	HIOW data hold (min)	30	20	15	10	10
t5	HIOR data setup (min)	50	35	20	20	20
t6	HIOR data hold (min)	5	5	5	5	5
t6Z	HIOR data tristate (max) ²	30	30	30	30	30
t7	Address valid to IOCS16 assertion (max) ⁴	90	50	40	n/a	n/a
t8	Address valid to IOCS16 released (max) ⁴	60	45	30	n/a	n/a
t9	HIOR/HIOW to address valid hold	20	15	10	10	10
tRD	Read Data Valid to IORDY active (min), if IORDY initially low after tA	0	0	0	0	0
tA	IORDY Setup time ³	35	35	35	35	35
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250
tC	IORDY assertion to release (max)	5	5	5	5	5

Notes:

All timings are in nanoseconds. The maximum load on IOCS16 is 1 LSTTL with a 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from IORDY high to HIOE high is 0 nsec, but minimum HIOE width shall still be met. (1) t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirement is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identify device data.

(2) This parameter specifies the time from the negation edge of HIOE to the time that the data bus is no longer driven by the device.

(3) The delay from the activation of HIOE or HIOW until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the device is not driving IORDY negated at tA after the activation of HIOE or HIOW, then t5 shall be met and tRD is not applicable. If the device is driving IORDY negated at the time tA after the activation of HIOE or HIOW, then tRD shall be met and t5 is not applicable. (4) t7 and t8 apply only to modes 0, 1 and 2. For other modes, this signal is not valid. (5) IORDY is not supported in this mode.

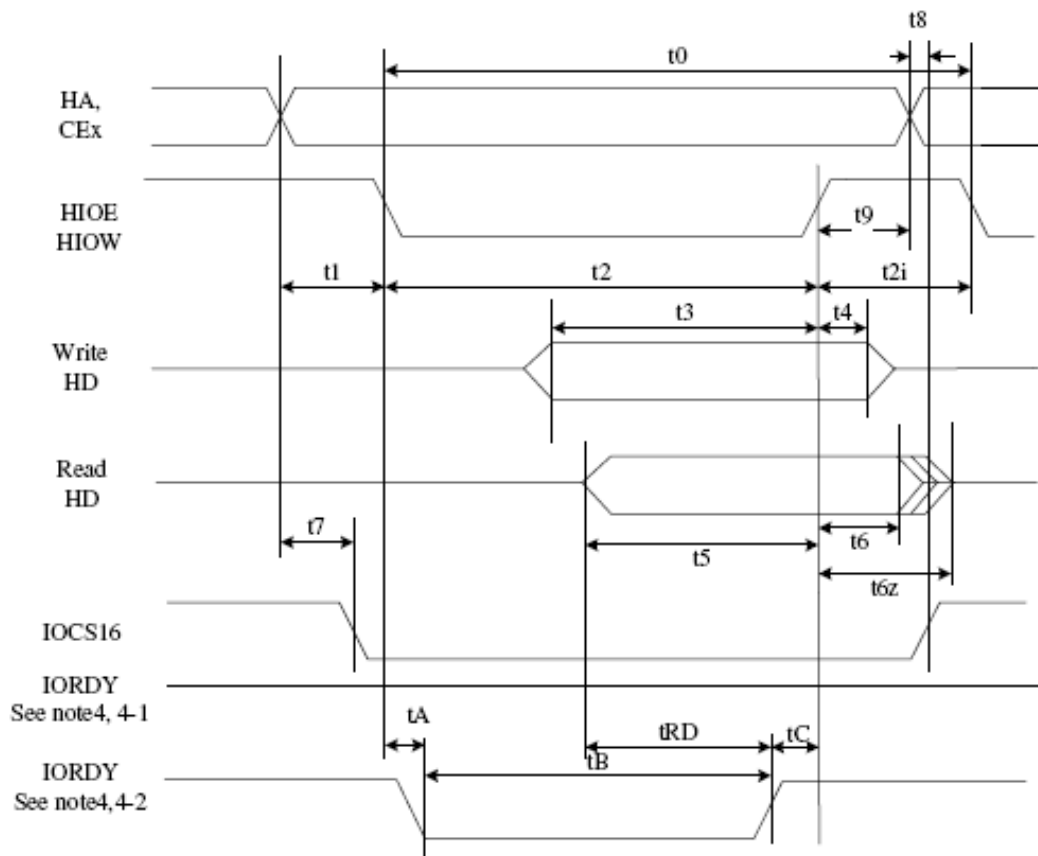


Figure 11: True IDE PIO Mode Read/Write Timing Diagram

Notes:

- 1) Device address consists of CE0, CE1, and HA [2:0]
- 2) Data consist of HD [15:00] (16-bit) or HD [7:0] (8-bit)
- 3) IOCS16 is shown for PIO modes 0, 1, and 2. For other modes, this signal is ignored.
- 4) The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of HIOE or HIOV. The assertion and negation of IORDY is described in the following three cases:
 - 4-1) Device never negates IORDY: No wait is generated.
 - 4-2) Device drives IORDY low before tA: wait generated. The cycle complete after IORDY is reasserted. For cycles where a wait is generated and HIOE is asserted, the device shall place read data on D15-D00 for tRD before causing IORDY to be asserted.

4.2.8. True IDE Multiword DMA Mode Read/Write Timing

Table 19: True IDE Multiword DMA Mode Read/Write Timing

Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Note	
t_0	Cycle time (min)	480	150	120	100	80	1
t_D	HIOR / HIOEW asserted width (min)	215	80	70	65	55	1
t_E	HIOR data access (max)	150	60	50	50	45	
t_F	HIOR data hold (min)	5	5	5	5	5	
t_G	HIOR/ HIOEW data setup (min)	100	30	20	15	10	
t_H	HIOEW data hold (min)	20	15	10	5	5	
t_I	DMACK(HREG) to HIOR/HIOEW setup (min)	0	0	0	0	0	
t_J	HIOR / HIOEW to -DMACK hold (min)	20	5	5	5	5	
t_{KR}	HIOR negated width (min)	50	50	25	25	20	1
t_{KW}	HIOEW negated width (min)	215	50	25	25	20	1
t_{LR}	HIOR to DMARQ delay (max)	120	40	35	35	35	
t_{LW}	HIOEW to DMARQ delay (max)	40	40	35	35	35	
t_M	CS1 CS0 valid to HIOR / HIOEW	50	30	25	10	5	
t_N	CS1 CS0 hold	15	10	10	10	10	
t_Z	DMACK-	20	25	25	25	25	

Notes: t_0 is the minimum total cycle time and t_D is the minimum command active time, while t_{KR} and t_{KW} are the minimum command recovery time or command inactive time for input and output cycles respectively. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0 , t_D , t_{KR} , and t_{KW} shall be met. The minimum total cycle time requirement is greater than the sum of t_D and t_{KR} or t_{KW} for input and output cycles respectively. This means a host implementation can lengthen either or both of t_D and either of t_{KR} , and t_{KW} as needed to ensure that t_0 is equal to or greater than the value reported in the device's identify device data. A device implementation shall support any legal host implementation.

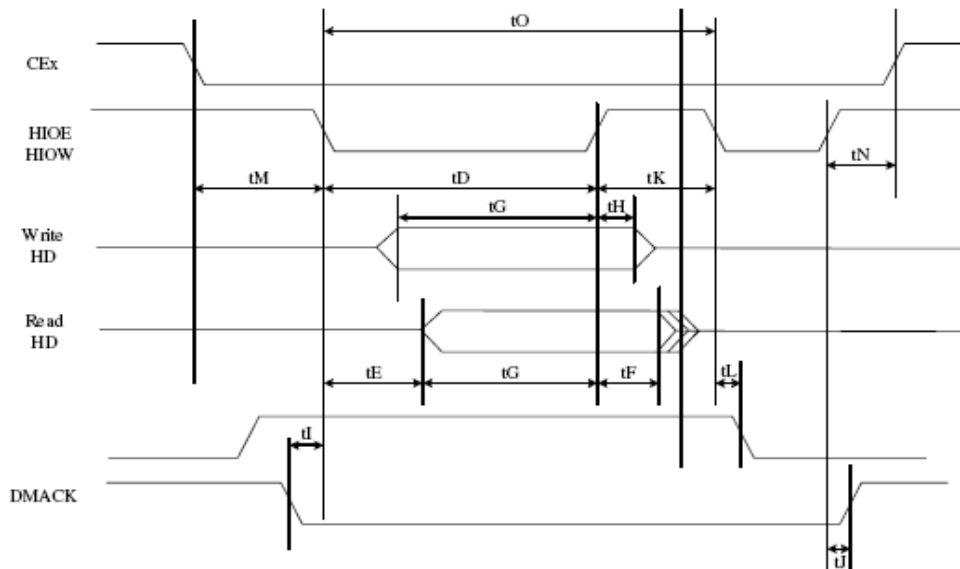


Figure 12: True IDE Multiword DMA Mode Read/Write Timing Diagram

Notes:

- 1) If the PCMCIA ATA Card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of a DMA transfer cycle to suspend the DMA transfers in progress and reassert the signal at a later time to continue the DMA operation.
- 2) This signal may be negated by the host to suspend the DMA transfer in progress.

4.2.9. Ultra DMA Signal in Each Interface Mode

Table 20: Ultra DMA Signal in True IDE Mode

Signal	Type	(Non UDMA Memory Mode)	PC Card Memory Mode UDMA	PC Card IO Mode UDMA	TRUE IDE MODE UDMA
DMARQ	Output	(-INPACK)	-DMARQ	-DMARQ	DMARQ
HREG	Input	(-REG)	-DMARQ	DMARQ	-DMARQ
HIOW	Input	(-IOWR)	STOP ¹	STOP ¹	STOP ¹
HIOE	Input	(-IORD)	-HDMARDY(R) ^{1,2} HSTROBE(W) ^{1,3,4}	-HDMARDY(R) ^{1,2} HSTROBE(W) ^{1,3,4}	-HDMARDY(R) ^{1,2} HSTROBE(W) ^{1,3,4}
IORDY	Output	(-WAIT)	-DDMARDY(W) ^{1,3} DSTROBE(R) ^{1,2,4}	-DDMARDY(W) ^{1,3} DSTROBE(R) ^{1,2,4}	-DDMARDY(W) ^{1,3} DSTROBE(R) ^{1,2,4}
HD [15:00]	Bidir	(D [15:00])	D [15:00]	D [15:00]	D [15:00]
HA [10:00]	Input	(A [10:00])	A [10:00] ⁵	A [10:00] ⁵	A [02:00] ⁵
CSEL	Input	(-CSEL)	-CSEL	-CSEL	-CSEL
HIRQ	Output	(READY)	READY	-INTRQ	INTRQ
CE1 CE2	Input	(-CE1) (-CE2)	-CE1 -CE2	-CE1 -CE2	-CS0 -CS1

Notes:

- 1) The UDMA interpretation of this signal is valid only during an Ultra DMA data burst.
- 2) The UDMA interpretation of this signal is valid only during an Ultra DMA data burst during a DMA Read command.
- 3) The UDMA interpretation of this signal is valid only during an Ultra DMA data burst during a DMA Write command.
- 4) The HSTROBE signals are active on both the rising and the falling edge.
- 5) Address lines 03 through 10 are not used in True IDE mode.

4.2.10. Ultra DMA Data Burst Timing Requirement

Table 21: Ultra DMA Data Burst Timing Requirement

Name	UDMA Mode 0		UDMA Mode 1		UDMA Mode 2		UDMA Mode 3		UDMA Mode 4		Measure Location2 (See Note 2)
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t2CYCTYP	240		160		120		90		60		Sender
tCYC	112		73		54		39		25		Note3
t2CYC	230		153		115		86		57		Sender
tDS	15.0		10.0		7.0		7.0		5.0		Recipient
tDH	5.0		5.0		5.0		5.0		5.0		Recipient
tDVS	70.0		48.0		31.0		20.0		6.7		Sender
tDVH	6.2		6.2		6.2		6.2		6.2		Sender
tCS	15.0		10.0		7.0		7.0		5.0		Device
tCH	5.0		5.0		5.0		5.0		5.0		Device
tCVS	70.0		48.0		31.0		20.0		6.7		Host
tCVH	6.2		6.2		6.2		6.2		6.2		Host
tZFS	0		0		0		0		0		Device
tDZFS	70.0		48.0		31.0		20.0		6.7		Sender
tFS		230		200		170		130		120	Device
tLI	0	150	0	150	0	150	0	100	0	100	Note4
tMLI	20		20		20		20		20		Host
tUI	0		0		0		0		0		Host
tAZ		10		10		10		10		10	Note5
tZAH	20		20		20		20		20		Host
tZAD	0		0		0		0		0		Device
tENV	20	70	20	70	20	70	20	55	20	55	Host
tRFS		75		70		60		60		60	Sender
tRP	160		125		100		100		100		Recipient
tIORDYZ		20		20		20		20		20	Device
tZIORDY	0		0		0		0		0		Device
tACK	20		20		20		20		20		Host
tSS	50		50		50		50		50		Sender

Notes: All Timings in ns

- 1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.
- 2) All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of tRFS, both STROBE and -DMARDY transitions are measured at the sender connector.
- 3) The parameter tCYC shall be measured at the recipient's connector farthest from the sender.
- 4) The parameter tLI shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.
- 5) The parameter tAZ shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus to allow for a bus turnaround.
- 6) See the AC Timing requirements in 4.2.12. Ultra DMA AC Signal Requirements.

4.2.11. Ultra DMA Data Burst Timing Descriptions

Table 22: Ultra DMA Data Burst Timing Descriptions

Name	Comment	Notes
T2CYCTYP	Typical sustained average two cycle time	
tCYC	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t2CYC	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge next falling edge of STROBE)	
tDS	Data setup time at recipient (from data valid until STROBE edge)	2,5
tDH	Data hold time at recipient (from STROBE edge until data may become invalid)	2,5
tDVS	Data valid setup time at sender (from data valid until STROBE edge)	3
tDVH	Data valid hold time at sender (from STROBE edge until data may become invalid)	3
tCS	CRC word setup time at device	2
tCH	CRC word hold time device	2
tCVS	CRC word valid setup time at host (from CRC valid until -DMACK negation)	3
tCVH	CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid)	3
tZFS	Time from STROBE output released-to-driving until the first transition of critical timing.	
tDZFS	Time from data output released-to-driving until the first transition of critical timing.	
tFS	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
tLI	Limited interlock time	1
tMLI	Interlock time with minimum	1
tUI	Unlimited interlock time	1
tAZ	Maximum time allowed for output drivers to release (from asserted or negated)	
tZAH	Minimum delay time required for output	
tZAD	drivers to assert or negate (from released)	
tENV	Envelope time (from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)	
tRFS	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY)	
tRP	Ready-to-pause time (that recipient shall wait to pause after negating -DMARDY)	
tIORDYZ	Maximum time before releasing IORDY	
tZIORDY	Minimum time before driving IORDY	4
tACK	Setup and hold times for -DMACK (before assertion or negation)	
tSS	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	

Notes:

- (1) The parameters tUI, tMLI (in Figure 16: Ultra DMA Data-In Burst Device Termination Timing and Figure 17: Ultra DMA Data-In Burst Host Termination Timing), and tLI indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. tUI is an unlimited interlock that has no maximum time value. tMLI is a limited time-out that has a defined minimum. tLI is a limited time-out that has a defined maximum.
- (2) 80-conductor cabling shall be required in order to meet setup (tDS, tCS) and hold (tDH, tCH) times in modes greater than 2.
- (3) Timing for tDVS, tDVH, tCVS and tCVH shall be met for lumped capacitive loads of 15 and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.
- (4) For all timing modes the parameter tZIORDY may be greater than tENV due to the fact that the host has a pull-up on IORDY- giving it a known state when released.
- (5) The parameters tDS, and tDH for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for tDS and tDH for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.

4.2.12. Ultra DMA Sender and Recipient IC Timing Requirements

Table 23: Ultra DMA Sender and Recipient IC Timing Requirements

Name	UDMA Mode 0		UDMA Mode 1		UDMA Mode 2		UDMA Mode 3		UDMA Mode 4	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tDSIC	14.7		9.7		6.8		6.8		4.8	
tDHIC	4.8		4.8		4.8		4.8		4.8	
tDVSIC	72.9		50.9		33.9		22.6		9.5	
tDVHIC	9.0		9.0		9.0		9.0		9.0	
tDSIC	Recipient IC data setup time (from data valid until STROBE edge) (see note 2)									
tDHIC	Recipient IC data hold time (from STROBE edge until data may become invalid) (see note 2)									
tDVSIC	Sender IC data valid setup time (from data valid until STROBE edge) (see note 3)									
tDVHIC	Sender IC data valid hold time (from STROBE edge until data may become invalid) (see note 3)									

Notes:

- (1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.
- (2) The correct data value shall be captured by the recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at tDSIC and tDHIC timing (as measured through 1.5 V).
- (3) The parameters tDVSIC and tDVHIC shall be met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values.

4.2.13. Ultra DMA AC Signal Requirements

Table 24: Ultra DMA AC Signal Requirements

Name	Comment	Min [V/ns]	Max [V/ns]	Notes
SRISE	Rising Edge Slew Rate for any signal		1.25	1
SFALL	Falling Edge Slew Rate for any signal		1.25	1

Notes:

- (1) The sender shall be tested while driving an 18 inch long, 80 conductor cable with PVC insulation material. The signal under test shall be cut at a test point so that it has not trace, cable or recipient loading after the test point. All other signals should remain connected through to the recipient. The test point may be located at any point between the sender's series termination resistor and one half inch or less of conductor exiting the connector. If the test point is on a cable conductor rather than the PCB, an adjacent ground conductor shall also be cut within one half inch of the connector. The test load and test points should then be soldered directly to the exposed source side connectors. The test loads consist of a 15 pF or a 40 pF, 5%, 0.08 inch by 0.05 inch surface mount or smaller size capacitor from the test point to ground. Slew rates shall be met for both capacitor values. Measurements shall be taken at the test point using a <1 pF, >100 Kohm, 1 Ghz or faster probe and a 500 MHz or faster oscilloscope. The average rate shall be measured from 20% to 80% of the settled VOH level with data transitions at least 120 nsec apart. The settled VOH level shall be measured as the average output high level under the defined testing conditions from 100 nsec after 80% of a rising edge until 20% of the subsequent falling edge.

4.2.14. Ultra DMA Data-In Burst Initiation Timing

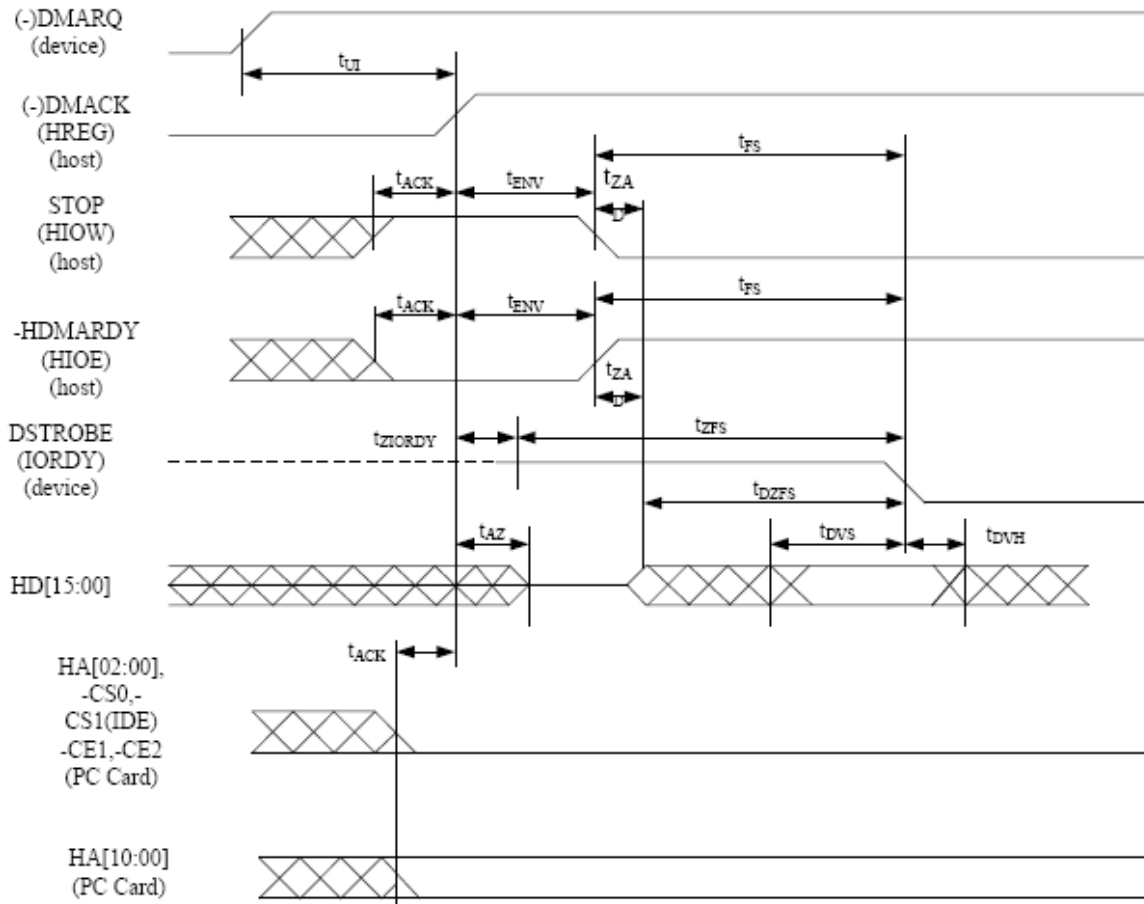


Figure 13: Ultra DMA Data-in Burst Initiation Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH.
 NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the IORDY:-DDMARDY: DSTROBE,-IORD:-HDMARDY: HSTROBE,
 and -IOWR:STOP signal lines are not in effect until DMARQ and -DMACK are asserted.
 HA [02:00] , -CS0 & -CS1 are True IDE mode signal definitions. HA [10:00] , -CE1 and -CE2
 are PC Card mode signals. The Bus polarity of (-) DMACK and (-) DMARQ are dependent
 on interface mode active.

4.2.15. Sustained Ultra DMA Data-In Burst Timing

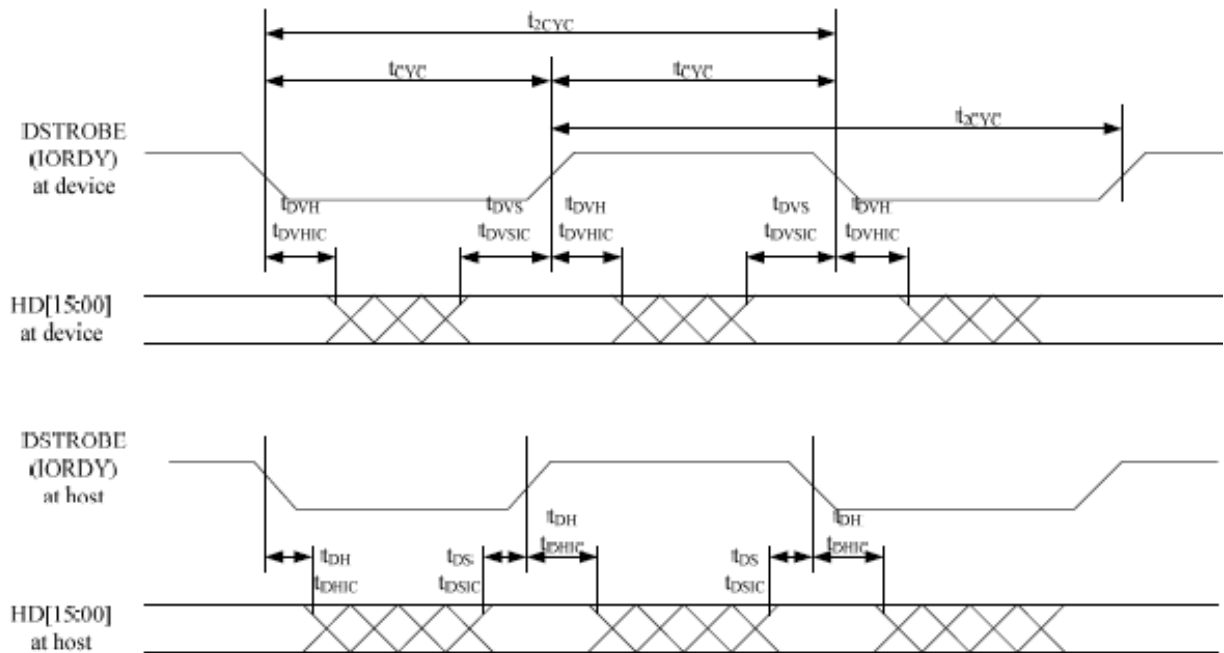


Figure 14: Sustained Ultra DMA Data-in Burst Initiation Timing Diagram

Note:

$\text{HD}[15:00]$ and $\overline{\text{DSTROBE}}$ signals are shown at both the host and the device to emphasize that cable setting time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

4.2.16. Ultra DMA Data-In Burst Host Pause Timing

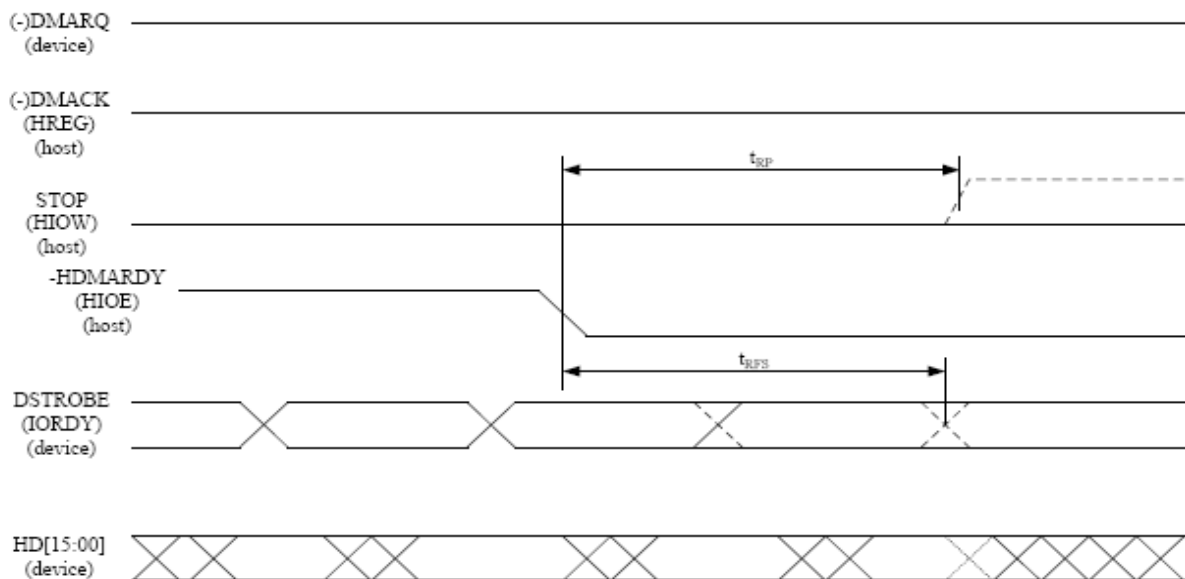


Figure 15: Ultra DMA Data-In Burst Host Pause Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes:

- (1) The host may assert STOP to request termination of the Ultra DMA data burst no sooner than t_{RP} after -HDMARDY is negated.
- (2) After negating -HDMARDY , the host may receive zero, one, two, or three more data words from the device.
- (3) The bus polarity of the (-) DMARQ and (-) DMACK signals is dependent on the active interface mode.

4.2.17. Ultra DMA Data-In Burst Device Termination Timing Diagram

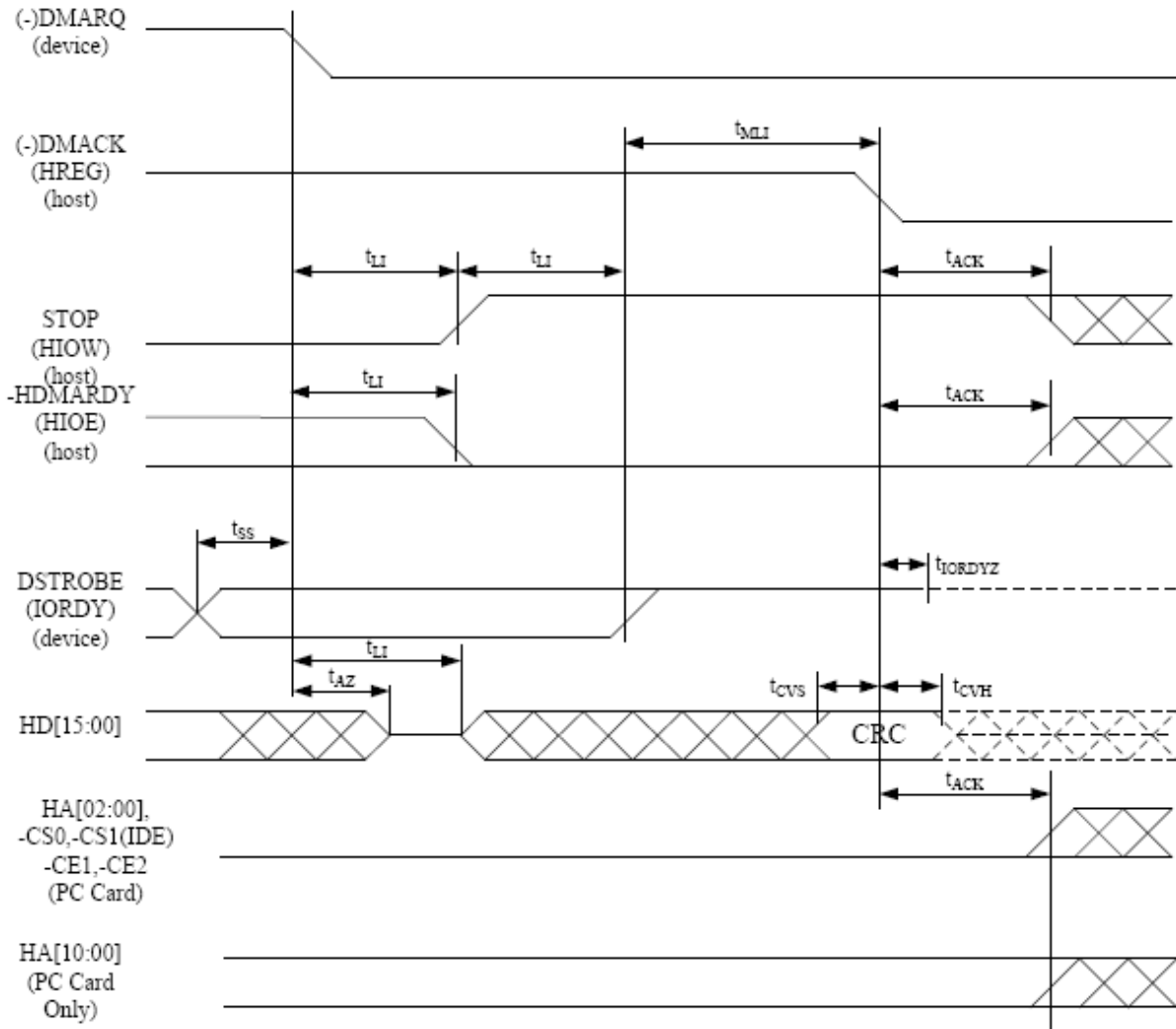


Figure 16: Ultra DMA Data-In Burst Device Termination Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. HA[02:00], -CS0 & -CS1 are True IDE mode signal definitions. HA[10:00], -CE1 and -CE2 are PC Card mode signals. The bus polarity of DMARQ and DMACK are dependent on the active interface mode.

4.2.18. Ultra DMA Data-In Burst Host Termination Timing

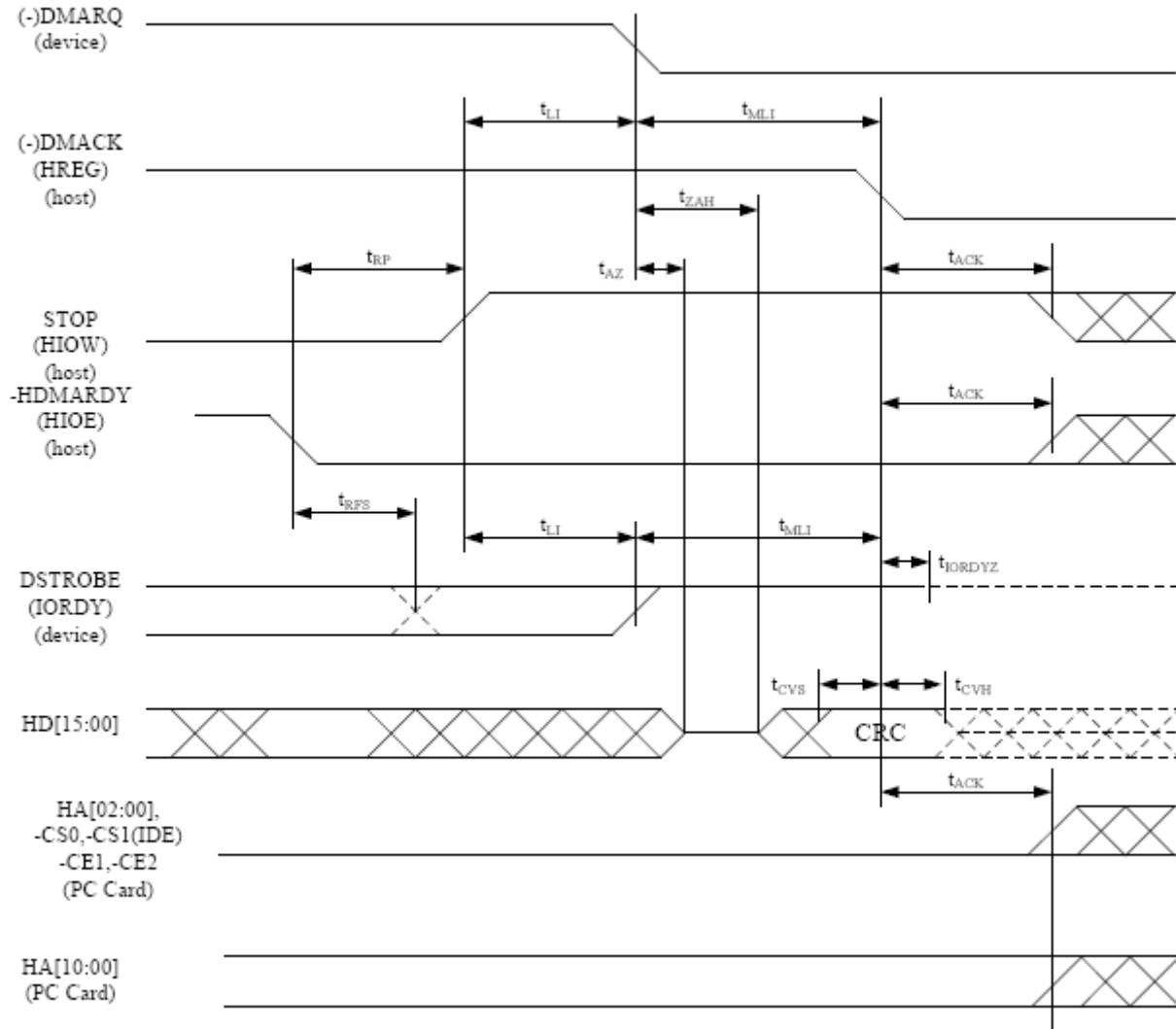


Figure 17: Ultra DMA Data-In Burst Host Termination Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. HA[02:00], -CS0 & -CS1 are True IDE mode signal definitions. HA[10:00], -CE1 and -CE2 are PC Card mode signals. The bus polarity of DMARQ and DMACK are dependent on the active interface mode.

4.2.20. Sustained Ultra DMA Data-Out Burst Host Initiation Timing

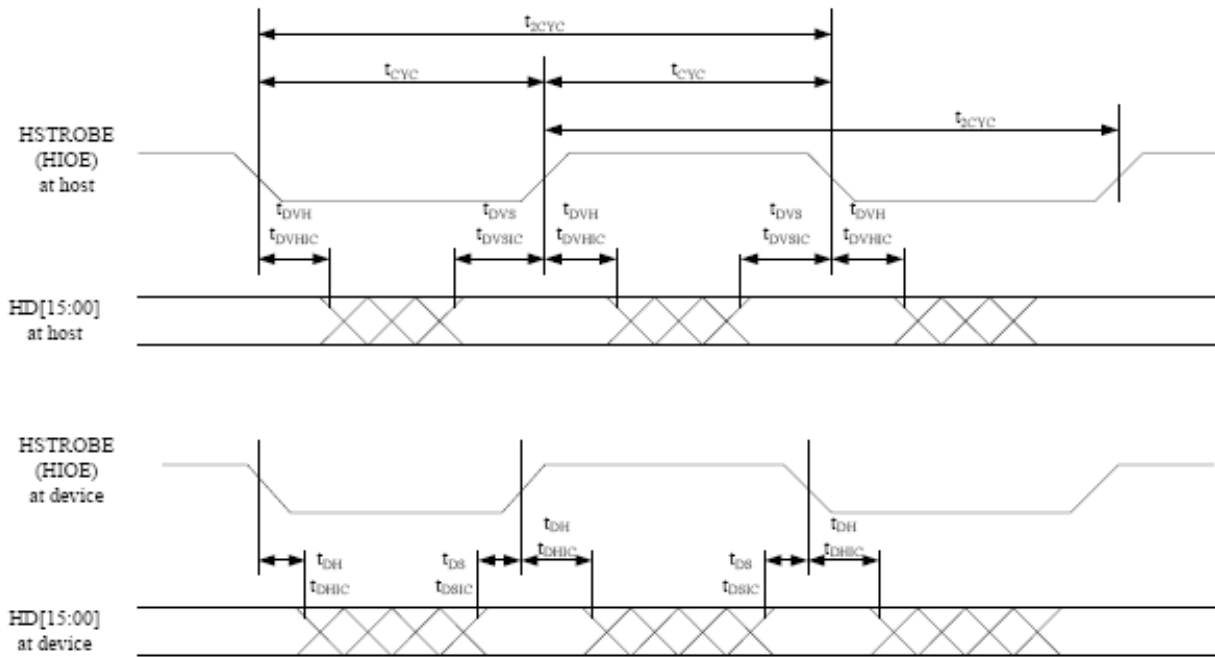


Figure 19: Sustained Ultra DMA Data-Out Burst Timing Diagram

Notes: Data (HD[15:00]) and HSTROBE signals are shown at both the device and the host to emphasize that cable setting time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until some time after they are driven by the host.

4.2.21. Ultra DMA Data-Out Burst Device Pause Timing

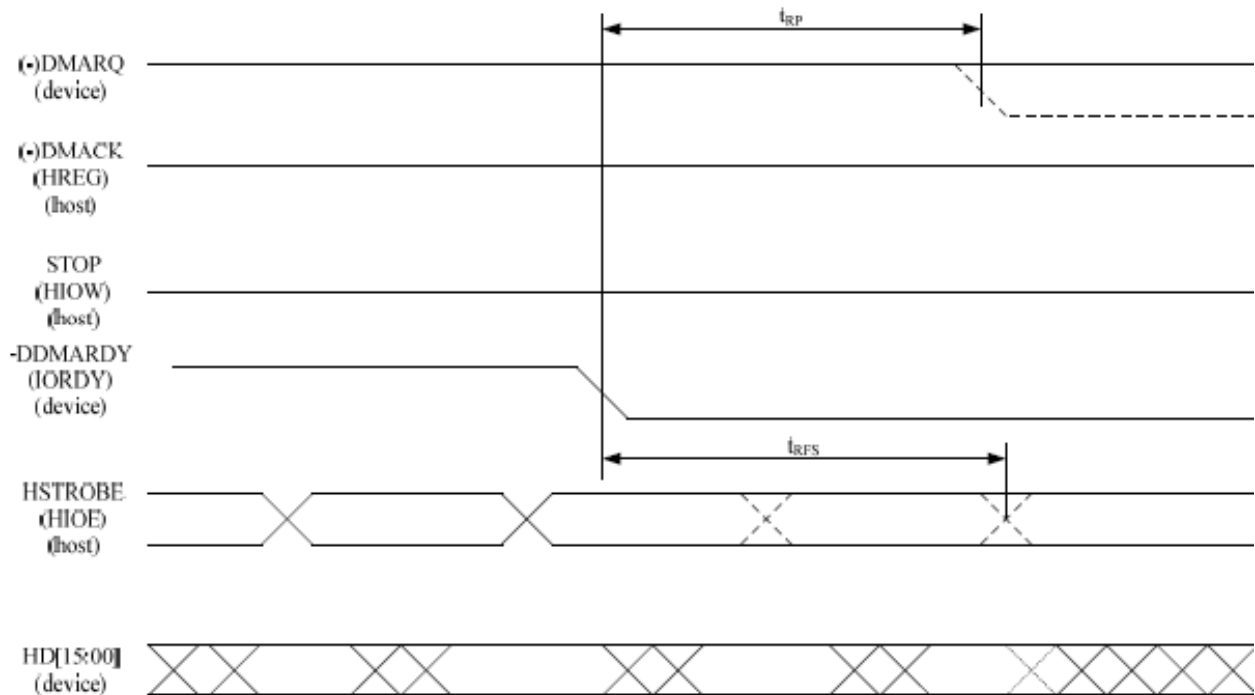


Figure 20: Ultra DMA Data-out Burst Device Pause Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

- Notes: (1) The device may negate DMARQ to request termination of the Ultra DMA data burst no sooner than t_{RP} after $-DDMARDY$, is negated.
- (2) After negating $-DDMARDY$, the device may receive zero, one, two, or three more data words from the host.
- (3) The bus polarity of DMARQ and DMACK depend on the active interface mode.

4.2.22. Ultra DMA Data-Out Burst Device Termination Timing

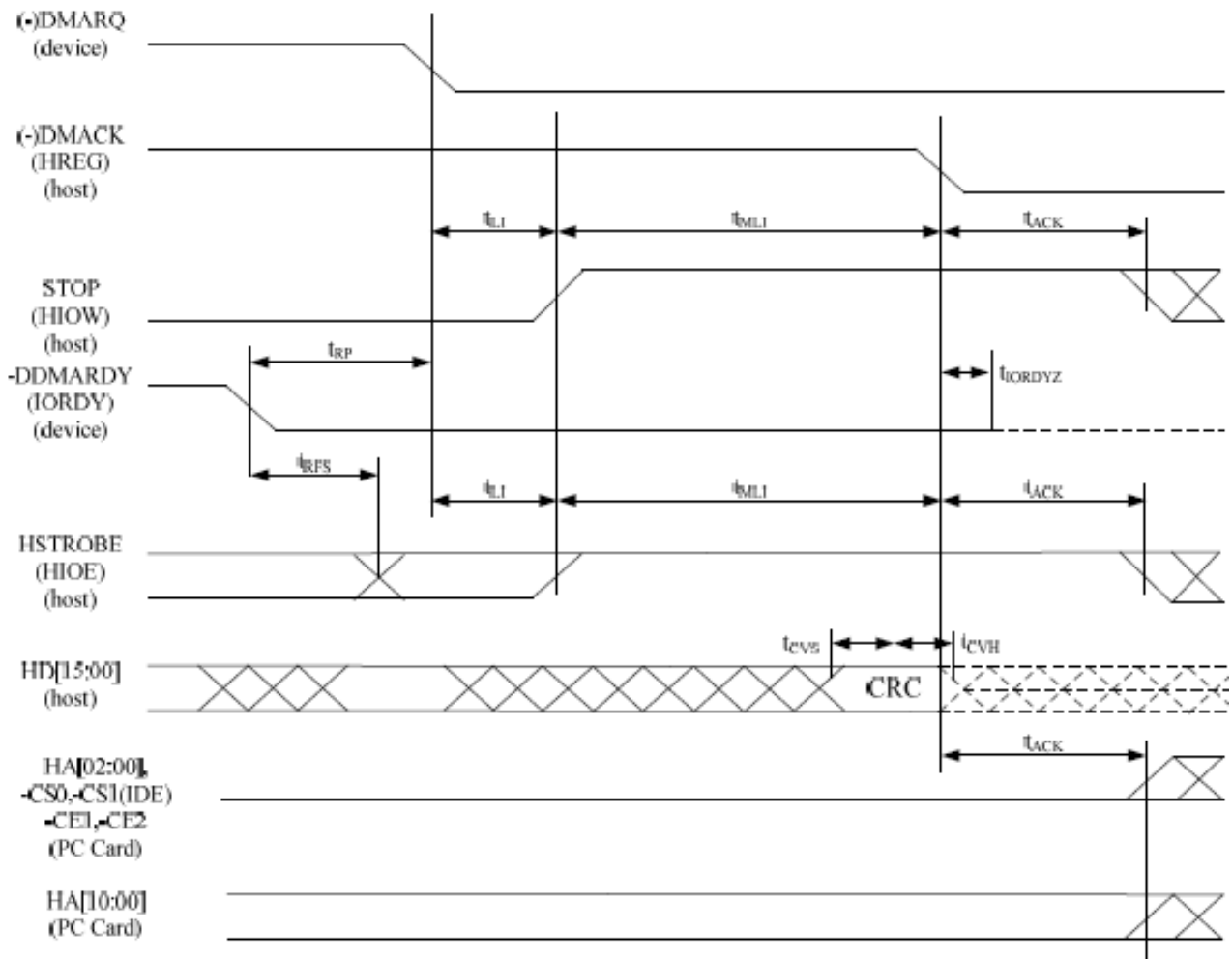


Figure 21: Ultra DMA Data-Out Burst Device Termination Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. HA[00:02], -CS0 & -CS1 are True IDE mode signal definitions. HA[00:10], -CE1 and -CE2 are PC Card mode signals. The bus polarity of DMARQ and DMACK are dependent on the active interface mode.

4.2.23. Ultra DMA Data-Out Burst Host Termination Timing

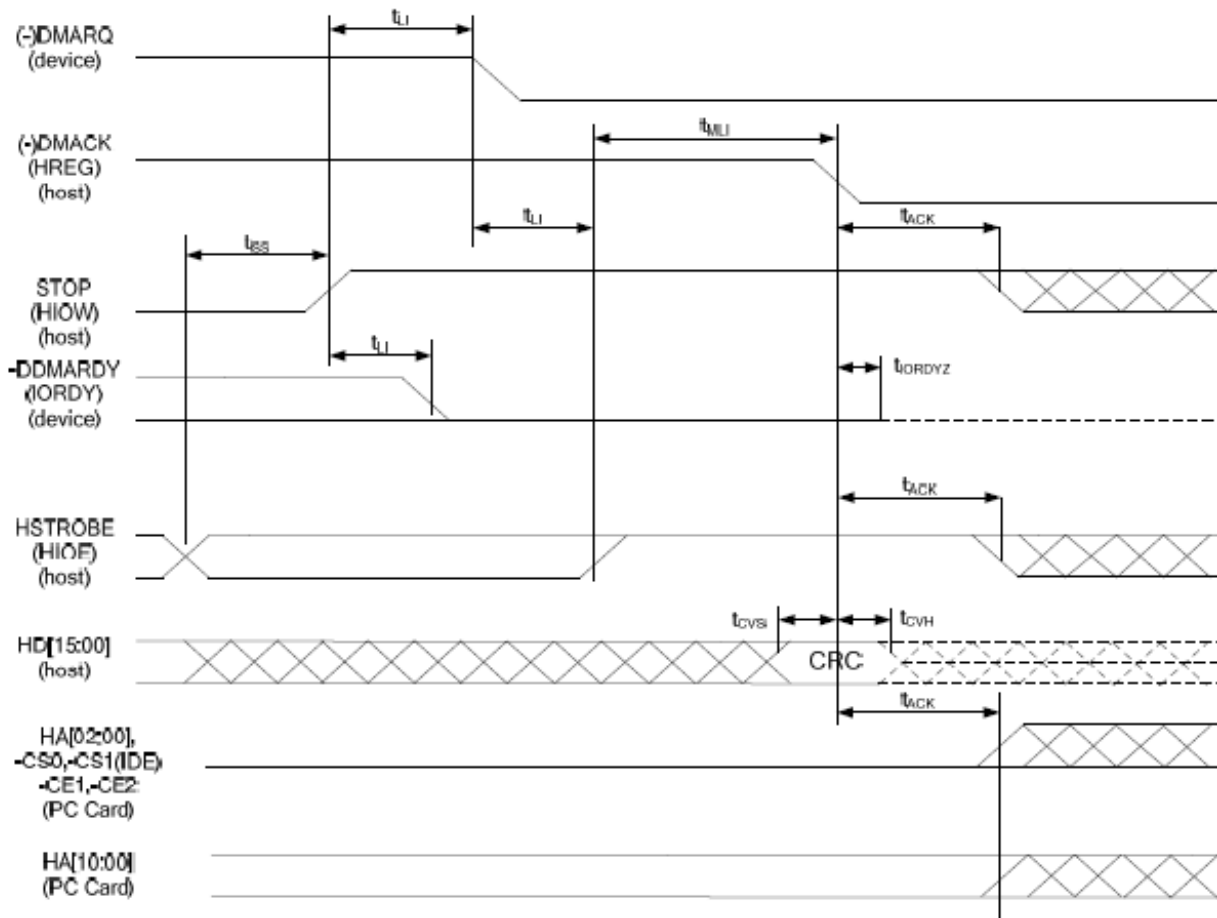


Figure 22: Ultra DMA Data-Out Burst Host Termination Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. HA[02:00], -CS0, -CS1 (IDE) and -CE1, -CE2 are PC Card mode signal definitions. HA[10:00], -CE1 and -CE2 are PC Card mode signal definitions. The bus polarity of DMARQ and DMACK are dependent on the active interface mode.

5. Interface Register Definition

5.1. Device Address

This controller receives commands from the host only when it is the selected device by checking the DEV bit in the Device Register.

This interface is for the host to program and perform commands and return status.

Table 25: Device Address Commands

CS1-	CS0-	A2	A1	A0	DMACK-	DIOR- = L	DIOW- = L
1	0	0	0	0	X	Data register	Data register
1	1	X	X	X	0	DMA Data RD	DMA Data Write
1	0	0	0	1	X	Error register	Feature register
1	0	0	1	0	X	Sector Count register	Sector Count register
1	0	0	1	1	X	LBA Low register	LBA Low register
1	0	1	0	0	X	LBA Mid register	LBA Mid register
1	0	1	0	1	X	LBA High register	LBA High register
1	0	1	1	0	X	Device register	Device register
1	0	1	1	1	X	Status register	Command register
0	1	1	1	0	X	Alt. Status register	Device Control register

5.2. I/O Register Descriptions

The Command Block registers are used for the host to send commands to this controller or for this controller to post status. These registers include the LBA High, LBA Mid, LBA Low, Device, Sector Count, Command, Status, Features, Error and Data Registers. The Control Block register is used for device control and to post alternate status. These registers include Device Control and Alternate Status registers.

For the detail field/bit description of every register, please refer to the ATAPI-5 specification.

(4) Alternate Status Register

This register contains the same information as the Status register in the Command Block.

(5) Command Register

This register contains the command code being sent. This controller begins immediately to execute the command after receipt of the command

(6) DMA Data Port

This port is only accessed for the host DMA data transfers when DMACK- and DMARQ are asserted. The data is 16-bits in width.

(7) Data Register

This register is accessed for the host PIO data transfer only when DRQ is set to one and DMACK– is not asserted. The contents of this register are not valid while it is in the Sleep mode. This register is 16 bits wide.

(8) Device Register

This register is for the host to set bit 4, DEV, of this register to select the device. Other bits in this register are command dependent.

(9) Device Control Register

This register allows the host to software reset attached devices and to enable or disable the assertion of the INTRQ signal by a selected device. When this register is written, the controller will respond to the write no matter the device is selected or not. And this controller will respond to the SRST bit when in the SLEEP mode.

(10) Error Register

At command completion of any command, the contents of this register are valid when the ERR bit is set to one in the Status register.

(11) Feature Register

This register is writing only. If this address is read by the host, the content read by the host will be the Error register.

The content of this register is command dependent.

(12) LBA High Register

This register contains the high order bits of logic block address and becomes a command parameter when Command register is written.

(13) LBA Low Register

This register contains the low order bits of logic block address and becomes a command parameter when Command register is written.

(14) LBA Mid Register

This register contains bit 15-8 of logic block address and becomes a command parameter when Command register is written.

(15) Sector Count Register

This register contains the numbers of sectors of data requested to be transferred on a read or write operation.

(16) Status Register

This register contains the device status. The contents of this register are updated to reflect the current state of the device.

6. Software Specification

6.1. ATA Command Description

This section defines the software requirements and the format of the commands the host sends to the PCMCIA ATA Flash Cards. Commands are issued to the PCMCIA ATA Flash Card by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command Register. The manner in which a command is accepted varies. There are three classes (see ATA Command Set) of command acceptance, all dependent on the host not issuing commands unless the PCMCIA ATA Flash Card Card is not busy (BSY=0). All commands listed in this specification shall be implemented.

Commands can be implemented as "no operation" to meet this requirement. The Security Mode feature set (command codes F1, F2, F3, F4, F5, and F6) should not be implemented unless the device is intended to be used in an embedded, non-removable application. The Security Mode feature set was not designed for removable devices and certain problems may be encountered when using these commands in a removable application. This specification introduces some new commands and features. If these commands are used on an older PCMCIA card, an Invalid Command Error may occur.

7. Upon receipt of a Class 1 command, the PCMCIA ATA Flash Card sets BSY within 400 nsec.
8. Upon receipt of a Class 2 command, the PCMCIA ATA Flash Card sets BSY within 400 nsec, sets up the sector buffer for a write operation, sets DRQ within 700 µsec, and clears BSY within 400 nsec of setting DRQ.
9. Upon receipt of a Class 3 command, the PCMCIA ATA Flash Card sets BSY within 400 nsec, sets up the sector buffer for a write operation, sets DRQ within 20 msec (assuming no re-assignments), and clears BSY within 400 nsec of setting DRQ.

6.2.1. ATA Command Set

The following table summarizes the ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 26: ATA Command Set

No	Command set	Supported2	Code	FR1	SC1	SN1	CY1	DR1	HD1	LBA1
1	Check Power Mode	Y	E5H or 98H	—	—	—	—	Y	—	—
2	Execute Drive Diagnostic	Y	90H	—	—	—	—	Y	—	—
3	Erase Sector(s)	Y	C0H	—	Y	Y	Y	Y	Y	Y
4	Flush Cache	—	E7	—	—	—	—	Y	—	—
5	Format Track	Y	50H	—	Y	—	Y	Y	Y	Y
6	Identify Drive	Y	ECH	—	—	—	—	Y	—	—
7	Idle	Y	E3H or 97H	—	Y	—	—	Y	—	—
8	Idle Immediate	Y	E1H or 95H	—	—	—	—	Y	—	—
9	Initialize Drive Parameters	Y	91H	—	Y	—	—	Y	Y	—
10	Key Management	—	B9H	C	C	C	C	C	Y	—
11	NOP	Y	00H	—	—	—	—	Y	—	—

No	Command set	Supported2	Code	FR1	SC1	SN1	CY1	DR1	HD1	LBA1
12	Read Buffer	Y	E4H	—	—	—	—	Y	—	—
13	Read DMA	Y	C8H	—	Y	Y	Y	Y	Y	Y
14	Read Long Sector	Y	22H,23H	—	—	Y	Y	Y	Y	Y
15	Read Multiple	Y	C4H	—	Y	Y	Y	Y	Y	Y
16	Read Sector(s)	Y	20H,21H	—	Y	Y	Y	Y	Y	Y
17	Read Verify Sector(s)	Y	40H,41H	—	Y	Y	Y	Y	Y	Y
18	Recalibrate	Y	1XH	—	—	—	—	Y	—	—
19	Request Sense	Y	03H	—	—	—	—	Y	—	—
20	Security Feature Set	—	F1H – F6H	—	—	—	—	Y	—	—
21	Seek	Y	7XH	—	—	Y	Y	Y	Y	Y
22	Set Features3	—	EFH	Y	C	—	—	Y	—	—
23	Set Multiple Mode	Y	C6H	—	Y	—	—	Y	—	—
24	Set Sleep Mode	Y	E6H or 99H	—	—	—	—	Y	—	—
25	Standby	Y	E2H or 96H	—	—	—	—	Y	—	—
26	Standby Immediate	Y	E0H or 94H	—	—	—	—	Y	—	—
27	Translate sector	Y	87H	—	Y	Y	Y	Y	Y	Y
28	Wear Level	Y	F5H	—	—	—	—	Y	Y	—
29	Write Buffer	Y	E8H	—	—	—	—	Y	—	—
30	Write DMA	Y	CAH	—	Y	Y	Y	Y	Y	Y
31	Write Long Sector	Y	32H or 33H	—	—	Y	Y	Y	Y	Y
32	Write Multiple	Y	C5H	—	Y	Y	Y	Y	Y	Y
33	Write Multiple w/o Erase	Y	CDH	—	Y	Y	Y	Y	Y	
34	Write Sector	Y	30H or 31H	—	Y	Y	Y	Y	Y	Y
35	Write Sector w/o Erase	Y	38H	—	Y	Y	Y	Y	Y	Y
36	Write Verify	Y	3CH	—	Y	Y	Y	Y	Y	Y

Note:

(1) FR: Feature Register

SC: Sector Count registers

SN: Sector Number register

CY: Cylinder Low/High register

DR: Drive bit of Drive/Head register

HD: Head No. (bit0-bit3) of Drive/Head register

LBA: Logical Block Address Mode Supported.

Y: Set up; —: Not set up; C: The register contains command specific data.

(2) Y: Supported; —: Not supported.

(3) For "Set Features" command, the controller supports all features listed in the PCMCIA ATA Flash™ Spec Revision 3.0.

(4) For the descriptions of all the command set, refer to PCMCIA ATA Flash™ Spec Revision 3.0.

6.2.1 Check Power Mode— 98H, E5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	98h or E5h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 28: Check Power Mode

This command checks the power mode.

If the PCMCIA ATA Flash Card is in, going to, or recovering from the sleep mode, the PCMCIA ATA Flash Card sets BSY, sets the Sector Count Register to 00h, clears BSY and generates an interrupt.

If the PCMCIA ATA Flash Card is in Idle mode, the PCMCIA ATA Flash Card sets BSY, sets the Sector Count Register to FFh, clears BSY and generates an interrupt.

6.2.2 Execute Drive Diagnostic— 90H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	90h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 29: Execute Drive Diagnostic

This command performs the internal diagnostic tests implemented by the PCMCIA ATA Flash Card.

When the diagnostic command is issued in a PCMCIA configuration mode, this command runs only on the PCMCIA ATA Flash Card that is addressed by the Drive/Head register. This is because PCMCIA card interface does not allow for direct inter-drive communication (such as the ATA PDIAG and DASP signals). When the diagnostic command is issued in the True IDE Mode, the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with status for both devices.

The Diagnostic codes shown in Table 39: Diagnostic Codes are returned in the Error Register at the end of the command.

Table 39: Diagnostic Codes

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controlling Microprocessor Error
8Xh	Slave Error in True IDE Mode

6.2.3. Erase Sector(s) – C0H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C0h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 30: Erase Sector

This command is used to pre-erase and condition data sectors in advance of a Write without Erase or Write Multiple without Erase command. There is no data transfer associated with this command but a Write Fault error status can occur.

6.2.4. Flush Cache – E7h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E7h							
C/D/H (6)	X				Drive	X		
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 31: Flush Cache

This command causes the card to complete writing data from its cache. The card returns status with RDY=1 and DSC=1 after the data in the write cache buffer is written to the media. If the Compact Flash Storage Card does not support the Flush Cache command, the Compact Flash Storage Card shall return command aborted.

6.2.5. Format Track – 50H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	50h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							

Sec Num (3)	X (LBA 7-0)
Sec Cnt (2)	Count (LBA mode only)
Feature (1)	X

Figure 32: Format Track

This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically FFh or 00h). To remain host backward compatible, the PCMCIA ATA Flash Card expects a sector buffer of data from the host to follow the command with the same protocol as the Write Sector(s) command although the information in the buffer is not used by the PCMCIA ATA Flash Card. If LBA=1 then the number of sectors to format is taken from the Sec Cnt register (0=256). The use of this command is not recommended.

6.2.6. Identify Drive— ECH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	ECh							
C/D/H (6)	X	X	X	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 33: Identify Device

The Identify Device command enables the host to receive parameter information from the PCMCIA ATA Flash Card. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 40. All reserved bits or words are zero. Hosts should not depend on Obsolete words in Identify Device containing 0.

Table 40: Identify Device Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	848Ah	2	General configuration - signature for the PCMCIA ATA Flash Card
	0XXX	2	General configuration – Bit Significant with ATA-4 definitions.
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4	0000h	2	Obsolete
5	0000h	2	Obsolete
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	XXXXh	2	Obsolete
10-19	aaaa	20	Serial number in ASCII (Right Justified)
20	0000h	2	Obsolete
21	0000h	2	Obsolete
22	0004h	2	Number of ECC bytes passed on Read/Write Long Commands
23-26	aaaa	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	aaaa	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word
47	XXXXh	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Reserved

Word Address	Default Value	Total Bytes	Data Field Type Information
49	XX00h	2	Capabilities
50	0000h	2	Reserved
51	0X00h	2	PIO data transfer cycle timing mode
52	0000h	2	Obsolete
53	000Xh	2	Field Validity
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW)
59	01XXh	2	Multiple sector setting
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Reserved
63	0X0Xh	2	Multiword DMA transfer. In PCMCIA mode this value shall be 0h
64	00XXh	2	Advanced PIO modes supported
65	XXXXh	2	Minimum Multiword DMA transfer cycle time per word. In PCMCIA mode this value shall be 0h
66	XXXXh	2	Recommended Multiword DMA transfer cycle time. In PCMCIA mode this value shall be 0h
67	XXXXh	2	Minimum PIO transfer cycle time without flow control
68	XXXXh	2	Minimum PIO transfer cycle time with IORDY flow control
69-79	0000h	20	Reserved
80-81	0000h	4	Reserved – ATA Flash cards do not return an ATA version
82-84	XXXXh	6	Features/command sets supported
85-87	XXXXh	6	Features/command sets enabled
88	XXXXh	2	Ultra DMA Mode Supported and Selected
89	XXXXh	2	Time required for Security erase unit completion
90	XXXXh	2	Time required for Enhanced security erase unit completion
91	XXXXh	2	Current Advanced power management value
92-127	0000h	72	Reserved
128	XXXXh	2	Security status
129-159	0000h	64	Vendor unique bytes
160	XXXXh	2	Power requirement description
161	0000h	2	Reserved for assignment by the CFA
162	0000h	2	Key management schemes supported
163	XXXXh	2	CF Advanced True IDE Timing Mode Capability and Setting
164	XXXXh	2	CF Advanced PCMCIA I/O and Memory Timing Mode Capability
165-175	0000h	22	Reserved for assignment by the CFA
176-255	0000h	140	Reserved

6.2.6.1 Word 0: General Configuration

This field indicates the general characteristics of the device. When Word 0 of the Identify drive information is 848Ah then the device is a PCMCIA ATA Flash Card and complies with the CFA specification and CFA command set. It is recommended that PCMCIA modes of operation report only the 848Ah value as they are always intended as removable devices.

Bits 15-0: CF Standard Configuration Value

Word 0 is 848Ah. This is the recommended value of Word 0.

Some operating systems require Bit 6 of Word 0 to be set to 1 (Non-removable device) to use the card as the root storage device. The Card must be the root storage device when a host completely replaces

conventional disk storage with a PCMCIA ATA Flash Card in True IDE mode. To support this requirement and provide capability for any future removable media Cards, alternate handling of Word 0 is permitted.

Bits 15-0: CF Preferred Alternate Configuration Values

044Ah: This is the alternate value of Word 0 turns on ATA device and turns off Removable Media and Removable Device while preserving all Retired bits in the word.

0040h: This is the alternate value of Word 0 turns on ATA device and turns off Removable Media and Removable Device while zeroing all Retired bits in the word

Bit 15-12: Configuration Flag

If bits 15:12 are set to 8h then Word 0 shall be 848Ah.

If bits 15:12 are set to 0h then Bits 11:0 are set using the definitions below and the Card is required to support for the CFA command set and report that in bit 2 of Word 83.

Bit 15:12 values other than 8h and 0h are prohibited.

Bits 11-8: Retired

These bits have retired ATA bit definitions. It is recommended that the value of these bits be either the preferred value of 0h or the value of 4h that preserves the corresponding bits from the 848Ah CF signature value.

Bit 7: Removable Media Device

If Bit 7 is set to 1, the Card contains media that can be removed during Card operation.

If Bit 7 is set to 0, the Card contains nonremovable media.

Bit 6: Not Removable Controller and/or Device

Alert! This bit will be considered for obsolescence in a future revision of this standard.

If Bit 6 is set to 1, the Card is intended to be nonremovable during operation.

If Bit 6 is set to 0, the Card is intended to be removable during operation.

Bits 5-0: Retired/Reserved

Alert! Bit 2 will be considered for definition in a future revision of this standard and shall be 0 at this time.

Bits 5-1 have retired ATA bit definitions.

Bit 2 shall be 0. Bit 0 is Reserved and shall be 0.

It is recommended that the value of bits 5-0 be either the preferred value of 00h or the value of 0Ah that preserves the corresponding bits from the 848Ah CF signature value.

6.2.6.2 Word 1: Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

6.2.6.3 Word 3: Default Number of Heads

This field contains the number of translated heads in the default translation mode.

6.2.6.4 Word 6: Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

6.2.6.5 Word 7-8: Number of Sectors per Card

This field contains the number of sectors per PCMCIA ATA Flash Card. This double word value is also

the first invalid address in LBA translation mode.

6.2.6.6. Word 10-19: Memory Card Serial Number

This field contains the serial number for this PCMCIA ATA Flash Card and is right justified and padded with spaces (20h).

6.2.6.7. Word 22: ECC Count

This field defines the number of ECC bytes used on each sector in the Read and Write Long commands. This value shall be set to 0004h.

6.2.6.8. Word 23-26: Firmware Revision

This field contains the revision of the firmware for this product.

6.2.6.9. Word 27-46: Model Number

This field contains the model number for this product and is left justified and padded with spaces (20h).

6.2.6.10. Word 47: Read/Write Multiple Sector Count

Bits 15-8 shall be the recommended value of 80h or the permitted value of 00h. Bits 7-0 of this word define the maximum number of sectors per block that the PCMCIA ATA Flash Card supports for Read/Write Multiple commands.

6.2.6.11. Word 49: Capabilities

Bit 13: Standby Timer

If bit 13 is set to 1 then the Standby timer is supported as defined by the IDLE command
If bit 13 is set to 0 then the Standby timer operation is defined by the vendor.

Bit 11: IORDY Supported

If bit 11 is set to 1 then this PCMCIA ATA Flash Card supports IORDY operation.
If bit 11 is set to 0 then this PCMCIA ATA Flash Card may support IORDY operation.

Bit 10: IORDY may be disabled

Bit 10 shall be set to 0, indicating that IORDY may not be disabled.

Bit 9: LBA supported

Bit 9 shall be set to 1, indicating that this PCMCIA ATA Flash Card supports LBA mode addressing.
CF devices shall support LBA addressing.

Bit 8: DMA Supported

If bit 8 is set to 1 then Read DMA and Write DMA commands are supported.
Bit 8 shall be set to 0. Read/Write DMA commands are not currently permitted on CF cards.

6.2.6.12 Word 51: PIO Data Transfer Cycle Timing Mode

The PIO transfer timing for each PCMCIA ATA Flash Card falls into modes that have unique parametric timing specifications. The value returned in Bits 15-8 shall be 00h for mode 0, 01h for mode 1, or 02h for mode 2. Values 03h through FFh are reserved.

6.2.6.13. Word 53: Translation Parameters Valid

Bit 0 shall be set to 1 indicating that words 54 to 58 are valid and reflect the current number of cylinders, heads and sectors. If bit 1 of word 53 is set to 1, the values in words 64 through 70 are valid. If this bit is cleared to 0, the values reported in words 64-70 are not valid. Any PCMCIA ATA Flash Card that supports PIO mode 3 or above shall set bit 1 of word 53 to one and support the fields contained in words 64 through 70.

6.2.6.14. Word 54-56: Current Number of Cylinders, Heads, Sectors/Track

These fields contain the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

6.2.6.15. Word 57-58: Current Capacity

This field contains the product of the current cylinders times heads times sectors.

6.2.6.16. Word 59: Multiple Sector Setting

Bits 15-9 are reserved and shall be set to 0.

Bit 8 shall be set to 1 indicating that the Multiple Sector Setting is valid.

Bits 7-0 are the current setting for the number of sectors that shall be transferred per interrupt on Read/Write Multiple commands.

6.2.6.17. Word 60-61: Total Sectors Addressable in LBA Mode

This field contains the total number of user addressable sectors for the PCMCIA ATA Flash Card in LBA mode only.

6.2.6.18. Word 63: : Multiword DMA Transfer

Bits 15 through 8 of word 63 of the Identify Device parameter information is defined as the Multiword DMA mode selected field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Only one of bits may be set to one in this field by the PCMCIA ATA Flash Card to indicate the multiword DMA mode which is currently selected.

Of these bits, bits 15 through 11 are reserved. Bit 8, if set to one, indicates that Multiword DMA mode 0 has been selected. Bit 9, if set to one, indicates that Multiword DMA mode 1 has been selected. Bit 10, if set to one, indicates that Multiword DMA mode 2 has been selected.

Selections of Multiword DMA modes 3 and above are specific to PCMCIA ATA Flash are reported in word 16.

Bits 7 through 0 of word 63 of the Identify Device parameter information is defined as the Multiword DMA data transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the PCMCIA ATA Flash Card to indicate the Multiword DMA modes it is capable of supporting.

Of these bits, bits 7 through 2 are reserved. Bit 0, if set to one, indicates that the PCMCIA ATA Flash Card supports Multiword DMA mode 0. Bit 1, if set to one, indicates that the PCMCIA ATA Flash Card supports Multiword DMA modes 1 and 0. Bit 2, if set to one, indicates that the PCMCIA ATA Flash Card

supports Multiword DMA modes 2, 1 and 0.

Support for Multiword DMA modes 3 and above are specific to PCMCIA ATA Flash are reported in word 163.

6.2.6.19. Word 64: Advanced PIO Transfer Modes Supported

Bits 7 through 0 of word 64 of the Identify Device parameter information is defined as the advanced PIO data transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the PCMCIA ATA Flash Card to indicate the advanced PIO modes it is capable of supporting.

Of these bits, bits 7 through 2 are reserved. Bit 0, if set to one, indicates that the PCMCIA ATA Flash Card supports PIO mode 3. Bit 1, if set to one, indicates that the PCMCIA ATA Flash Card supports PIO mode 4.

Support for PIO modes 5 and above are specific to PCMCIA ATA Flash are reported in word 163.

6.2.6.20. Word 65: Minimum Multiword DMA Transfer cycle time

Word 65 of the parameter information of the Identify Device command is defined as the minimum Multiword DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the PCMCIA ATA Flash Card guarantees data integrity during the transfer.

If this field is supported, bit 1 of word 53 shall be set to one. The value in word 65 shall not be less than the minimum cycle time for the fastest DMA mode supported by the device. This field shall be supported by all PCMCIA ATA Flash Cards supporting DMA modes 1 and above.

If bit 1 of word 53 is set to one, but this field is not supported, the Card shall return a value of zero in this field.

6.2.6.21. Word 66: Recommended Multiword DMA transfer cycle time

Word 66 of the parameter information of the Identify Device command is defined as the recommended Multiword DMA transfers cycle time. This field defines, in nanoseconds, the cycle time that, if used by the host, may optimize the data transfer from by reducing the probability that the PCMCIA ATA Flash Card will need to negate the DMARQ signal during the transfer of a sector.

If this field is supported, bit 1 of word 53 shall be set to one. The value in word 66 shall not be less than the value in word 65. This field shall be supported by all PCMCIA ATA Flash Cards supporting DMA modes 1 and above.

If bit 1 of word 53 is set to one, but this field is not supported, the Card shall return a value of zero in this field.

6.2.6.22. Word 67: Minimum PIO Transfer Cycle Time Without Flow Control

Word 67 of the parameter information of the Identify Device command is defined as the minimum PIO transfer without flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the PCMCIA ATA Flash Card guarantees data integrity during the transfer without utilization of flow control.

If this field is supported, Bit 1 of word 53 shall be set to one.

Any PCMCIA ATA Flash Card that supports PIO mode 3 or above shall support this field, and the value in word 67 shall not be less than the value reported in word 68.

If bit 1 of word 53 is set to one because a PCMCIA ATA Flash Card supports a field in words 64-70 other than this field and the PCMCIA ATA Flash Card does not support this field, the PCMCIA ATA Flash Card shall return a value of zero in this field.

6.2.6.23. Word 68: Minimum PIO Transfer Cycle Time With Flow Control

Word 68 of the parameter information of the Identify Device command is defined as the minimum PIO transfer with IORDY flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that the PCMCIA ATA Flash Card supports while performing data transfers while utilizing IORDY flow control.

If this field is supported, Bit 1 of word 53 shall be set to one.

Any PCMCIA ATA Flash Card that supports PIO mode 3 or above shall support this field, and the value in word 68 shall be the fastest defined PIO mode supported by the PCMCIA ATA Flash Card.

If bit 1 of word 53 is set to one because a PCMCIA ATA Flash Card supports a field in words 64-70 other than this field and the PCMCIA ATA Flash Card does not support this field, the PCMCIA ATA Flash Card shall return a value of zero in this field.

6.2.6.24. Words 82-84: Features/command sets supported

Words 82, 83, and 84 shall indicate features/command sets supported. The value 0000h or FFFFh was placed in each of these words by PCMCIA ATA Flash Cards prior to ATA-3 and shall be interpreted by the host as meaning that features/command sets supported are not indicated. Bits 1 through 13 of word 83 and bits 0 through 13 of word 84 are reserved. Bit 14 of word 83 and word 84 shall be set to one and bit 15 of word 83 and word 84 shall be cleared to zero to provide indication that the features/command sets supported words are valid. The values in these words should not be depended on by host implementers.

Bit 0 of word 82 shall be set to zero; the SMART feature set is not supported.

If bit 1 of word 82 is set to one, the Security Mode feature set is supported.

Bit 2 of word 82 shall be set to zero; the Removable Media feature set is not supported.

Bit 3 of word 82 shall be set to one; the Power Management feature set is supported.

Bit 4 of word 82 shall be set to zero; the Packet Command feature set is not supported.

If bit 5 of word 82 is set to one, write cache is supported.

If bit 6 of word 82 is set to one, look-ahead is supported.

Bit 7 of word 82 shall be set to zero; release interrupt is not supported.

Bit 8 of word 82 shall be set to zero; Service interrupt is not supported.

Bit 9 of word 82 shall be set to zero; the Device Reset command is not supported.

Bit 10 of word 82 shall be set to zero; the Host Protected Area feature set is not supported.

Bit 11 of word 82 is obsolete.

Bit 12 of word 82 shall be set to one; the PCMCIA ATA Flash Card supports the Write Buffer command.

Bit 13 of word 82 shall be set to one; the PCMCIA ATA Flash Card supports the Read Buffer command.

Bit 14 of word 82 shall be set to one; the PCMCIA ATA Flash Card supports the NOP command.

Bit 15 of word 82 is obsolete.

Bit 0 of word 83 shall be set to zero; the PCMCIA ATA Flash Card does not support the Download Microcode command.

Bit 1 of word 83 shall be set to zero; the PCMCIA ATA Flash Card does not support the Read DMA Queued and Write DMA Queued commands.

Bit 2 of word 83 shall be set to one; the PCMCIA ATA Flash Card supports the CFA feature set.

If bit 3 of word 83 is set to one, the PCMCIA ATA Flash Card supports the Advanced Power Management feature set.

Bit 4 of word 83 shall be set to zero; the PCMCIA ATA Flash Card does not support the Removable Media Status feature set.

6.2.6.25. Words 85-87: Features/command sets enabled

Words 85, 86, and 87 shall indicate features/command sets enabled. The value 0000h or FFFFh was placed in each of these words by PCMCIA ATA Flash Cards prior to ATA-4 and shall be interpreted by the host as meaning that features/command sets enabled are not indicated. Bits 1 through 15 of word 86 are reserved. Bits 0-13 of word 87 are reserved. Bit 14 of word 87 shall be set to one and bit 15 of word 87 shall be cleared to zero to provide indication that the Features / command sets enabled words are valid. The values in these words should not be depended on by host implementers.

Bit 0 of word 85 shall be set to zero; the SMART feature set is not enabled.

If bit 1 of word 85 is set to one, the Security Mode feature set has been enabled via the Security Set Password command.

Bit 2 of word 85 shall be set to zero; the Removable Media feature set is not supported.

Bit 3 of word 85 shall be set to one; the Power Management feature set is supported.

Bit 4 of word 85 shall be set to zero; the Packet Command feature set is not enabled.

If bit 5 of word 85 is set to one, write cache is enabled.

If bit 6 of word 85 is set to one, look-ahead is enabled.

Bit 7 of word 85 shall be set to zero; release interrupt is not enabled.

Bit 8 of word 85 shall be set to zero; Service interrupt is not enabled.

Bit 9 of word 85 shall be set to zero; the Device Reset command is not supported.

Bit 10 of word 85 shall be set to zero; the Host Protected Area feature set is not supported.

Bit 11 of word 85 is obsolete.

Bit 12 of word 85 shall be set to one; the PCMCIA ATA Flash Card supports the Write Buffer command.

Bit 13 of word 85 shall be set to one; the PCMCIA ATA Flash Card supports the Read Buffer command.

Bit 14 of word 85 shall be set to one; the PCMCIA ATA Flash Card supports the NOP command.

Bit 15 of word 85 is obsolete.

Bit 0 of word 86 shall be set to zero; the PCMCIA ATA Flash Card does not support the Download Microcode command.

Bit 1 of word 86 shall be set to zero; the PCMCIA ATA Flash Card does not support the Read DMA Queued and Write DMA Queued commands.

If bit 2 of word 86 shall be set to one, the PCMCIA ATA Flash Card supports the CFA feature set.

If bit 3 of word 86 is set to one, the Advanced Power Management feature set has been enabled via the Set Features command.

Bit 4 of word 86 shall be set to zero; the PCMCIA ATA Flash Card does not support the Removable Media Status feature set.

6.2.6.26. Word 88: Ultra DMA Modes Supported and Selected

Word 88 identifies the Ultra DMA transfer modes supported by the device and indicates the mode that is currently selected. Only one DMA mode shall be selected at any given time. If an Ultra DMA mode is selected, then no Multiword DMA mode shall be selected. If a Multiword DMA mode is selected, then no Ultra DMA mode shall be selected. Support of this word is mandatory if Ultra DMA is supported.

Bits 15-13: Reserved

Bit 12: 1 = Ultra DMA mode 4 is selected 0 = Ultra DMA mode 4 is not selected

Bit 11: 1 = Ultra DMA mode 3 is selected 0 = Ultra DMA mode 3 is not selected

Bit 10: 1 = Ultra DMA mode 2 is selected 0 = Ultra DMA mode 2 is not selected

Bit 9: 1 = Ultra DMA mode 1 is selected 0 = Ultra DMA mode 1 is not selected

Bit 8: 1 = Ultra DMA mode 0 is selected 0 = Ultra DMA mode 0 is not selected

Bits 7-5: Reserved

Bit 4: 1 = Ultra DMA mode 4 and below are supported. Bits 0-3 Shall be set to 1.

Bit 3: 1 = Ultra DMA mode 3 and below are supported, Bits 0-2 Shall be set to 1.

Bit 2: 1 = Ultra DMA mode 2 and below are supported. Bits 0-1 Shall be set to 1.

Bit 1: 1 = Ultra DMA mode 1 and below are supported. Bit 0 Shall be set to 1.

Bit 0: 1 = Ultra DMA mode 0 is supported

6.2.6.27. Word 89: Time required for Security erase unit completion

Word 89 specifies the time required for the Security Erase Unit command to complete. This command shall be supported on PCMCIA ATA Flash Cards that support security.

Value	Time
0	Value not specified
1-254	(Value * 2) minutes
255	>508 minutes

6.2.6.28. Word 90: Time required for Enhanced security erase unit completion

Word 90 specifies the time required for the Enhanced Security Erase Unit command to complete. This command shall be supported on PCMCIA ATA Flash Cards that support security.

Value	Time
0	Value not specified
1-254	(Value * 2) minutes
255	>508 minutes

6.2.6.29. Word 91: Advanced power management level value

Bits 7-0 of word 91 contain the current Advanced Power Management level setting.

6.2.6.30. Word 128: Security Status

Bit 8: Security Level

If set to 1, indicates that security mode is enabled and the security level is maximum.

If set to 0 and security mode is enabled, indicates that the security level is high.

Bit 5: Enhanced security erase unit feature supported

If set to 1, indicates that the Enhanced security erase unit feature set is supported.

Bit 4: Expire

If set to 1, indicates that the security count has expired and Security Unlock and Security Erase Unit are command aborted until a power-on reset or hard reset.

Bit 3: Freeze

If set to 1, indicates that the security is Frozen.

Bit 2: Lock

If set to 1, indicates that the security is locked.

Bit 1: Enable/Disable

If set to 1, indicates that the security is enabled.

If set to 0, indicates that the security is disabled.

Bit 0: Capability

If set to 1, indicates that PCMCIA ATA Flash Card supports security mode feature set.

If set to 0, indicates that PCMCIA ATA Flash Card does not support security mode feature set.

6.2.6.31. Word 160: Power Requirement Description

This word is required for PCMCIA ATA Flash Cards that support power mode 1.

Bit 15: VLD

If set to 1, indicates that this word contains a valid power requirement description.

If set to 0, indicates that this word does not contain a power requirement description.

Bit 14: RSV

This bit is reserved and shall be 0.

Bit 13: -XP

If set to 1, indicates that the PCMCIA ATA Flash Card does not have Power Level 1 commands.

If set to 0, indicates that the PCMCIA ATA Flash Card has Power Level 1 commands

Bit 12: -XE

If set to 1, indicates that Power Level 1 commands are disabled.

If set to 0, indicates that Power Level 1 commands are enabled.

Bit 0-11: Maximum current

This field contains the PCMCIA ATA Flash Card's maximum current in mA.

6.2.6.32. Word 162: Key Management Schemes Supported

Bit 0: CPRM support

If set to 1, the device supports CPRM Scheme (Content Protection for Recordable Media)

If set to 0, the device does not support CPRM.

Bits 1-15 are reserved for future additional Key Management schemes.

6.2.6.33. Word 163: CF Advanced True IDE Timing Mode Capabilities and Settings

This word describes the capabilities and current settings for CFA defined advanced timing modes using the True IDE interface.

Notice! The use of True IDE PIO Modes 5 and above or of Multiword DMA Modes 3 and above impose significant restrictions on the implementation of the host as indicated in Additional Requirements for CF Advanced Timing Modes.

There are four separate fields defined that describe support and selection of Advanced PIO timing modes and Advanced Multiword DMA timing modes. The older modes are reported in words 63 and 64 as described in Word 63: Multiword DMA transfer and Word 64: Advanced PIO transfer modes supported.

Bits 2-0: Advanced True IDE PIO Mode Support

Indicates the maximum True IDE PIO mode supported by the card.

Value	Maximum PIO mode timing supported
0	Specified in word 64
1	PIO Mode 5
2	PIO Mode 6
3-7	Reserved

Bits 5-3: Advanced True IDE Multiword DMA Mode Support
Indicates the maximum True IDE Multiword DMA mode supported by the card.

Value	Maximum Multiword DMA timing mode supported
0	Specified in word 63
1	Multiword DMA Mode 3
2	Multiword DMA Mode 4
3-7	Reserved

Bits 8-6: Advanced True IDE PIO Mode Selected
Indicates the current True IDE PIO mode selected on the card.

Value	Current PIO timing mode selected
0	Specified in word 64
1	PIO Mode 5
2	PIO Mode 6
3-7	Reserved

Bits 11-9: Advanced True IDE Multiword DMA Mode Selected
Indicates the current True IDE Multiword DMA Mode Selected on the card.

Value	Current Multiword DMA timing mode selected
0	Specified in word 63
1	Multiword DMA Mode 3
2	Multiword DMA Mode 4
3-7	Reserved

Bits 15-12 are reserved.

6.2.6.34. Word 164: CF Advanced PCMCIA I/O and Memory Timing Modes Capabilities and Settings

This word describes the capabilities and current settings for CFA defined advanced timing modes using the Memory and PCMCIA I/O interface.

Notice! The use of PCMCIA I/O or Memory modes that are 100ns or faster impose significant restrictions on the implementation of the host as indicated in Additional Requirements for CF Advanced Timing Modes.

Bits 2-0: Maximum Advanced PCMCIA I/O Mode Support
Indicates the maximum I/O timing mode supported by the card.

Value	Maximum PCMCIA IO timing mode supported
0	255 ns Cycle PCMCIA I/O Mode
1	120 ns Cycle PCMCIA I/O Mode
2	100 ns Cycle PCMCIA I/O Mode
3	80 ns Cycle PCMCIA I/O Mode
4-7	Reserved

Bits 15-6: Reserved.

6.2.7. Idle—97H or E3H

Bit ->	7	6	5	4	3	2	1	0
--------	---	---	---	---	---	---	---	---

Command (7)	97h or E3h		
C/D/H (6)	X	Drive	X
Cyl High (5)	X		
Cyl Low (4)	X		
Sec Num (3)	X		
Sec Cnt (2)	Timer Count (5 msec increments)		
Feature (1)	X		

Figure 34: Idle

This command causes the PCMCIA ATA Flash Card to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5 msec) is different from the ATA specification.

6.2.8. Idle Immediate—95 or ,E1H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	95h or E1h							
C/D/H (6)	X			Drive		X		
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 35: Idle Immediate

This command causes the PCMCIA ATA Flash Card to set BSY, enter the Idle mode, clear BSY and generate an interrupt.

6.2.9. Initialize Drive Parameters—91H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	91h							
C/D/H (6)	X	0	X	Drive	Max Head (no. of heads-1)			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Number of Sectors							
Feature (1)	X							

Figure 36: Initialize Drive Parameters

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Card/Drive/Head registers are used by this command.

6.2.10. Key Management Structure Read – B9h (Feature: 0-127)

Bit ->	7	6	5	4	3	2	1	0
Command (7)	B9h							
C/D/H (6)	Reserved (0)			Drive	Reserved (0)			
Cyl High (5)	C7-0							
Cyl Low (4)	C15-8							

Sec Num (3)	C23-16		
Sec Cnt (2)	C31-24		
Feature (1)	0	C38-32	

Feature 37: key Management Structure Read

The KEY MANAGEMENT STRUCTURE READ command is optional, depending on the Key Management scheme in use.

This command returns a 512-byte Key Management data structure via PIO data-in transfer. The structure encodes device Key Management status defined by the Key Management scheme in use. In some schemes, this structure may include a cryptographic response.

The values 39-bit value C38-0 is a random number picked by the host. It is used as a challenge value by some Key Management schemes. All 39-bit values are acceptable.

6.2.11. Key Management Read Keying Material –B9h (Feature : 80)

Bit ->	7	6	5	4	3	2	1	0
Command (7)	B9h							
C/D/H (6)	Reserved (0)			Drive	Reserved (0)			
Cyl High (5)	Reserved (0)							
Cyl Low (4)	Keying Material Sector Offset - High							
Sec Num (3)	Keying Material Sector Offset - Low							
Sec Cnt (2)	Keying Material Count							
Feature (1)	80h							

Feature 38: key Management Read Keying Material

The KEY MANAGEMENT READ KEYING MATERIAL command is optional, depending on the Key Management scheme in use.

This command reads from 1 to 256 sectors as specified in the Sector Count register. A Sector Count of 0 requests 256 sectors. The transfer shall begin at the Sector Offset within the keying material specified in the 16 bit number comprised of the Sector Number and Cylinder Low registers. The size and format of the keying material is specific to the Key Management scheme in use.

If an uncorrectable error occurs reading the keying material, the Sector Number and Cylinder Low registers are left indicating the offset of the sector in error.

6.2.12. Key Management Change Key Management Value – B9h (Feature : 81)

Bit ->	7	6	5	4	3	2	1	0
Command (7)	B9h							
C/D/H (6)	Reserved (0)			Drive	Reserved (0)			
Cyl High (5)	B2h							
Cyl Low (4)	6Eh							
Sec Num (3)	Reserved (0)							
Sec Cnt (2)	Reserved (0)							
Feature (1)	81h							

Feature 39: Key Management Change Key Management Value

The KEY MANAGEMENT CHANGE KEY MANAGEMENT VALUE command is optional, depending on the Key Management scheme in use.

This command causes the device to change a value found in the KEY MANAGEMENT READ KEY MANAGEMENT STRUCTURE response. The method is specific to the Key Management scheme in use. The special value B26Eh in the cylinder registers is checked by the card to make it less likely that the command was executed by mistake.

6.2.13. NOP – 00h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	00h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 40: NOP

This command always fails with the PCMCIA ATA Flash Card returning command aborted.

6.2.14. Read Buffer – E4h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E4h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 41: Read Buffer

The Read Buffer command enables the host to read the current contents of the PCMCIA ATA Flash Card's sector buffer. This command has the same protocol as the Read Sector(s) command.

6.2.15. Read DMA – C8h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E4h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 42: Read DMA

This command uses DMA mode to read from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the PCMCIA ATA Flash Card sets BSY, puts all or part of the sector of data in the buffer. The Card is then permitted, although not required, to set DRQ, clear BSY. The Card asserts DMAREQ while data is available to be transferred. The Card asserts DMAREQ while data is available to be transferred. The host then reads the (512 * sector-count) bytes of data from the Card using DMA. While DMAREQ is asserted by the Card, the Host asserts -DMACK while it is ready to transfer data by DMA and asserts -IORD once for each 16 bit word to be transferred to the Host.

Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The amount of data transferred is indeterminate.

When a Read DMA command is received by the Card and 8 bit transfer mode has been enabled by the Set Features command, the Card shall return the Aborted error.

6.2.16. Read Long Sector—22H, 23H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	22h or 23h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 43: Read Long Sector

The Read Long command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes. During a Read Long command, the PCMCIA ATA Flash Card does not check the ECC bytes to determine if there has been a data error. Only single sector read long operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC data transferred in byte mode. This command has the same protocol as the Read Sector(s) command. Use of this command is not recommended.

6.2.17. Read Multiple—C4h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C4h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 44: Read Multiple

Note: This specification requires that PCMCIA ATA Flash Cards support a multiple block count of 1 and permits larger values to be supported.

The Read Multiple command performs similarly to the Read Sectors command. Interrupts are not generated on every sector, but on the transfer of a block, which contains the number of sectors defined by a Set Multiple command.

Command execution is identical to the Read Sectors operation except that the number of sectors defined by a Set Multiple command is transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which shall be executed prior to the Read Multiple command. When the Read Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the

number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where

$$n = (\text{sector count}) \text{ modulo } (\text{block count}).$$

If the Read Multiple command is attempted before the Set Multiple Mode command has been executed or when Read Multiple commands are disabled, the Read Multiple operation is rejected with an Aborted Command error. Disk errors encountered during Read Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer shall take place as it normally would, including transfer of corrupted data, if any.

Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read Sector(s) Command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block that contained the error.

6.2.18. Read Sector(s)—20H, 21H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	20h or 21h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)				Cylinder High (LBA 23-16)				
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 45: Read Sector(s)

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has been read by the host, the PCMCIA ATA Flash Card sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 bytes of data from the buffer.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

6.2.19. Read Verify Sector(s)—40H, 41H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	40h or 41h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							

Sec Num (3)	Sector Number (LBA 7-0)
Sec Cnt (2)	Sector Count
Feature (1)	X

Figure 46: Read Verify Sector(s)

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the PCMCIA ATA Flash Card sets BSY.

When the requested sectors have been verified, the PCMCIA ATA Flash Card clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the cylinder, head, and sector number of the last sector verified.

If an error occurs, the Read Verify Command terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

6.2.20. Recalibrate—1XH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	1Xh							
C/D/H (6)	1	LBA	1	Drive		X		
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 47: Recalibrate

This command is effectively a NOP command to the PCMCIA ATA Flash Card and is provided for compatibility purposes.

6.2.21. Request Sense—03h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	03h							
C/D/H (6)	1	X	1	Drive		X		
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 48: Request Sense

This command requests extended error information for the previous command.

Table 41: Extended Error Codes

Extended Error Code	Description
00h	No Error Detected
01h	Self Test OK (No Error)
09h	Miscellaneous Error
20h	Invalid Command
21h	Invalid Address (Requested Head or Sector Invalid)
2Fh	Address Overflow (Address Too Large)
35h, 36h	Supply or generated Voltage Out of Tolerance

11h	Uncorrectable ECC Error
18h	Corrected ECC Error
05h, 30-34h, 37h, 3Eh	Self Test or Diagnostic Failed
10h, 14h	ID Not Found
3Ah	Spare Sectors Exhausted
1Fh	Data Transfer Error / Aborted Command
0Ch, 38h, 3Bh, 3Ch, 3Fh	Corrupted Media Format
03h	Write / Erase Failed
22h	Power Level 1 Disabled

6.2.22. Seek—7XH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	7Xh							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 49: Seek

This command is effectively a NOP command to the PCMCIA ATA Flash Card although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

6.2.23. Set Features—EFH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	EFh							
C/D/H (6)		X		Drive		X		
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Config							
Feature (1)	Feature							

Figure 50: Set Features

This command is used by the host to establish or select certain features. If any subcommand input value is not supported or is invalid, the Compact Flash Storage Card shall return command aborted. Table 42: Feature Supported defines all features that are supported.

Table 42: Feature Supported

Feature	Operation
01h	Enable 8 bit data transfers.
02h	Enable Write Cache.
03h	Set transfer mode based on value in Sector Count register.
05h	Enable Advanced Power Management.
09h	Enable Extended Power operations. <i>(Alert: It has been proposed to remove this feature from a future revision of the specification. Please notify the CFA if you have a requirement for this feature.)</i>
0Ah	Enable Power Level 1 commands.

Feature	Operation
44h	Product specific ECC bytes apply on Read/Write Long commands.
55h	Disable Read Look Ahead.
66h	Disable Power on Reset (POR) establishment of defaults at Soft Reset.
69h	NOP - Accepted for backward compatibility.
81h	Disable 8 bit data transfer.
82h	Disable Write Cache.
85h	Disable Advanced Power Management.
89h	Disable Extended Power operations. (<i>Alert: It has been proposed to remove this feature from a future revision of the specification. Please notify the CFA if you have a requirement for this feature.</i>)
8Ah	Disable Power Level 1 commands.
96h	NOP - Accepted for backward compatibility.
97h	Accepted for backward compatibility. Use of this Feature is not recommended.
9Ah	Set the host current source capability. Allows tradeoff between current drawn and read/write speed.
AAh	Enable Read Look Ahead.
BBh	4 bytes of data apply on Read/Write Long commands.
CCh	Enable Power on Reset (POR) establishment of defaults at Soft Reset.

Features 01h and 81h are used to enable and clear 8 bit data transfer modes in True IDE Mode. If the 01h feature command is issued all data transfers shall occur on the low order D[7:0] data bus and the -IOIS16 signal shall not be asserted for data register accesses. The host shall not enable this feature for DMA transfers.

Features 02h and 82h allow the host to enable or disable write cache in PCMCIA ATA Flash Cards that implement write cache. When the subcommand disable write cache is issued, the PCMCIA ATA Flash Card shall initiate the sequence to flush cache to non-volatile memory before command completion.

Feature 03h allows the host to select the PIO or Multiword DMA transfer mode by specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. One PIO mode shall be selected at all times. For Cards which support DMA, one Multiword DMA mode shall be selected at all times. The host may change the selected modes by the Set Features command.

Table 43: Transfer mode values

Mode	Bits (7:3)	Bits (2:0)
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	Mode
Reserved	00010b	N/A
Multiword DMA mode	00100b	Mode
Ultra DMA Mode	01000b	Mode
Reserved	10000b	N/A
Mode = transfer mode number		

If a PCMCIA ATA Flash Card supports PIO modes greater than 0 and receives a Set Features command with a Set Transfer Mode parameter and a Sector Count register value of "00000000b", it shall set its default PIO mode. If the value is "00000001b" and the PCMCIA ATA Flash Card supports disabling of IORDY, then the PCMCIA ATA Flash Card shall set its default PIO mode and disable IORDY. A PCMCIA ATA Flash Card shall support all PIO modes below the highest mode supported, e.g., if PIO mode 1 is supported PIO mode 0 shall be supported.

Support of IORDY is mandatory when PIO mode 3 or above is the current mode of operation.

A PCMCIA ATA Flash Card reporting support for Multiword DMA modes shall support all Multiword DMA modes below the highest mode supported. For example, if Multiword DMA mode 2 support is reported, then modes 1 and 0 shall also be supported.

A PCMCIA ATA Flash Card reporting support for Ultra DMA modes shall support all Ultra DMA modes below the highest mode supported. For example, if Ultra DMA mode 2 support is reported then modes 1 and 0 shall also be supported.

If an Ultra DMA mode is enabled any previously enabled Multiword DMA mode shall be disabled by the device. If a Multiword DMA mode is enabled any previously enabled Ultra DMA mode shall be disabled by the device. Feature 05h allows the host to enable Advanced Power Management. To enable Advanced Power Management, the host writes the Sector Count register with the desired advanced power management level and then executes a Set Features command with subcommand code 05h. The power management level is a scale from the lowest power consumption setting of 01h to the maximum performance level of FEh. Table 44: Advanced power management levels shows these values.

Table 44: Advanced power management levels

Level	Sector Count Value
Maximum performance	FEh
Intermediate power management levels without Standby	81h-FDh
Minimum power consumption without Standby	80h
Intermediate power management levels with Standby	02h-7Fh
Minimum power consumption with Standby	01h
Reserved	FFh
Reserved	00h

Device performance may increase with increasing power management levels. Device power consumption may increase with increasing power management levels. The power management levels may contain discrete bands. For example, a device may implement one power management method from 80h to A0h and a higher performance, higher power consumption method from level A1h to FEh. Advanced power management levels 80h and higher do not permit the device to spin down to save power.

Feature 85h disables Advanced Power Management. Subcommand 85h may not be implemented on all devices that implement Set Features subcommand 05h.

Features 0Ah and 8Ah are used to enable and disable Power Level 1 commands. Feature 0Ah is the default feature for the PCMCIA ATA Flash Card with extended power.

Features 55h and BBh are the default features for the PCMCIA ATA Flash Card; thus, the host does not have to issue this command with these features unless it is necessary for compatibility reasons.

Feature code 9Ah enables the host to configure the card to best meet the host system's power requirements. The host sets a value in the Sector Count register that is equal to one-fourth of the desired maximum average current (in mA) that the card should consume. For example, if the Sector Count register were set to 6, the card would be configured to provide the best possible performance without exceeding 24 mA. Upon completion of the command, the card responds to the host with the range of values supported by the card. The minimum value is set in the Cylinder Low register, and the maximum value is set in the Cylinder Hi register. The default value, after a power on reset, is to operate at the highest performance and therefore the highest current mode. The card shall accept values outside this programmable range, but shall operate at either the lowest power or highest performance as appropriate.

Features 66h and CCh can be used to enable and disable whether the Power On Reset (POR) Defaults shall be set when a soft reset occurs. The default setting is to revert to the POR defaults when a soft reset occurs.

6.2.24. Set Multiple Mode—C6h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C6h							
C/D/H (6)		X		Drive		X		

Cyl High (5)	X
Cyl Low (4)	X
Sec Num (3)	X
Sec Cnt (2)	Sector Count
Feature (1)	X

Figure 51: Set Multiple Mode

This command enables the PCMCIA ATA Flash Card to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count Register is loaded with the number of sectors per block. Upon receipt of the command, the PCMCIA ATA Flash Card sets BSY to 1 and checks the Sector Count Register.

If the Sector Count Register contains a valid value and the block count is supported, the value is loaded and execution is enabled for all subsequent Read Multiple and Write Multiple commands.

If the block count is not supported, an Aborted Command error is posted and the Read Multiple and Write Multiple commands are disabled. If the Sector Count Register contains 0 when the command is issued, Read and Write Multiple commands are disabled. At power on, or after a hardware or (unless disabled by a Set Feature command) software reset, the default mode is Read and Write Multiple disabled.

6.2.25. Set Sleep Mode-99H or E6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	99h or E6h							
C/D/H (6)	X			Drive			X	
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 52: Set Sleep Mode

This command causes the PCMCIA ATA Flash Card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 5 milliseconds. Note that this time base (5 msec) is different from the ATA Specification.

6.2.26. Standby-96H, E2H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	96h or E2h							
C/D/H (6)		X		Drive			X	
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 53: Standby

This command causes the PCMCIA ATA Flash Card to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

6.2.27. Standby Immediate—94H, E0H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	94h or E0h							
C/D/H (6)		X		Drive		X		
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 54: Standby Immediate

This command causes the PCMCIA ATA Flash Card to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

6.2.28. Translate Sector—87H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	87h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 55: Translate Sector

This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. The controller responds with a 512 byte buffer of information containing the desired cylinder, head and sector, including its Logical Address, and the Hot Count, if available, for that sector. Table 45 represents the information in the buffer. Please note that this command is unique to the PCMCIA ATA Flash Card.

Table 45: Translate Sector Information

Address	Information
00h-01h	Cylinder MSB (00), Cylinder LSB (01)
02h	Head
03h	Sector
04h-06h	LBA MSB (04) - LSB (06)
07h-12h	Reserved
13h	Erased Flag (FFh) = Erased; 00h = Not Erased
14h – 17h	Reserved
18h-1Ah	Hot Count MSB (18) - LSB (1A) 1
1Bh-1FFh	Reserved

Notes 1) A value of 0 indicates Hot Count is not supported.

6.2.29. Wear Level—F5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F5h							
C/D/H (6)	X	X	X	Drive	Flag			
Cyl High (5)	X							
Cyl Low (4)	X							

Sec Num (3)	X
Sec Cnt (2)	Completion Status
Feature (1)	X

Figure 56: Wear Level

For the PCMCIA ATA Flash Cards that do not support security mode feature set, this command is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register shall always be returned with a 00h indicating Wear Level is not needed. If the PCMCIA ATA Flash Card supports security mode feature set, this command shall be handled as Security Freeze Lock.

6.2.30. Write Buffer—E8H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E8h							
C/D/H (6)		X		Drive		X		
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 57: Write Buffer

The Write Buffer command enables the host to overwrite contents of the PCMCIA ATA Flash Card's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfers 512 bytes.

6.2.31. Write DMA – C4h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	CAh							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 58: Write DMA

This command uses DMA mode to write from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the PCMCIA ATA Flash Card sets BSY, puts all or part of the sector of data in the buffer. The Card is then permitted, although not required, to set DRQ, clear BSY. The Card asserts DMAREQ while data is available to be transferred. The host then writes the (512 * sector-count) bytes of data to the Card using DMA. While DMAREQ is asserted by the Card, the Host asserts -DMACK while it is ready to transfer data by DMA and asserts -IOWR once for each 16 bit word to be transferred from the Host.

Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The amount of data transferred is indeterminate. When a Write DMA command is received by the Card and 8 bit transfer mode has been enabled by the Set

Features command, the Card shall return the Aborted error.

6.2.32. Write Long Sector—32H, 33H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	32h or 33h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 59: Write Long Sector

This command is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes. Only single sector Write Long operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC transferred in byte mode. Because of the unique nature of the solid-state PCMCIA ATA Flash Card, the four bytes of ECC transferred by the host may be used by the PCMCIA ATA Flash Card. The PCMCIA ATA Flash Card may discard these four bytes and write the sector with valid ECC data. This command has the same protocol as the Write Sector(s) command. Use of this command is not recommended.

6.2.33. Write Multiple Command—C5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C5h							
C/D/H (6)	1	LBA	1	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 60: Write Multiple Command

Note: This specification requires that PCMCIA ATA Flash Cards support a multiple block count of 1 and permits larger values to be supported.

This command is similar to the Write Sectors command. The PCMCIA ATA Flash Card sets BSY within 400 nsec of accepting the command. Interrupts are not presented on each sector but on the transfer of a block that contains the number of sectors defined by Set Multiple. Command execution is identical to the Write Sectors operation except that the number of sectors defined by the Set Multiple command is transferred without intervening interrupts.

DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which shall be executed prior to the Write Multiple command.

When the Write Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

$$n = (\text{sector count}) \bmod (\text{block count}).$$

If the Write Multiple command is attempted before the Set Multiple Mode command has been executed or when Write

Multiple commands are disabled, the Write Multiple operation shall be rejected with an aborted command error.

Errors encountered during Write Multiple commands are posted after the attempted writes of the block or partial block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

The Command Block Registers contain the cylinder, head and sector numbers of the sector where the error occurred. The Sector Count Register contains the residual number of sectors that need to be transferred for successful completion of the command, e.g., each block has 4 sectors, a request for 8 sectors is issued and an error occurs on the third sector. The Sector Count Register contains 6 and the address is that of the third sector.

6.2.34. Write Multiple without Erase— CDH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	CDh							
C/D/H (6)	X1	LBA	1	Drive			Head	
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 61: Write Multiple without Erase

This command is similar to the Write Multiple command with the exception that an implied erase before write operation is not performed. The sectors should be pre-erased with the Erase Sector(s) command before this command is issued.

6.2.35. Write Sector(s)—30H, 31H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	30h or 31h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 62: Write Sector(s)

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the PCMCIA ATA Flash Card sets BSY, then sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY shall be set and DRQ shall be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It shall remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated.

If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

6.2.36. Write Sector(s) without Erase—38H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	38h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 63: Write Sector(s) without Erase

This command is similar to the Write Sector(s) command with the exception that an implied erase before write operation is not performed. This command has the same protocol as the Write Sector(s) command. The sectors should be pre-erased with the Erase Sector(s) command before this command is issued. If the sector is not pre-erased with the Erase Sector(s) command, a normal write sector operation will occur.

6.2.37. Write Verify Sector(s)—3CH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	3Ch							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 64: Write Verify

This command is similar to the Write Sector(s) command, except each sector is verified immediately after being written. This command has the same protocol as the Write Sector(s) command.

6.3. Card Information Structure (CIS)

The default Card Information Structure (CIS) is defined as following. The CIS can be modified during initialization.

Table 46: Card Information Structure

Address	Data	Description of Contents	CIS function
000H	01h	CISTPL_DEVICE	Tuple code
002H	03h	TPL_LINK	Tuple link
004H	d9h	Device information	Tuple data
006H	01h	Device information	Tuple data
008H	ffh	END MARKER	Tuple data
00AH	1ch	CISTPL_DEVICE_OC	Tuple code
00CH	04h	TPL_LINK	Tuple link
00EH	03h	Conditions information	Tuple data
010H	d9h	Device information	Tuple data
012H	01h	Device information	Tuple data
014H	ffh	END MARKER	Tuple data
016H	18h	CISTPL_JEDEC_C	Tuple code
018H	02h	TPL_LINK	Tuple link
01AH	dfh	PCMCIA's manufacture's JEDEC ID code	Tuple data
01CH	01h	PCMCIA's JEDEC device code	Tuple data
01EH	20h	CISTPL_MANFID	Tuple code
020H	04h	TPL_LINK	Tuple link
022H	00h	Low byte of manufacturer's ID code	Tuple data
024H	00h	High byte of manufacturer's ID code	Tuple data
026H	00h	Low byte of product code	Tuple data
028H	00h	High byte of product code	Tuple data
02AH	15h	CISTPL_VERS_1	Tuple code
02CH	20h	TPL_LINK	Tuple link
02EH	04h	TPLL11_MAJOR	Tuple data
030H	01h	TPLL11_MINOR	Tuple data
032H	33h	'I' (Vender Specific Strings)	Tuple data
034H	53h	'N' (Vender Specific Strings)	Tuple data
036H	20h	'D' (Vender Specific Strings)	Tuple data
038H	53h	' ' (Vender Specific Strings)	Tuple data
03AH	59h	'A' (Vender Specific Strings)	Tuple data
03CH	53h	'T' (Vender Specific Strings)	Tuple data

Address	Data	Description of Contents	CIS function
03EH	54h	'A' (Vender Specific Strings)	Tuple data
040H	45h	' ' (Vender Specific Strings)	Tuple data
042H	4dh	'8' (Vender Specific Strings)	Tuple data
044H	53h	'G' (Vender Specific Strings)	Tuple data
046H	2eh	'B' (Vender Specific Strings)	Tuple data
048H	00h	Null terminator	Tuple data
04AH	43h	' ' (Vender Specific Strings)	Tuple data
04CH	46h	' ' (Vender Specific Strings)	Tuple data
04EH	2dh	' ' (Vender Specific Strings)	Tuple data
050H	41h	' ' (Vender Specific Strings)	Tuple data
052H	54h	' ' (Vender Specific Strings)	Tuple data
054H	41h	' ' (Vender Specific Strings)	Tuple data
056H	20h	' ' (Vender Specific Strings)	Tuple data
058H	00h	Null terminator	Tuple data
05AH	56h	'V' (Vender Specific Strings)	Tuple data
05CH	45h	'E' (Vender Specific Strings)	Tuple data
05EH	52h	'R' (Vender Specific Strings)	Tuple data
060H	31h	'1' (Vender Specific Strings)	Tuple data
062H	2eh	'.' (Vender Specific Strings)	Tuple data
064H	30h	'1' (Vender Specific Strings)	Tuple data
066H	30h	'0' (Vender Specific Strings)	Tuple data
068H	20h	' ' (Vender Specific Strings)	Tuple data
06AH	00h	Null terminator	Tuple data
06CH	ffh	END MARKER	Tuple data
06EH	21h	CISTPL_FUNCID	Tuple code
070H	02h	TPL_LINK	Tuple link
072H	04h	IC Card function code	Tuple data
074H	01h	System initialization bit mask	Tuple data
076H	22h	CISTPL_FUNCCE	Tuple code
078H	02h	TPL_LINK	Tuple link
07AH	01h	Type of extended data	Tuple data
07CH	01h	Function information	Tuple data
07EH	22h	CISTPL_FUNCCE	Tuple code
080H	03h	TPL_LINK	Tuple link
082H	02h	Type of extended data	Tuple data

Address	Data	Description of Contents	CIS function
084H	0ch	Function information	Tuple data
086H	0fh	Function information	Tuple data
088H	1ah	CISTPL_CONFIG	Tuple code
08AH	05h	TPL_LINK	Tuple link
08CH	01h	Size field	Tuple data
08EH	03h	Index number of last entry	Tuple data
090H	00h	Configuration register base address (Low)	Tuple data
092H	02h	Configuration register base address (High)	Tuple data
094H	0fh	Configuration register present mask	Tuple data
096H	1bh	CISTPL_CFTABLE_ENTRY	Tuple code
098H	08h	TPL_LINK	Tuple link
09AH	c0h	Configuration Index Byte	Tuple data
09CH	c0h	Interface Descriptor	Tuple data
09EH	a1h	Feature Select	Tuple data
0A0H	01h	Vcc Selection Byte	Tuple data
0A2H	55h	Nom V Parameter	Tuple data
0A4H	08h	Memory length (256 byte pages)	Tuple data
0A6H	00h	Memory length (256 byte pages)	Tuple data
0A8H	20h	Misc features	Tuple data
0AAH	1bh	CISTPL_CFTABLE_ENTRY	Tuple code
0ACH	06h	TPL_LINK	Tuple link
0AEH	00h	Configuration Index Byte	Tuple data
0B0H	01h	Feature Select	Tuple data
0B2H	21h	Vcc Selection Byte	Tuple data
0B4H	b5h	Nom V Parameter	Tuple data
0B6H	1eh	Nom V Parameter	Tuple data
0B8H	4dh	Peak I Parameter	Tuple data
0BAH	1bh	CISTPL_CFTABLE_ENTRY	Tuple code
0BCH	0ah	TPL_LINK	Tuple link
0BEH	c1h	Configuration Index Byte	Tuple data
0C0H	41h	Interface Descriptor	Tuple data
0C2H	99h	Feature Select	Tuple data
0C4H	01h	Vcc Selection Byte	Tuple data
0C6H	55h	Nom V Parameter	Tuple data
0C8H	64h	I/O param	Tuple data

Address	Data	Description of Contents	CIS function
0CAH	f0h	IRQ parameter	Tuple data
0CCH	ffh	IRQ request mask	Tuple data
0CEH	ffh	IRQ request mask	Tuple data
0D0H	20h	Misc features	Tuple data
0D2H	1bh	CISTPL_CFTABLE_ENTRY	Tuple code
0D4H	06h	TPL_LINK	Tuple link
0D6H	01h	Configuration Index Byte	Tuple data
0D8H	01h	Feature Select	Tuple data
0DAH	21h	Vcc Selection Byte	Tuple data
0DCH	b5n	Nom V Parameter	Tuple data
0DEH	1eh	Nom V Parameter	Tuple data
0E0H	4dh	Peak I Parameter	Tuple data
0E2H	1bh	CISTPL_CFTABLE_ENTRY	Tuple code
0E4H	0fn	TPL_LINK	Tuple link
0E6H	c2h	Configuration Index Byte	Tuple data
0E8H	41h	Interface Descriptor	Tuple data
0EAH	99h	Feature Select	Tuple data
0ECH	01h	Vcc Selection Byte	Tuple data
0EEH	55h	Nom V Parameter	Tuple data
0F0H	eah	I/O param	Tuple data
0F2H	61h	I/O range length and size	Tuple data
0F4H	f0h	Base address	Tuple data
0F6H	01h	Base address	Tuple data
0F8H	07h	Address length	Tuple data
0FAH	f6h	Base address	Tuple data
0FCH	03h	Base address	Tuple data
0FEH	01h	Address length	Tuple data
100H	eeh	IRQ parameter	Tuple data
102H	20h	Misc features	Tuple data
104H	1bn	CISTPL_CFTABLE_ENTRY	Tuple code
106H	06h	TPL_LINK	Tuple link
108H	02h	Configuration Index Byte	Tuple data
10AH	01h	Feature Select	Tuple data
10CH	21h	Vcc Selection Byte	Tuple data
10EH	b5n	Nom V Parameter	Tuple data

Address	Data	Description of Contents	CIS function
110H	1eh	Nom V Parameter	Tuple data
112H	4dh	Peak I Parameter	Tuple data
114H	1bh	CISTPL_CFTABLE_ENTRY	Tuple code
116H	0fh	TPL_LINK	Tuple link
118H	c3h	Configuration Index Byte	Tuple data
11AH	41h	Interface Descriptor	Tuple data
11CH	99h	Feature Select	Tuple data
11EH	01h	Vcc Selection Byte	Tuple data
120H	55h	Nom V Parameter	Tuple data
122H	eah	I/O param	Tuple data
124H	61h	I/O range length and size	Tuple data
126H	70h	Base address	Tuple data
128H	01h	Base address	Tuple data
12AH	07h	Address Length	Tuple data
12CH	76h	Base address	Tuple data
12EH	03h	Base address	Tuple data
130H	01h	Address length	Tuple data
132H	eeh	IRQ parameter	Tuple data
134H	20h	Misc features	Tuple data
136H	1bh	CISTPL_CFTABLE_ENTRY	Tuple code
138H	06h	TPL_LINK	Tuple link
13AH	03h	Configuration Index Byte	Tuple data
13CH	01h	Feature Select	Tuple data
13EH	21h	Vcc Selection Byte	Tuple data
140H	b5h	Nom V parameter	Tuple data
142H	1eh	Nom V parameter	Tuple data
144H	4dh	Peak I Parameter	Tuple data
146H	14h	CISTPL_NO_LINK	Tuple code
148H	00h	TPL_LINK	Tuple link
14AH	ffh	CISTPL_END	Tuple data / Tuple link

Ordering Information

1. Part Number List

◆ Industrial Rugged PCMCIA ATA Card – Hermit Series in Removable Disk Type

Grade	Commercial Grade (0°C ~ 70°C)		Industrial Grade (-40°C ~ 85°C)	
	PIO Mode	UDMA Mode	PIO Mode	UDMA Mode
128MB	SRAF128MH-ACSC-PR	SRAF128MH-ACSC-UR	WRAF128MH-AISI-PR	WRAF128MH-AISI-UR
256MB	SRAF256MH-ACSC-PR	SRAF256MH-ACSC-UR	WRAF256MH-AISI-PR	WRAF256MH-AISI-UR
512MB	SRAF512MH-ACSC-PR	SRAF512MH-ACSC-UR	WRAF512MH-AISI-PR	WRAF512MH-AISI-UR
1GB	SRAF001GH-ACSC-PR	SRAF001GH-ACSC-UR	WRAF001GH-AISI-PR	WRAF001GH-AISI-UR
2GB	SRAF002GH-ACSC-PR	SRAF002GH-ACSC-UR	WRAF002GH-AISI-PR	WRAF002GH-AISI-UR
4GB	SRAF004GH-ACSC-PR	SRAF004GH-ACSC-UR	WRAF004GH-AISI-PR	WRAF004GH-AISI-UR
8GB	SRAF008GH-ACSC-PR	SRAF008GH-ACSC-UR	WRAF008GH-AISI-PR	WRAF008GH-AISI-UR
16GB	SRAF016GH-ACSC-PR	SRAF016GH-ACSC-UR	WRAF016GH-AISI-PR	WRAF016GH-AISI-UR

◆ Industrial Rugged PCMCIA ATA Card – Hermit Series in Fixed Disk Type

Grade	Commercial Grade (0°C ~ 70°C)		Industrial Grade (-40°C ~ 85°C)	
	PIO Mode	UDMA Mode	PIO Mode	UDMA Mode
128MB	SRAF128MH-ACSC-PF	SRAF128MH-ACSC-UF	WRAF128MH-AISI-PF	WRAF128MH-AISI-UF
256MB	SRAF256MH-ACSC-PF	SRAF256MH-ACSC-UF	WRAF256MH-AISI-PF	WRAF256MH-AISI-UF
512MB	SRAF512MH-ACSC-PF	SRAF512MH-ACSC-UF	WRAF512MH-AISI-PF	WRAF512MH-AISI-UF
1GB	SRAF001GH-ACSC-PF	SRAF001GH-ACSC-UF	WRAF001GH-AISI-PF	WRAF001GH-AISI-UF
2GB	SRAF002GH-ACSC-PF	SRAF002GH-ACSC-UF	WRAF002GH-AISI-PF	WRAF002GH-AISI-UF
4GB	SRAF004GH-ACSC-PF	SRAF004GH-ACSC-UF	WRAF004GH-AISI-PF	WRAF004GH-AISI-UF
8GB	SRAF008GH-ACSC-PF	SRAF008GH-ACSC-UF	WRAF008GH-AISI-PF	WRAF008GH-AISI-UF
16GB	SRAF016GH-ACSC-PF	SRAF016GH-ACSC-UF	WRAF016GH-AISI-PF	WRAF016GH-AISI-UF

2. Part Number Decoder

S	R	A	F	0	0	8	G	H	-	A	C	S	C	-	U	F	-	U
X	X	X	X	X	X	X	X	X		X	X	X	X		X	X		X
1	2	3	4	5	6	7	8	9		10	11	12	13		14	15		16

1 : Temperature

S = Standard (Commercial temperature)

Operating temperature 0°C ~ 70°C

W = Industrial (Wide temperature)

Operating temperature -40°C ~ 85°C

11 : Controller grading

C = Commercial grade

I = Industrial grade

2 : The material of Frame Kit

P = Plastic ; R = Rugged Metal

12 : The brand of flash memory chip

S = Samsung SLC flash memory

3 **4** : Product category

AF = PCMCIA ATA Card

13 : Flash memory grading

C = Commercial grade

I = Industrial grade

5 **6** **7** **8** : Card capacity

128M = 128MB, 256M = 256MB ,

512M = 512MB, 001G = 1GB , 002G = 2GB,

004G = 4GB, 008G = 8GB, 016G = 16GB

14 : Data transfer mode

P = PIO- 4 mode

U = UDMA-4 mode

9 : The brand of IDE flash controller

15 : Storage type

R = Removable Disk Type

F = Fixed Disk Type

10 : Controller model

16 : Specified by project

Appendix A. Limited Warranty

APRO warrants your Industrial Rugged PCMCIA ATA Card against defects in material and workmanship for the life of the drive. The warranty is void in the case of misuse, accident, alteration, improper installation, misapplication or the result of unauthorized service or repair. The implied warranties of merchantability and fitness for a particular purpose, and all other warranties, expressed or implied, except as set forth in this warranty, shall not apply to the products delivered. In no event shall APRO be liable for any lost profits, lost savings or other incidental or consequential damages arising out of the use of, or inability to use, this product.

BEFORE RETURNING PRODUCT, A RETURN MATERIAL AUTHORIZATION (RMA) MUST BE OBTAINED FROM APRO.

Product shall be returned to APRO with shipping prepaid. If the product fails to conform based on customers' purchasing orders, APRO will reimburse customers for the transportation charges incurred.

Appendix B. After Service

1. Policy

In order to return any item for repair, an RMA (Return Merchandise Authorization) number must be assigned by APRO. Customers need to provide the following information, before an RMA will be issued:

- **Product model**
- **Quantity**
- **Lot number**
- **Defect description**
- **Customer name**
- **Contact person**
- **Email address or telephone number**
- **Shipping address**

In order to receive an RMA number, please contact our customer service department via fax or email:

- **Fax the RMA Request Form to 886-2-2929 0307. The RMA Request Form can be downloaded from <http://www.apro-tw.com/support/rmaform.htm>)**
- **Email to rma@apro-tw.com.tw**

The description of the defect needs to be clear and complete in order for APRO to address the problem according to customer expectations. Without a clear description, APRO can only provide a basic test of the returned products.

1.1. Warranty period

- SRAFxxxH-ACSC- Series 1 year
- WRAFxxxH-AISI- Series 3 years

1.2. Service charge under warranty period

For a warranty repair, there is no charge.

Remark:

The warranty does not cover product damage due to improper operation or force of nature such as fire or flood.

1.3. Service charge for out of warranty period

Out of warranty repair charges are dependent on component cost and labor time. APRO will issue an estimate after diagnosing the problem.

1.4. End of Life service

APRO cannot guarantee repair of any products beyond one year of End-of-Life due to limited availability of replacement components. If repair components are not available, APRO will suggest equivalent products for purchase and offer special pricing.

1.5. Shipping Charges

The customer is responsible for packaging the product such that no additional damage occurs during normal shipping and handling. Any freight-collect shipments without notice in advance will be refused.

For warranty repairs, the customer is responsible for the cost of shipping the product back to APRO. APRO will pay for shipping back to the customer.

For DOA warranty replacements, APRO will pay shipping charges for return and replacement. APRO reserves the right to use the most economical shipping method available.

2. Procedure

The definition of defective products fall into three categories as described below:

- DOA (Defect on Arrival): Defect occurs within 30 days of purchase.
- RMA in warranty period
- RMA out of the warranty period

The above terms are determined by the purchase date on the invoice up to the time to product is returned to APRO. APRO's repair service procedure is as follows:

2.1. Request an RMA Number from APRO:

- (1) Fill out an "RMA Request Form" and send it by fax to +886-2-2929 0307 or e-mail to rma@APRO-tw.com
- (2) APRO's RMA engineer will check that the "RMA Request Form" has been completed with precise information. Then the customer will receive a RMA number.
If you need a replacement rather than wait for the returned defective product to be repaired, this requirement must be noted in your "RMA Request Form".

2.2. Package and Delivery to APRO

- (1) Returned products have to be packed properly to avoid damage during the transportation.
- (2) DOA products: DOA products qualify for complete replacement and have to be returned with all accessories included in the original purchase.

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- (3) Please indicate your unique RMA number on the top outside of the package.
 - (4) To speed up the RMA/DOA procedure, please notify us by e-mail (rma@APRO-tw.com) with information that includes the shipping date, the name of carrier and the tracking number of the package.

2.3. Product Check On Arrival

- (1) APRO's RMA engineer will check your product within 8 hours since arrival.
- (2) If the product arrives undamaged and conforms to the conditions described on the "RMA Request Form", it will be for repairing.
- (3) If the product is damaged or there is some inconsistency with the "RMA Request Form" description, APRO will contact and confirm the status with the customer before proceeding.

2.4. Repair

- (1) The RMA engineer will repair the defect as described by the customer. The products will also be tested to ensure it is in proper working order.
- (2) If no additional problems are detected, APRO will notify the customer.
- (3) If the customer does not reply us within 48 hours, and no failure occurs during testing, the product will be processed as NTF. (No testing failure).

2.5. Charge

The customer will be charged for repairs under below conditions:

- RMA is out of the warranty period
- RMA or DOA terms apply, but it is determined by APRO's RMA engineer that the defect was caused by abuse, misuse or unauthorized repair.

2.6. Package and Delivery to the customer

- (1) We will properly pack the repaired product along with a RMA report.
- (2) The RMA number and quantity will be clearly marked on the package.
- (3) The customer will receive an e-mail notification of the product RMA number and shipping advice.